SAMSUNG ELECTRONICS

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August 1999

SAMSUNG Semiconductor

SDRAM 64Mb

New part system
New millennium business

2000 Data Book

PRINTED IN KOREA

Circuit diagrams utilizing SAMSUNG products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of SAMSUNG or others. SAMSUNG reserves the right to change device specifications.

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M464S0824DT1-L1H,L1L,C1H,C1L ..... 8M x 64 2 row of 4MX16 142

64Mb C-die

M464S0424CT1-L1H,L1L ..... 4M x 64 1 row of 4MX16 153

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B . PC66 SODIMM Datasheet

64Mb D-die

M466S0424DT0-L10,C10 ..... 4M x 64 1 row of 4MX16 177
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64Mb C-die

M466S0424CT0-L10 ..... 4M x 64 1 row of 4MX16 221
M466S0823CT2-L10 ..... 8M x 64 1 row of 8MX 8 232
M466S0823CT3-L10 ..... 8M x 64 1 row of 8MX 8 243
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C . PC100 Registered DIMM (168pin) Datasheet

64Mb D-die

M377S0823DT3-C1H,C1L ..... 8M x 72 1 row of 8MX 8 267
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D . PC133 Registered DIMM (168pin) Datasheet

64Mb D-die

M390S0823DT1-C75 ..... 8M x 72 1 row of 8MX 8 377
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64Mb D-die

M366S0424DTS-C80, C1H, C1L ..... 4M x 64 1 row of 4MX16 403
M366S0823DTS-C80, C1H, C1L ..... 8M x 64 1 row of 8MX 8 414
M366S0824DT0-C80, C1H, C1L ..... 8M x 64 2 row of 4MX16 425
M366S1623DT0-C80, C1H, C1L ..... 16M x 64 2 row of 8MX 8 436
M374S0823DTS-C80, C1H, C1L ..... 8M x 72 1 row of 8MX 8 447
M374S1623DT0-C80, C1H, C1L ..... 16M x 72 2 row of 8MX 8 458

E . PC100 Unbuffered DIMM (168pin) Datasheet (Continued)

64Mb C-die

M366S0424CT0-C80, C1H, C1L ----- 4M x 64 1 row of 4MX16 ---------- 469
M366S0424CTS-C80, C1H, C1L ----- 4M x 64 1 row of 4MX16 ---------- 480
M366S0823CT0-C80, C1H, C1L ----- 8M x 64 1 row of 8MX 8 ---------- 491
M366S0823CTS-C80, C1H, C1L ----- 8M x 64 1 row of 8MX 8 ---------- 502
M366S0824CT0-C80, C1H, C1L ----- 8M x 64 2 row of 4MX16 ---------- 513
M366S1623CT0-C80, C1H, C1L ----- 16M x 64 2 row of 8MX 8 ---------- 524
M374S0823CT0-C80, C1H, C1L ----- 8M x 72 1 row of 8MX 8 ---------- 535
M374S0823CTS-C80, C1H, C1L ----- 8M x 72 1 row of 8MX 8 ---------- 546
M374S1623CT0-C80, C1H, C1L ----- 16M x 72 2 row of 8MX 8 ---------- 557

F . PC133 Unbuffered DIMM (168pin) Datasheet

64Mb D-die

M366S0424DTS-C75 ---------- 4M x 64 1 row of 4MX16 ---------- 571
M366S0823DTS-C75 ---------- 8M x 64 1 row of 8MX 8 ---------- 582
M366S1623DT0-C75 ---------- 16M x 64 2 row of 8MX 8 ---------- 593
M374S0823DTS-C75 ---------- 8M x 72 1 row of 8MX 8 ---------- 604
M374S1623DT0-C75 ---------- 16M x 72 2 row of 8MX 8 ---------- 615

G . PC66 Unbuffered DIMM (168pin) Datasheet

64Mb D-die

M366S0424DTF-C10 ---------- 4M x 64 1 row of 4MX16 ---------- 629
M366S0823DTF-C10 ---------- 8M x 64 1 row of 8MX 8 ---------- 640
M366S0824DTL-C10 ---------- 8M x 64 2 row of 4MX16 ---------- 651
M366S1623DTL-C10 ---------- 16M x 64 2 row of 8MX 8 ---------- 662
M374S0823DTF-C10 ---------- 8M x 72 1 row of 8MX 8 ---------- 673
M374S1623DTL-C10 ---------- 16M x 72 2 row of 8MX 8 ---------- 684

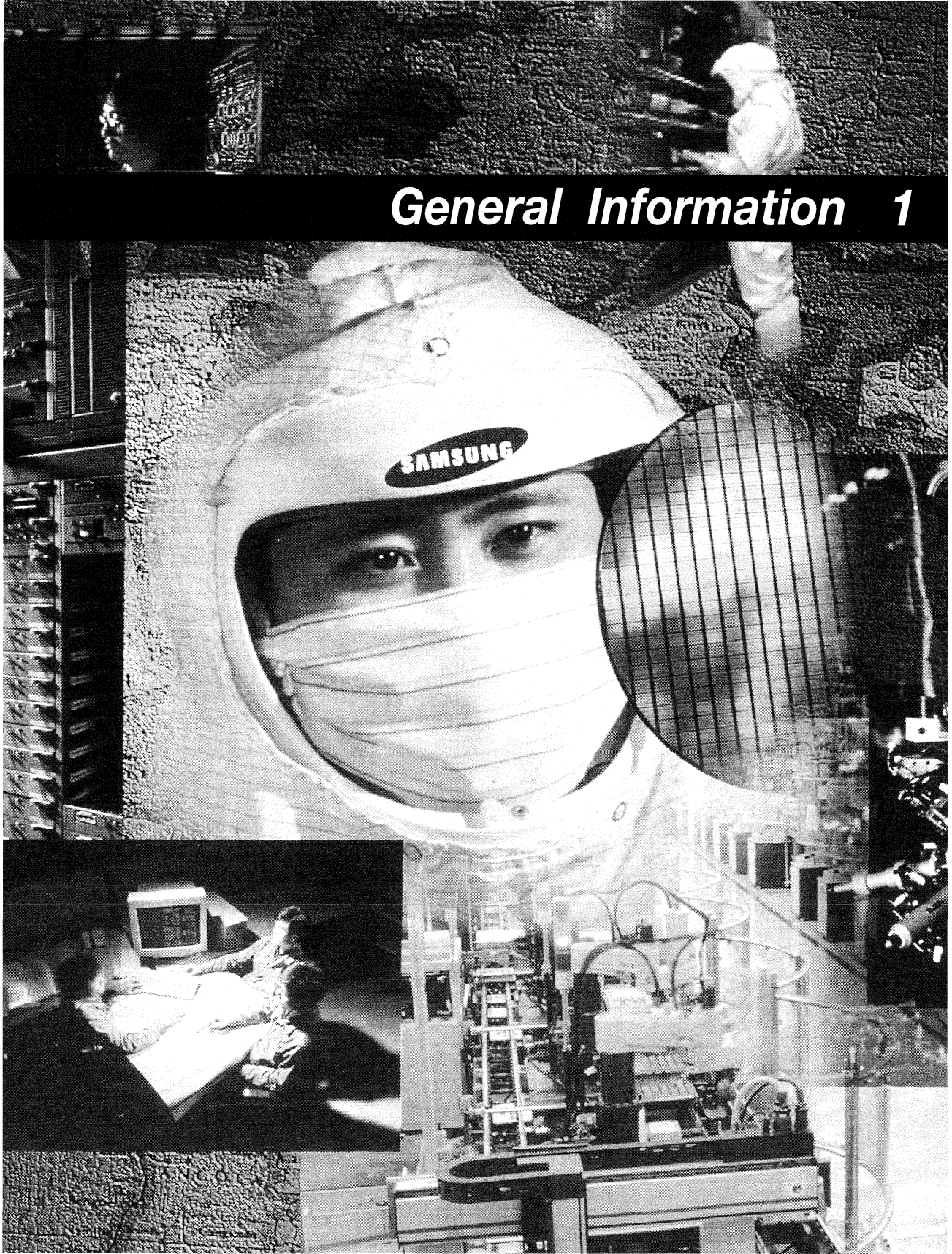
64Mb C-die

M366S0424CTF-C10 ---------- 4M x 64 1 row of 4MX16 ---------- 695
M366S0424CTL-C10 ---------- 4M x 64 1 row of 4MX16 ---------- 706
M366S0823CTF-C10 ---------- 8M x 64 1 row of 8MX 8 ---------- 717
M366S0823CTL-C10 ---------- 8M x 64 1 row of 8MX 8 ---------- 728
M366S0824CTL-C10 ---------- 8M x 64 2 row of 4MX16 ---------- 739
M366S1623CTL-C10 ---------- 16M x 64 2 row of 8MX 8 ---------- 750
M374S0823CTF-C10 ---------- 8M x 72 1 row of 8MX 8 ---------- 761
M374S0823CTL-C10 ---------- 8M x 72 1 row of 8MX 8 ---------- 772
M374S1623CTL-C10 ---------- 16M x 72 2 row of 8MX 8 ---------- 783

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General Information 1

A. SDRAM Component Product Guide

Density	Banks	New Part Number	Old Part Number	Power*1 (-C/-L) & Speed *2	Org.	Inter-face	Ref.	Power (V)	Pkg.	Avail
64M 5th	4Banks	K4S640432D	K4S640432D	C75/C80/C1H/C1L/C10 L75/L80/L1H/L1L/L10	16M x 4	LVTTL	4K	3.3 ± 0.3V	TSOP II 54pin	Now
		K4S640832D	K4S640832D		8M x 8					Now
		K4S641632D	K4S641632D		4M x16					Now
64M 4th	4Banks	K4S640432C	K4S640432C	C75/C80/C1H/C1L/C10 L75/L80/L1H/L1L/L10	16M x 4	LVTTL	4K	3.3 ± 0.3V	TSOP II 54pin	Now
		K4S640832C	K4S640832C		8M x 8					Now
		K4S641632C	K4S641632C		4M x16					Now

Note 1:

Temperature and Power		
NEW	OLD	Description
C	G	Commercial Temperature, Normal Power
L	F	Commercial Temperature, Low Power

Note 2:

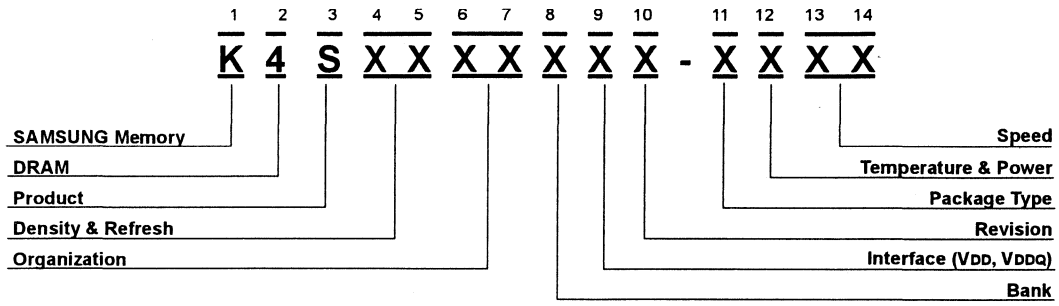
Speed (Default CL=3)		
NEW	OLD	Description
75	A	PC133 (@CL=3)
1H	H	PC100 (@CL=3)
1L	L	PC100 (@CL=3)
10	10	PC66 (@CL=2 & CL=3)
60	6	166Mhz (@CL=3)
70	7	143Mhz (@CL=3)
80	8	125MhZ (@CL=3)

B. SDRAM Module Product Guide

Org.	New Part No.	Old Part No.	Speed	Composition	Comp. Version	Vtg.	Internal Banks	External Banks	Feature	Avail.
144pin PC100 SODIMM										
4M x 64	M464S0424CT1	KMM464S424CT1	L1H, L1L	4M x16 * 4 pcs	64Mb 4th	3.3V	4	1	DS, 1000mil	Now
	M464S0424DT1	KMM464S424DT1	L1H, L1L, C1H, C1L	4M x16 * 4 pcs	64Mb 5th			1	DS, 1000mil	Now
8M x 64	M464S0824CT1	KMM464S824CT1	L1H, L1L	4M x16 * 8 pcs	64Mb 4th			2	DS, 1250mil	Now
	M464S0824DT1	KMM464S824DT1	L1H, L1L, C1H, C1L	4M x16 * 8 pcs	64Mb 5th			2	DS, 1250mil	Now
144pin PC66 SODIMM										
4M x 64	M466S0424CT0	KMM466S424CT	L10	4M x16 * 4 pcs	64Mb 4th	3.3V	4	1	DS, 1000mil	Now
	M466S0424DT0	KMM466S424DT	L10, C10	4M x16 * 4 pcs	64Mb 5th			1	DS, 1000mil	Now
8M x 64	M466S0823CT2	KMM466S823CT2	L10	8M x 8 * 8 pcs	64Mb 4th			1	DS, 1150mil	Now
	M466S0823DT2	KMM466S823DT2	L10, C10	8M x 8 * 8 pcs	64Mb 5th			1	DS, 1150mil	Now
	M466S0823CT3	KMM466S823CT3	L10	8M x 8 * 8 pcs	64Mb 4th			1	DS, 1050mil	Now
	M466S0823DT3	KMM466S823DT3	L10, C10	8M x 8 * 8 pcs	64Mb 5th			1	DS, 1050mil	Now
	M466S0824CT2	KMM466S824CT2	L10	4M x16 * 8 pcs	64Mb 4th			2	DS, 1150mil	Now
	M466S0824DT2	KMM466S824DT2	L10, C10	4M x16 * 8 pcs	64Mb 5th			2	DS, 1150mil	Now
168pin PC100 Registered DIMM										
8M x 72	M350S0823CT1	KMM350S823CT1	C80,C1H,C1L	8M x 8 * 9 pcs	64Mb 4th	3.3 V	4	1	DS, 1500mil	Now
	M377S0823CT1	KMM377S823CT1	C80,C1H,C1L	8M x 8 * 9 pcs	64Mb 4th			1	DS, 1500mil	Now
	M377S0823CT2	KMM377S823CT2	C1H, C1L	8M x 8 * 9 pcs	64Mb 4th			1	DS, 1500mil	Now
	M377S0823CT3	KMM377S823CT3	C1H, C1L	8M x 8 * 9 pcs	64Mb 4th			1	DS, 1500mil	Now
	M377S0823DT3	KMM377S823DT3	C1H, C1L	8M x 8 * 9 pcs	64Mb 5th			1	DS, 1500mil	Now
16M x 72	M377S1620CT1	KMM377S1620CT1	C80,C1H,C1L	16M x 4 * 18 pcs	64Mb 4th			1	DS, 1700mil	Now
	M377S1620CT2	KMM377S1620CT2	C1H, C1L	16M x 4 * 18 pcs	64Mb 4th			1	DS, 1700mil	Now
	M377S1620CT3	KMM377S1620CT3	C1H, C1L	16M x 4 * 18 pcs	64Mb 4th			1	DS, 1700mil	Now
	M377S1620DT3	KMM377S1620DT3	C1H, C1L	16M x 4 * 18 pcs	64Mb 5th			1	DS, 1700mil	Now
168pin PC133 Registered DIMM										
8M x 72	M390S0823DT1	KMM390S823DT1	C75	8M x 8 * 9 pcs	64Mb 5th	3.3 V	4	1	DS, 1500mil	Now
16M x 72	M390S1620DT1	KMM390S1620DT1	C75	16M x 4 * 18 pcs	64Mb 5th			1	DS, 1700mil	Now

Org.	New Part No.	Old Part No.	Speed	Composition	Comp.	Vtg.	Internal	External	Feature	Avail.
168pin PC100 Unbuffered DIMM										
4M x 64	M366S0424CT0	KMM366S424CT	C80,C1H,C1L	4M x16 * 4 pcs	64Mb 4th	3.3 V	4	1	SS, 1375mil	Now
	M366S0424CTS	KMM366S424CTS	C80,C1H,C1L	4M x16 * 4 pcs	64Mb 4th			1	SS, 1000mil	Now
	M366S0424DTS	KMM366S424DTS	C80,C1H,C1L	4M x16 * 4 pcs	64Mb 5th			1	SS, 1000mil	Now
8M x 64	M366S0823CT0	KMM366S823CT	C80,C1H,C1L	8M x 8 * 8 pcs	64Mb 4th			1	SS, 1375mil	Now
	M366S0823CTS	KMM366S823CTS	C80,C1H,C1L	8M x 8 * 8 pcs	64Mb 4th			1	SS, 1375mil	Now
	M366S0823DTS	KMM366S823DTS	C80,C1H,C1L	8M x 8 * 8 pcs	64Mb 5th			1	SS, 1375mil	Now
	M366S0824CT0	KMM366S824CT	C80,C1H,C1L	4M x16 * 8 pcs	64Mb 4th			2	DS, 1375mil	Now
	M366S0824DT0	KMM366S824DT	C80,C1H,C1L	4M x16 * 8 pcs	64Mb 5th			2	DS, 1375mil	Now
8M x 72	M374S0823CT0	KMM374S823CT	C80,C1H,C1L	8M x 8 * 9 pcs	64Mb 4th			1	SS, 1375mil	Now
	M374S0823CTS	KMM374S823CTS	C80,C1H,C1L	8M x 8 * 9 pcs	64Mb 4th			1	SS, 1375mil	Now
	M374S0823DTS	KMM374S823DTS	C80,C1H,C1L	8M x 8 * 9 pcs	64Mb 5th			1	SS, 1375mil	Now
16M x 64	M366S1623CT0	KMM366S1623CT	C80,C1H,C1L	8M x 8 * 16 pcs	64Mb 4th			2	DS, 1375mil	Now
	M366S1623DT0	KMM366S1623DT	C80,C1H,C1L	8M x 8 * 16 pcs	64Mb 5th			2	DS, 1375mil	Now
16M x 72	M374S1623CT0	KMM374S1623CT	C80,C1H,C1L	8M x 8 * 18 pcs	64Mb 4th			2	DS, 1375mil	Now
	M374S1623DT0	KMM374S1623DT	C80,C1H,C1L	8M x 8 * 18 pcs	64Mb 5th			2	DS, 1375mil	Now
168pin PC133 Unbuffered DIMM										
4M x 64	M366S0424DTS	KMM366S424DTS	C75	4M x16 * 4 pcs	64Mb 5th	3.3 V	4	1	SS, 1000mil	Now
8M x 64	M366S0823DTS	KMM366S823DTS	C75	8M x 8 * 8 pcs	64Mb 5th			1	SS, 1375mil	Now
8M x 72	M374S0823DTS	KMM374S823DTS	C75	8M x 8 * 9 pcs	64Mb 5th			1	SS, 1375mil	Now
16M x 64	M366S1623DT0	KMM366S1623DT	C75	8M x 8 * 16 pcs	64Mb 5th			2	DS, 1375mil	Now
16M x 72	M374S1623DT0	KMM374S1623DT	C75	8M x 8 * 18 pcs	64Mb 5th			2	DS, 1375mil	Now
168pin PC66 Unbuffered DIMM										
4M x 64	M366S0424CTL	KMM366S424CTL	C10	4M x16 * 4 pcs	64Mb 4th	3.3 V	4	1	SS, 1000mil	Now
	M366S0424CTF	KMM366S424CTF	C10	4M x16 * 4 pcs	64Mb 4th			1	SS, 1000mil	Now
	M366S0424DTF	KMM366S424DTF	C10	4M x16 * 4 pcs	64Mb 5th			1	SS, 1000mil	Now
8M x 64	M366S0823CTL	KMM366S823CTL	C10	8M x 8 * 8 pcs	64Mb 4th			1	DS, 1000mil	Now
	M366S0823CTF	KMM366S823CTF	C10	8M x 8 * 8 pcs	64Mb 4th			1	SS, 1250mil	Now
	M366S0823DTF	KMM366S823DTF	C10	8M x 8 * 8 pcs	64Mb 5th			1	SS, 1250mil	Now
	M366S0824CTL	KMM366S824CTL	C10	4M x16 * 8 pcs	64Mb 4th			2	DS, 1000mil	Now
	M366S0824DTL	KMM366S824DTL	C10	4M x16 * 8 pcs	64Mb 5th			2	DS, 1000mil	Now
8M x 72	M374S0823CTL	KMM374S823CTL	C10	8M x 8 * 9 pcs	64Mb 4th			1	DS, 1000mil	Now
	M374S0823CTF	KMM374S823CTF	C10	8M x 8 * 9 pcs	64Mb 4th			1	SS, 1250mil	Now
	M374S0823DTF	KMM374S823DTF	C10	8M x 8 * 9 pcs	64Mb 5th			1	SS, 1250mil	Now
16M x 64	M366S1623CTL	KMM366S1623CTL	C10	8M x 8 * 16 pcs	64Mb 4th			2	DS, 1250mil	Now
	M366S1623DTL	KMM366S1623DTL	C10	8M x 8 * 16 pcs	64Mb 5th			2	DS, 1250mil	Now
16M x 72	M374S1623CTL	KMM374S1623CTL	C10	8M x 8 * 18 pcs	64Mb 4th			2	DS, 1250mil	Now
	M374S1623DTL	KMM374S1623DTL	C10	8M x 8 * 18 pcs	64Mb 5th			2	DS, 1250mil	Now

C. SDRAM Component Ordering Information : NEW



1. SAMSUNG Memory (1)

2. DRAM (2)

3. Product(3)

S : SDRAM

4. Density & Refresh(4~5)

64 : 64M, 4K/64ms

5. Organization(6~7)

04 : x 4 08 : x 8
16 : x16 32 : x32

6. Bank(8)

3 : 4 Banks

7. Interface (9) : VDD, VDDQ

2 : LVTTL (3.3V, 3.3V)

8. Revision(10)

M : 1st Gen.
A : 2nd Gen.
B : 3rd Gen.
C : 4th Gen.
D : 5th Gen.

9. Package Type(11)

T : TSOP II (400mil)
C : u - BGA (CSP)

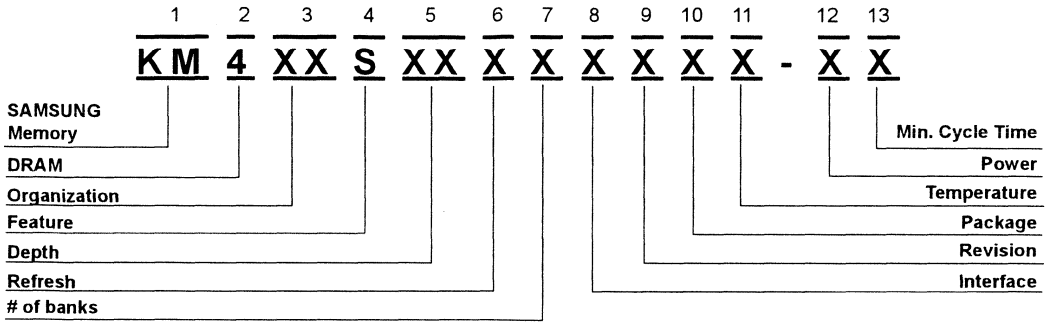
10. Temperature & Power(12)

C : Commecial Normal
L : Commecial Low

11. Speed (13~14) : Default CL= 3

75 : PC133 (133MHz @ CL=3)
1H : PC100 (100MHz @ CL=2 & CL=3)
1L : PC100 (100MHz @ CL=3)
10 : PC66 (66MHz @ CL=2 & CL=3)
60 : 6ns (166MHz @ CL=3)
70 : 7ns (143MHz @ CL=3)
80 : 8ns (125MHz @ CL=3)

D. SDRAM Component Ordering Information : OLD



1. SAMSUNG Memory

2. DRAM

3. Organization

4 : x4 8 : x8
16 : x16 32 : x32

4. Feature

S : SDRAM

5. Depth

1 : 1M	2 : 2M
4 : 4M	8 : 8M
16 : 16M	32 : 32M
64 : 64M	28 : 128M

6. Refresh

0 : 4K
1 : 2K
2 : 8K
3 : 16K

7. # of banks

2 : 2Banks
3 : 4Banks

8. Interface

0 : LVTTL (3.3V)
1 : SSTL-3 (3.3V)
2 : SSTL-2 (2.5V)
3 : LVTTL (2.5V)
4 : LVTTL (3.0V)
5 : SSTL (2.5V)
7 : x4 Stack (Uniframe)
8 : x4 Stack (Flexframe)
9 : x8 Stack (Flexframe)

9. Revision

Blank : 1st Gen.
A : 2nd Gen.
B : 3rd Gen.
C : 4th Gen.
D : 5th Gen.

10. Package

T : TSOP II (400mil)
N : STSOP II
C : u - BGA (CSP)

11. Temperature

Blank : Normal (0°C ~ **70**°C)
E : Extended (-25°C ~ **85**°C)
I : Industrial (-40°C ~ **85**°C)

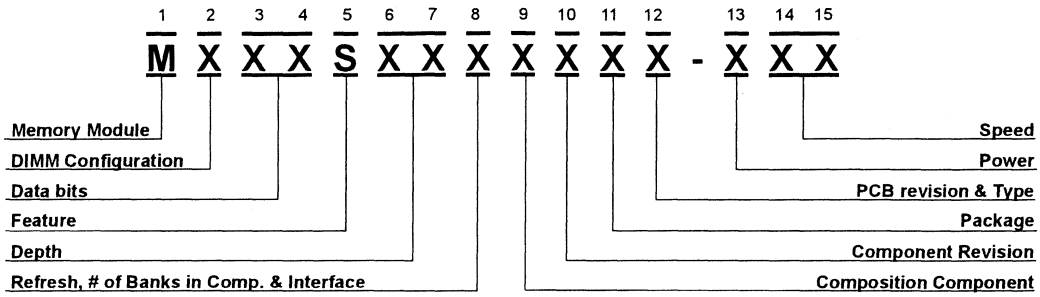
12. Power

G : Auto & Self refresh (3.3V)
F : Auto & Self refresh with Low - power(3.3V)
D : Auto & Self refresh (2.5V)
E : Auto & Self refresh with Low - power(2.5V)
B : Auto & Self refresh (3.0V)
C : Auto & Self refresh with Low - power(3.0V)

13. Min. Cycle Time

A : PC133 (133MHz @ CL=3)
H : PC100 (100MHz @ CL=2 & CL=3)
L : PC100 (100MHz @ CL=3)
10 : PC66 (66MHz @ CL=2 & CL=3)
6 : 6ns (166MHz @ CL=3)
7 : 7ns (143MHz @ CL=3)
8 : 8ns (125MHz @ CL=3)

E. SDRAM Module Ordering Information : NEW



1. Memory Module (1)

2. DIMM Configuration (2)

3 : DIMM
4 : SODIMM

3. Data Bits (3~4)

50 : x72 /ECC w/o PLL + Register DIMM with SPD for 168pin(Intel)
64 : x64 Unbuffered SODIMM with SPD for 144pin (Intel PC100)
66 : x64 Unbuffered DIMM with SPD for 168pin (Intel/JEDEC)
74 : X72 /ECC Unbuffered DIMM with SPD for 168pin (Intel/JEDEC)
77 : x72 /ECC PLL + Register DIMM with SPD for 168pin (Intel PC100)
90 : x72 /ECC PLL + Register DIMM with SPD for 168pin (JEDEC PC133)

4. Feature (5)

S : SDRAM

5. Depth (6~7)

01 :	1M	02 :	2M
04 :	4M,	08 :	8M
		09 :	8M (for 128Mb/512Mb)
16 :	16M	17 :	16M (for 128Mb/512Mb)
32 :	32M	33 :	32M (for 128Mb/512Mb)
64 :	64M	65 :	64M (for 128Mb/512Mb)

6. Refresh, # of Banks in comp. & Interface (8)

1 : 2K/ 32ms Ref., 2Banks & LVTTL
2 : 4K/ 64ms Ref., 4Banks & LVTTL
5 : 8K/ 64ms Ref., 4Banks & LVTTL

7. Composition Component (9)

0 : x 4
3 : x 8
4 : x16
5 : x32
8 : x 4 Stack (Flexframe)
9 : x 8 Stack (Flexframe)

8. Component Revision (10)

M : 1st
A : 2nd Gen. B : 3rd Gen.
C : 4th Gen. D : 5th Gen.

9. Package (11)

T : TSOP II (400mil)
C : u - BGA (CSP)

10. PCB Revision & Type (12)

0 : 1st 1 : 2nd
2 : 3rd 3 : 4th
S : PC100 (4 Layer)
L : PC66 (6 Layer)
F : PC66 (4 Layer)

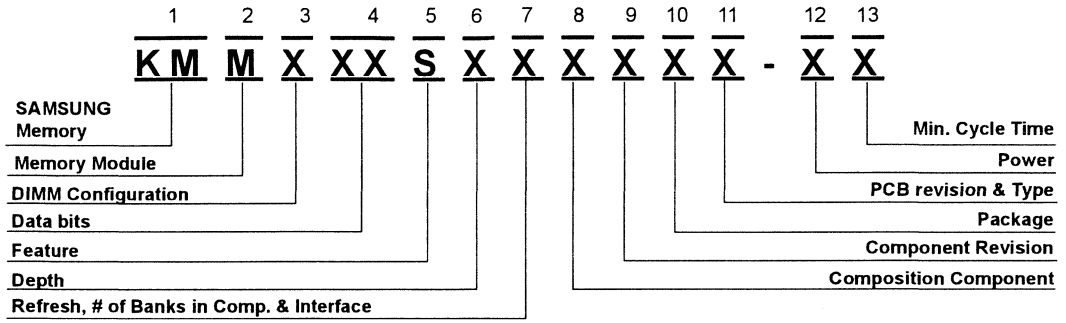
11. Power (13)

C : Auto & Self refresh
L : Auto & Self refresh with Low power

12. Speed (14~15) : Default CL= 3

75 : PC133 (133MHz @ CL=3)
1H : PC100 (100MHz @ CL=2 & CL=3)
1L : PC100 (100MHz @ CL=3)
10 : PC66 (66MHz @ CL=2 & CL=3)
60 : 6ns (166MHz @ CL=3)
70 : 7ns (143MHz @ CL=3)
80 : 8ns (125MHz @ CL=3)

F. SDRAM Module Ordering Information : OLD



1. SAMSUNG Memory

2. Memory Module

3. DIMM Configuration

3 : DIMM
4 : SODIMM

4. Data Bits

50 : x72 Register DIMM + w/o PLL /ECC with SPD for 168pin(Intel)
64 : x64 Unbuffered PC100 SODIMM with SPD for 144pin (Intel)
66 : x64 Unbuffered DIMM with SPD for 168pin(Intel/JEDEC)
74 : X72 /ECC Unbuffered DIMM with SPD for 168pin(Intel/JEDEC)
75 : x72 Register DIMM + PLL /ECC with SPD for 168pin (JEDEC)
77 : x72 Register DIMM + PLL /ECC with SPD for 168pin (Intel)
78 : x72 Register DIMM + PLL /ECC with SPD for 200pin (JEDEC)
90 : x72 Register DIMM + PLL /ECC with SPD for 168pin (RCC)

5. Feature

S : SDRAM

6. Depth

1 :	1M	2 :	2M
4 :	4M,	8 :	8M
		9 :	8M (for 128Mb/512Mb)
16 :	16M	17 :	16M (for 128Mb/512Mb)
32 :	32M	33 :	32M (for 128Mb/512Mb)
64 :	64M	65 :	64M (for 128Mb/512Mb)

7. Refresh, # of Banks in comp. & Interface

0 : 4K/ 64ms Ref., 2Banks & LVTTL
1 : 2K/ 32ms Ref., 2Banks & LVTTL
2 : 4K/ 64ms Ref., 4Banks & LVTTL
3 : 4K/ 64ms Ref., 2Banks & SSTL
4 : 4K/ 64ms Ref., 4Banks & SSTL
5 : 8K/ 64ms Ref., 4Banks & LVTTL
6 : 16K/128ms Ref., 4Banks & LVTTL

8. Composition Component

0 : LVTTL (3.3V) 1 : SSTL-3 (3.3V)
2 : SSTL-2 (2.5V) 3 : LVTTL (2.5V)
4 : LVTTL (3.0V) 5 : SSTL (2.5V)
7 : x4 Stack (Uniframe) 8 : x4 Stack (Flexframe)
9 : x8 Stack (Flexframe)

9. Component Revision

Blank : 1st
A : 2nd Gen. B : 3rd Gen.
C : 4th Gen. D : 5th Gen.

10. Package

T : TSOP II (400mil)
N : STSOP II
C : u - BGA (CSP)

11. PCB Revision & Type

Blank : 1st 1 : 2nd
2 : 3rd 3 : 4th
S : PC100 (4 Layer)

12. Power

G : Auto & Self refresh (3.3V)
F : Auto & Self refresh with Low power(3.3V)

13. Min. Cycle Time

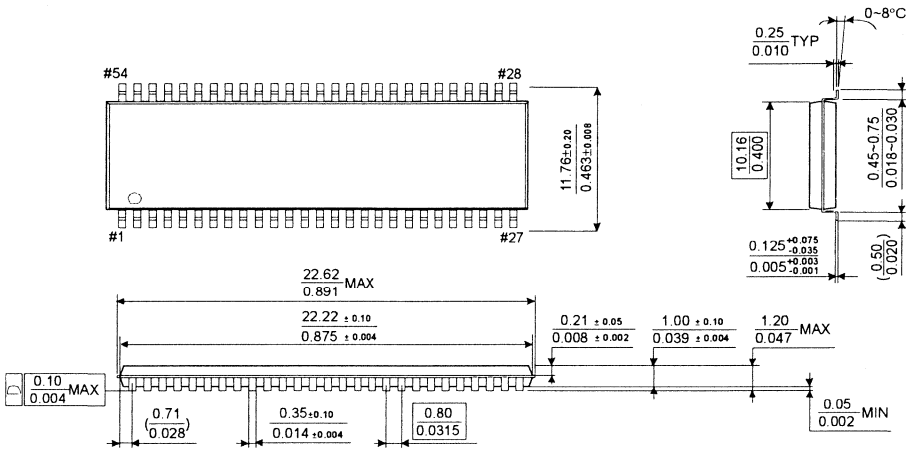
A : PC133 (133MHz @ CL=3)
H : PC100 (100MHz @ CL=2 & CL=3)
L : PC100 (100MHz @ CL=3)
10 : PC66 (66MHz @ CL=2 & CL=3)
6 : 6ns (166MHz @ CL=3)
7 : 7ns (143MHz @ CL=3)
8 : 8ns (125MHz @ CL=3)

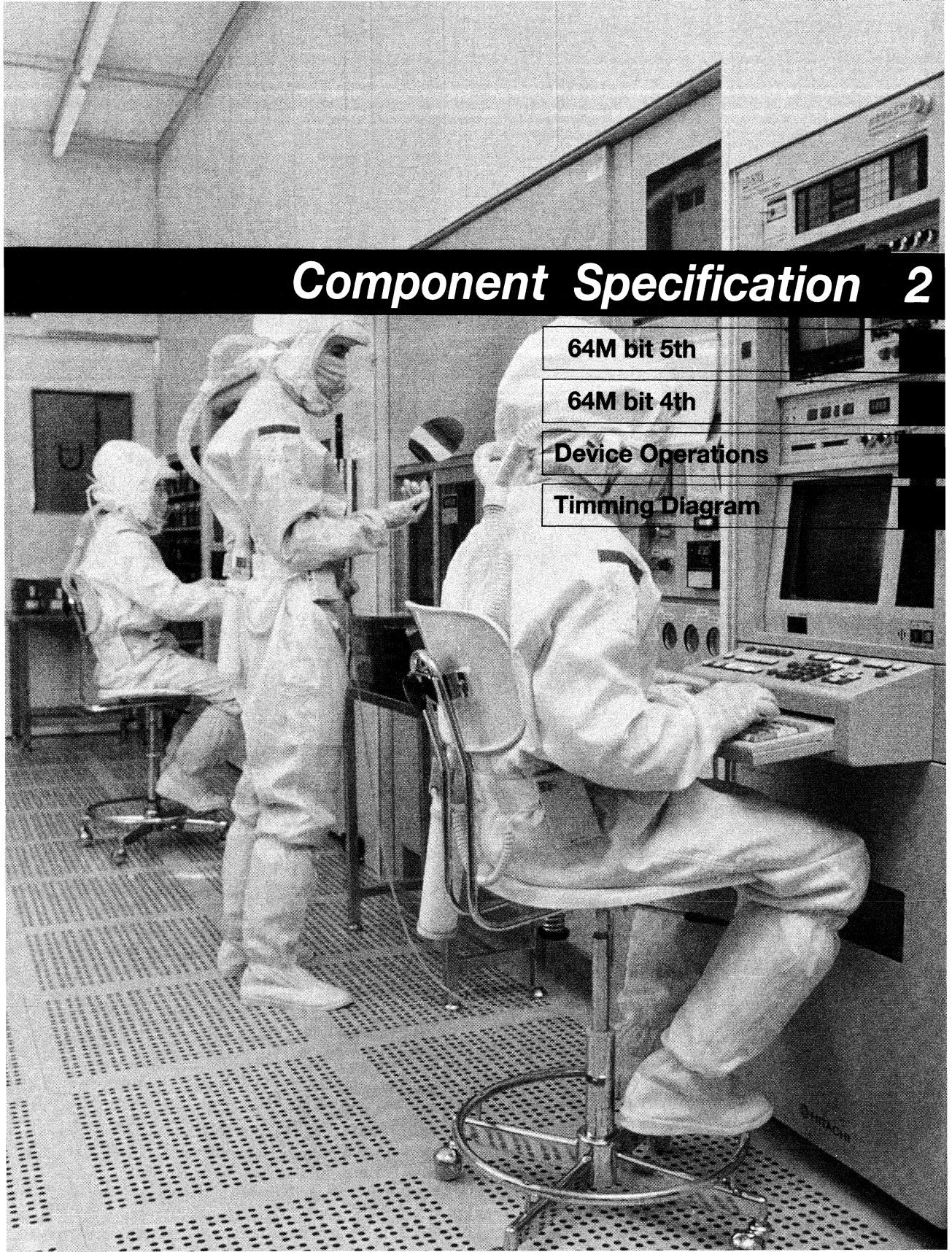
G. Package Dimension

PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE

54-TSOP2-400AF

Unit : Millimeters





Component Specification 2

64M bit 5th

64M bit 4th

Device Operations

Timming Diagram

SEC changed some symbols and test conditions from 64M bit D-die.

• Symbol Change Notice (64Mb D-die)

Before		After	
I_{IL}	Input leakage current (inputs)	I_{LI}	Input leakage current
I_{IL}	Input leakage current (I/O pins)		
I_{OL}	Output open @ DC characteristic table	Io	Output open @ DC characteristic table

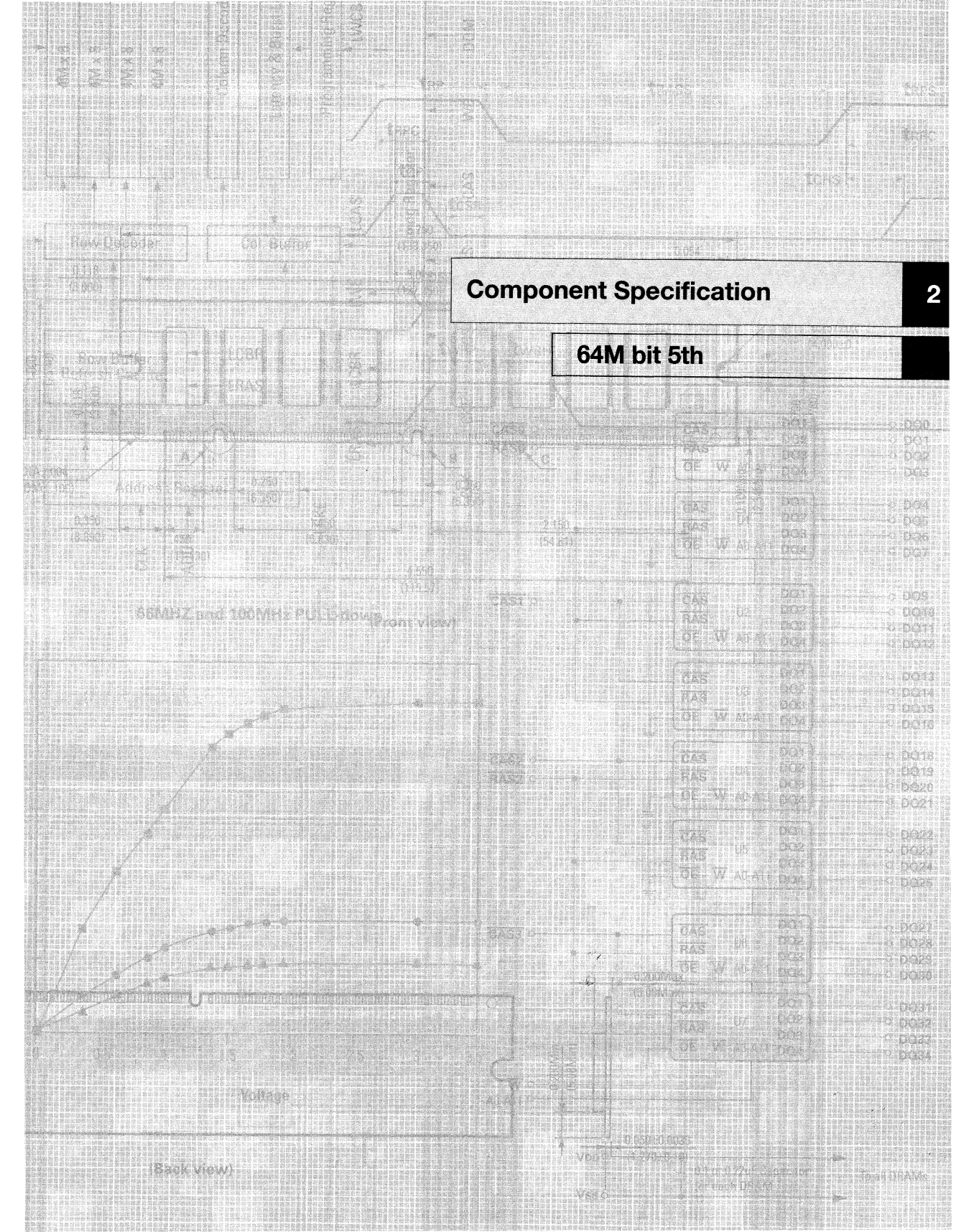
• Test Condition in DC CHARACTERISTIC Change Notice (64Mb D-die)

Symbol	Before	After
I_{CC2P}, I_{CC3P}	CKE ≤ V_{IL}(max), tCC = 15ns	CKE ≤ V_{IL}(max), tCC = 10ns
I_{CC2N}, I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tCC = 15ns Input signals are changed one time during 30ns	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tCC = 10ns Input signals are changed one time during 20ns
I_{CC4}	2 Banks activated	4 Banks activated

Component Specification

2

64M bit 5th



4M x 4Bit x 4 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS latency (2 & 3)
  - -. Burst length (1, 2, 4, 8 & Full page)
  - -. Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

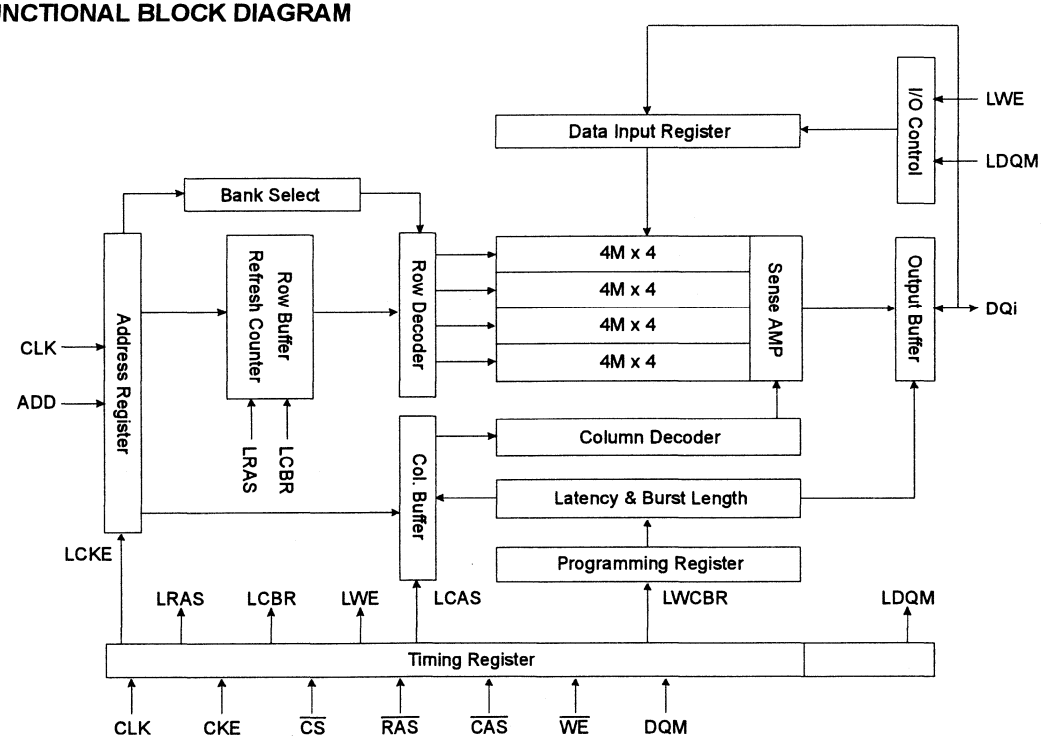
GENERAL DESCRIPTION

The K4S640432D is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 4,194,304 words by 4 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
K4S640432D-TC/L75	133MHz(CL=3)	LVTTL	54 TSOP(II)
K4S640432D-TC/L80	125MHz(CL=3)		
K4S640432D-TC/L1H	100MHz(CL=2)		
K4S640432D-TC/L1L	100MHz(CL=3)		
K4S640432D-TC/L10	66MHz(CL=2 &3)		

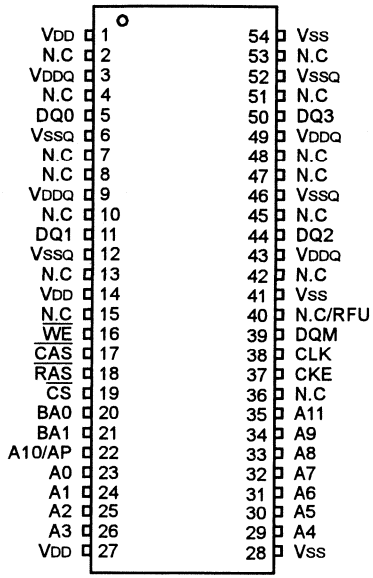
FUNCTIONAL BLOCK DIAGRAM



* Samsung Electronics reserves the right to change products or specification without notice.

SAMSUNG ELECTRONICS

PIN CONFIGURATION (Top view)



54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{11}	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{11}, Column address : CA_0 ~ CA_9
BA_0 ~ BA_1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.
$DQ_{0 \sim 3}$	*Data input/output*	Data Inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data output power/ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No connection /reserved for future use*	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ASOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC.The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	C_{CLK}	2.5	4.0	pF	1
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM	C_{IN}	2.5	5.0	pF	2
Address	C_{ADD}	2.5	5.0	pF	2
DQ_0 ~ DQ_3	C_{OUT}	4.0	6.5	pF	3

Notes : 1. -75 only specify a maximum value of 3.5pF
2. -75 only specify a maximum value of 3.8pF
3. -75 only specify a maximum value of 6.0pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

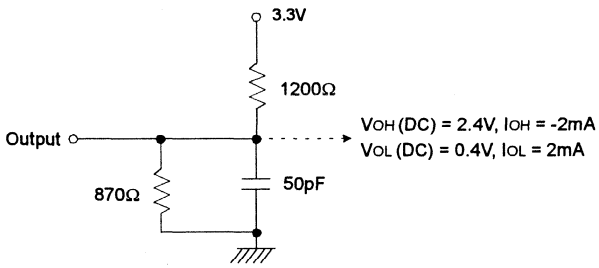
Parameter	Symbol	Test Condition		Version					Unit	Note
				-75	-80	-1H	-1L	-10		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA		70	70	65	65	65	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		1					mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		1						
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		15					mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		6						
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		3					mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		3						
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		25					mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		15						
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks Activated t_{CCD} = 2CLKs		100	95	80	80	80	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		135	135	125	125	125	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	C	1					mA	3
			L	400					uA	4

Notes : 1. Measured with outputs open.

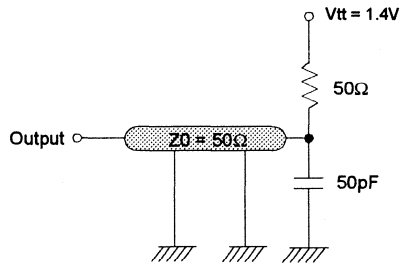
2. Refresh period is 64ms.
3. K4S640432D-TC**
4. K4S640432D-TL**
5. Unless otherwise noted, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ})

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version					Unit	Note
			-75	-80	-1H	-1L	-10		
Row active to row active delay		tRRD(min)	15	16	20	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	20	24	ns	1
Row precharge time		tRP(min)	20	20	20	20	24	ns	1
Row active time		tRAS(min)	45	48	50	50	50	ns	1
		tRAS(max)	100					us	
Row cycle time		tRC(min)	65	68	70	70	80	ns	1
Last data in to row precharge		tRDL(min)	2					CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns					-	5
Last data in to new col. address delay		tCDL(min)	1					CLK	2
Last data in to burst stop		tBDL(min)	1					CLK	2
Col. address to col. address delay		tCCD(min)	1					CLK	3
Number of valid output data	CAS latency=3		2					ea	4
	CAS latency=2		-		1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -80/1H/1L/10, tRDL=1CLK and tDAL=1CLK+20ns is also supported . SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-75		-80		-1H		-1L		-10		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	8	1000	10	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		-		10		12		13			
CLK to valid output delay	CAS latency=3	tSAC		5.4		6		6		6		7	ns	1,2
	CAS latency=2			-		-		6		7		7		
Output data hold time	CAS latency=3	tOH	2.7		3		3		3		3		ns	2
	CAS latency=2		-		-		3		3		3			
CLK high pulse width		tCH	2.5		3		3		3		3.5		ns	3
CLK low pulse width		tCL	2.5		3		3		3		3.5		ns	3
Input setup time		tSS	1.5		2		2		2		2.5		ns	3
Input hold time		tSH	0.8		1		1		1		1.5		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4		6		6		6		7	ns	
	CAS latency=2			-		-		6		7		7		

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

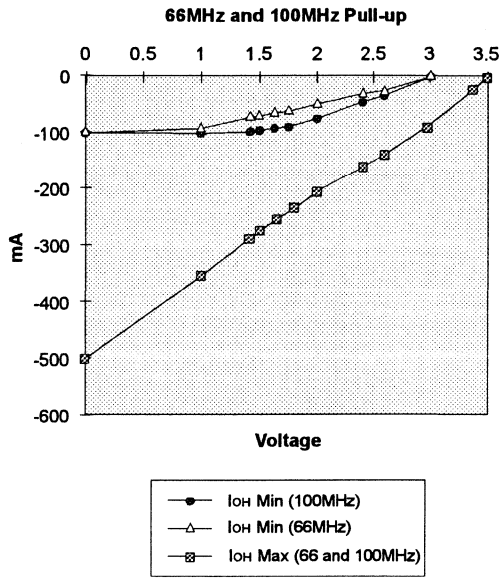
Parameter	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	1.37		4.37	Volts/ns	3
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	2.0	2.9	5.0	Volts/ns	1,2

Notes : 1. Rise time specification based on 0pF + 50 Ω to VSS, use these values to design to.
2. Fall time specification based on 0pF + 50 Ω to VDD, use these values to design to.
3. Measured into 50pF only, use these values to characterize to.
4. All measurements done with respect to VSS.

IBIS SPECIFICATION

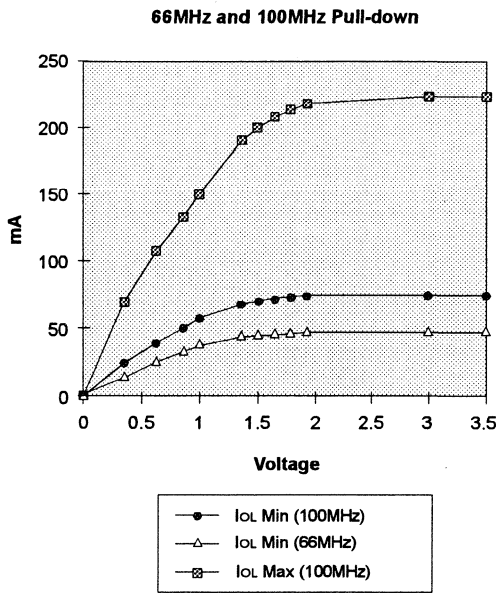
I_{OH} Characteristics (Pull-up)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
3.45		-2.4	
3.3		-27.3	
3.0	0.0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197.0	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73.0	-248.0	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0.0	-93.0	-502.4	-93.0



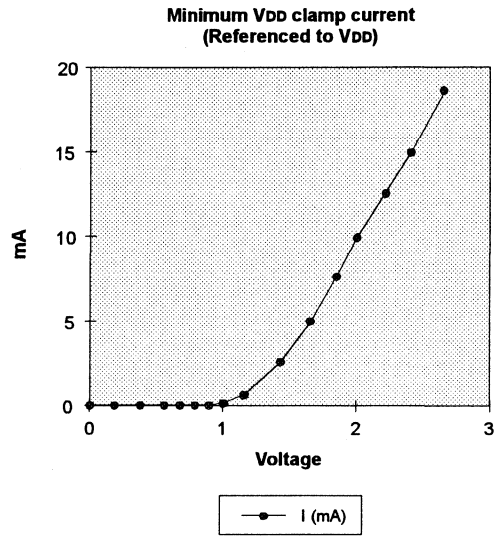
I_{OL} Characteristics (Pull-down)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
0.0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1.0	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3.0	80.3	219.6	54.2
3.45	81.4	222.6	54.9



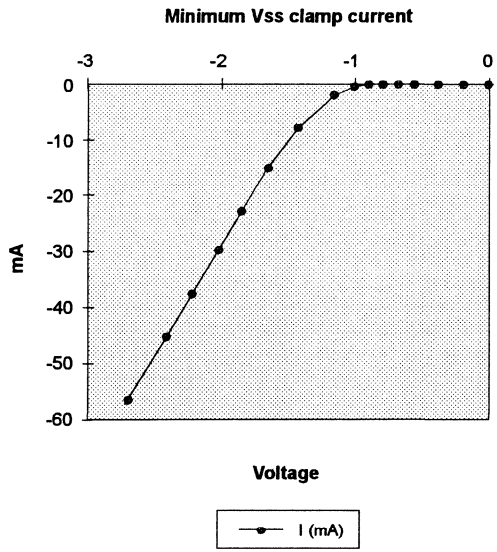
VDD Clamp @ CLK, CKE, $\overline{CS}$, DQM & DQ

VDD (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31



Vss Clamp @ CLK, CKE, $\overline{CS}$, DQM & DQ

Vss (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0



SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

2M x 8Bit x 4 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS latency (2 & 3)
  - -. Burst length (1, 2, 4, 8 & Full page)
  - -. Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K Cycle)

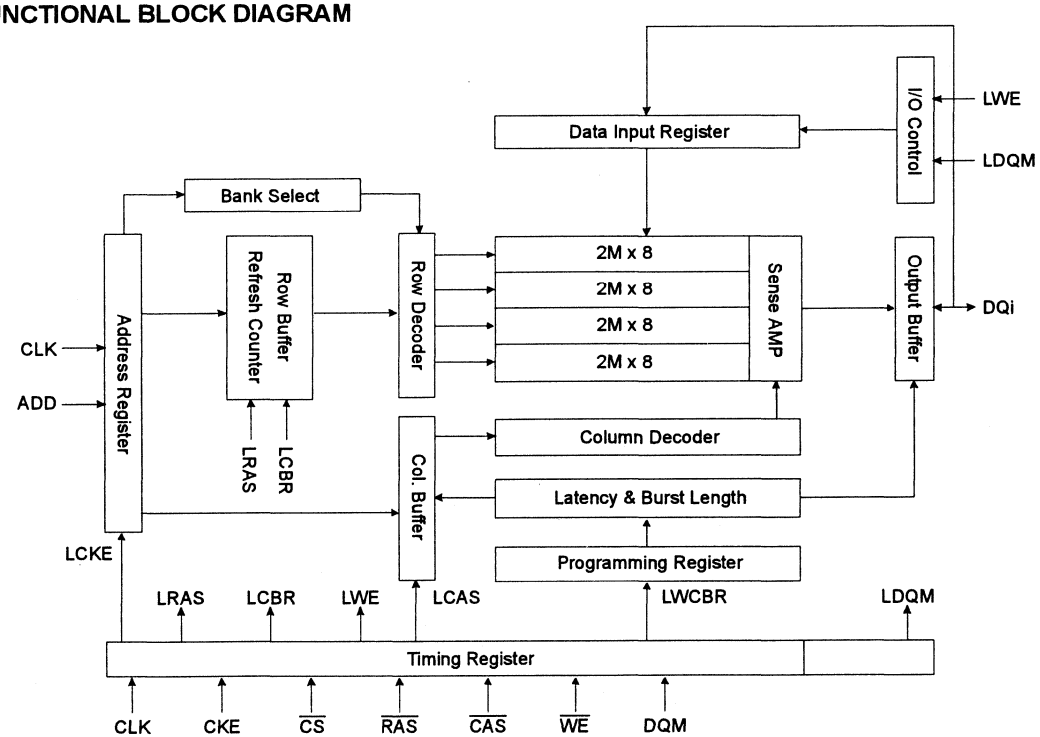
GENERAL DESCRIPTION

The K4S640832D is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 2,097,152 words by 8 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
K4S640832D-TC/L75	133MHz(CL=3)	LVTTL	54 TSOP(II)
K4S640832D-TC/L80	125MHz(CL=3)		
K4S640832D-TC/L1H	100MHz(CL=2)		
K4S640832D-TC/L1L	100MHz(CL=3)		
K4S640832D-TC/L10	66MHz(CL=2 &3)		

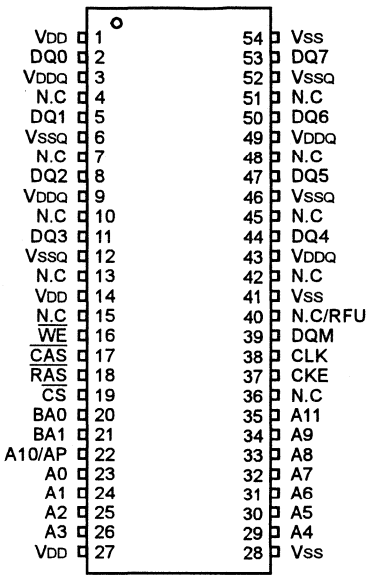
FUNCTIONAL BLOCK DIAGRAM



* Samsung Electronics reserves the right to change products or specification without notice.

SAMSUNG ELECTRONICS

PIN CONFIGURATION (Top view)



54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{11}	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{11}, Column address : CA_0 ~ CA_8
BA_0 ~ BA_1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.
DQ_0 ~ 7	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data output power/ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No connection /reserved for future use*	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input ieakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	C_{CLK}	2.5	4.0	pF	1
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM	C_{IN}	2.5	5.0	pF	2
Address	C_{ADD}	2.5	5.0	pF	2
DQ_0 ~ DQ_7	C_{OUT}	4.0	6.5	pF	3

Notes : 1. -75 only specify a maximum value of 3.5pF
2. -75 only specify a maximum value of 3.8pF
3. -75 only specify a maximum value of 6.0pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition		Version					Unit	Note
				-75	-80	-1H	-1L	-10		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA		75	75	70	70	70	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		1					mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		1						
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		15					mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		6						
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		3					mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		3						
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		25					mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		15						
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks Activated t_{CCD} = 2CLKs		115	110	95	95	95	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		135	130	125	125	125	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	C	1					mA	3
			L	400					uA	4

Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

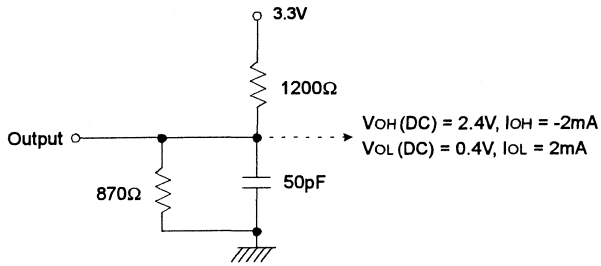
3. K4S640832D-TC**

4. K4S640832D-TL**

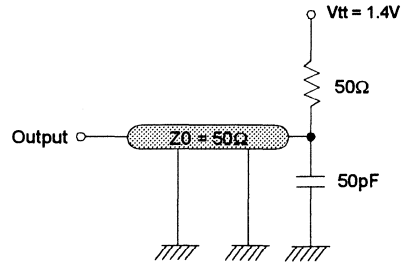
5. Unless otherwise noted, input swing level is CMOS(V_{IH} /V_{IL}=V_{DDQ}/V_{SSQ})

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version					Unit	Note
			-75	-80	-1H	-1L	-10		
Row active to row active delay		tRRD(min)	15	16	20	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	20	24	ns	1
Row precharge time		tRP(min)	20	20	20	20	24	ns	1
Row active time		tRAS(min)	45	48	50	50	50	ns	1
		tRAS(max)	100					us	
Row cycle time		tRC(min)	65	68	70	70	80	ns	1
Last data in to row precharge		tRDL(min)	2					CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns					-	5
Last data in to new col. address delay		tCDL(min)	1					CLK	2
Last data in to burst stop		tBDL(min)	1					CLK	2
Col. address to col. address delay		tCCD(min)	1					CLK	3
Number of valid output data	CAS latency=3		2					ea	4
	CAS latency=2		-		1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -80/1H/1L/10, tRDL=1CLK and tDAL=1CLK+20ns is also supported . SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-75		-80		-1H		-1L		-10		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	8	1000	10	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		-		10		12		13			
CLK to valid output delay	CAS latency=3	tSAC		5.4		6		6		6		7	ns	1,2
	CAS latency=2			-		-		6		7		7		
Output data hold time	CAS latency=3	tOH	2.7		3		3		3		3		ns	2
	CAS latency=2		-		-		3		3		3			
CLK high pulse width		tCH	2.5		3		3		3		3.5		ns	3
CLK low pulse width		tCL	2.5		3		3		3		3.5		ns	3
Input setup time		tSS	1.5		2		2		2		2.5		ns	3
Input hold time		tSH	0.8		1		1		1		1.5		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4		6		6		6		7	ns	
	CAS latency=2			-		-		6		7		7		

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

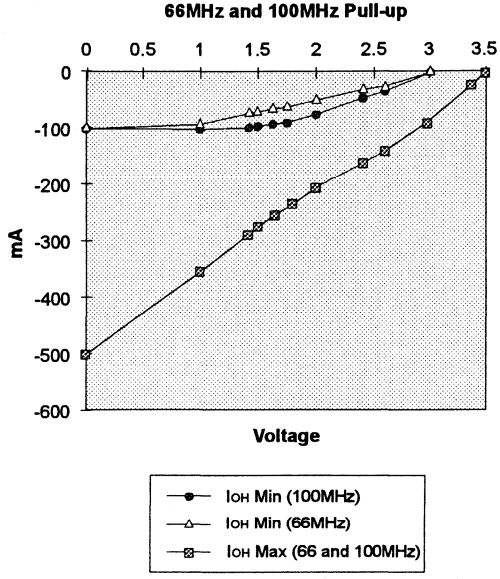
Parameter	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output rise time	trh	Measure in linear region : 1.2V ~1.8V	1.37		4.37	Volts/ns	3
Output fall time	tfh	Measure in linear region : 1.2V ~1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tfh	Measure in linear region : 1.2V ~1.8V	2.0	2.9	5.0	Volts/ns	1,2

Notes : 1. Rise time specification based on 0pF + 50 Ohms to VSS, use these values to design to.
2. Fall time specification based on 0pF + 50 Ohms to VDD, use these values to design to.
3. Measured into 50pF only, use these values to characterize to.
4. All measurements done with respect to VSS.

IBIS SPECIFICATION

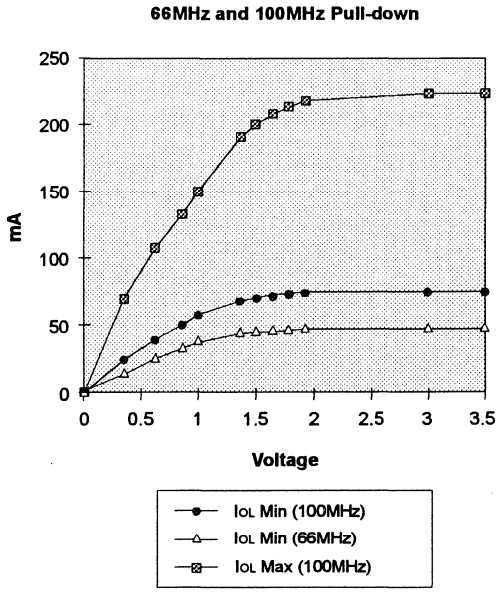
I_{OH} Characteristics (Pull-up)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
3.45		-2.4	
3.3		-27.3	
3.0	0.0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197.0	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73.0	-248.0	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0.0	-93.0	-502.4	-93.0



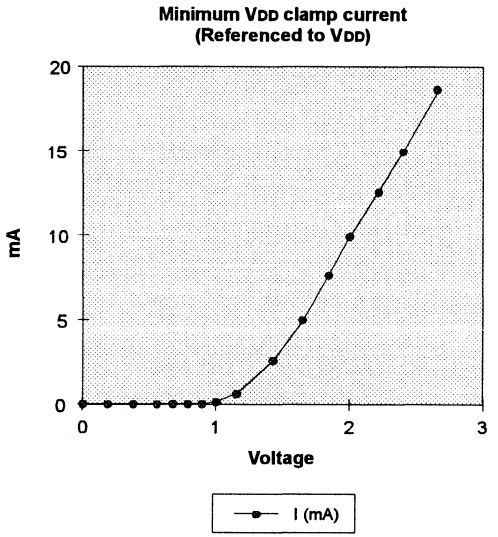
I_{OL} Characteristics (Pull-down)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3	80.3	219.6	54.2
3.45	81.4	222.6	54.9



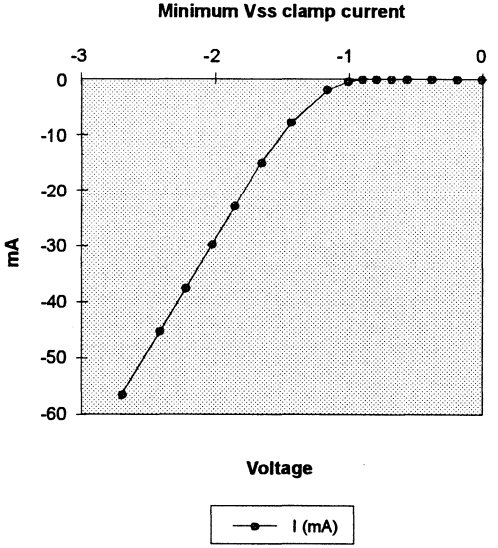
VDD Clamp @ CLK, CKE, $\overline{CS}$, DQM & DQ

VDD (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31



Vss Clamp @ CLK, CKE, $\overline{CS}$, DQM & DQ

Vss (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0



SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
		Entry		L									3
	Self refresh	Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A8)	4
	Auto precharge enable										H		4,5
Write & Column Address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A8)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

1M x 16Bit x 4 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS latency (2 & 3)
  - -. Burst length (1, 2, 4, 8 & Full page)
  - -. Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

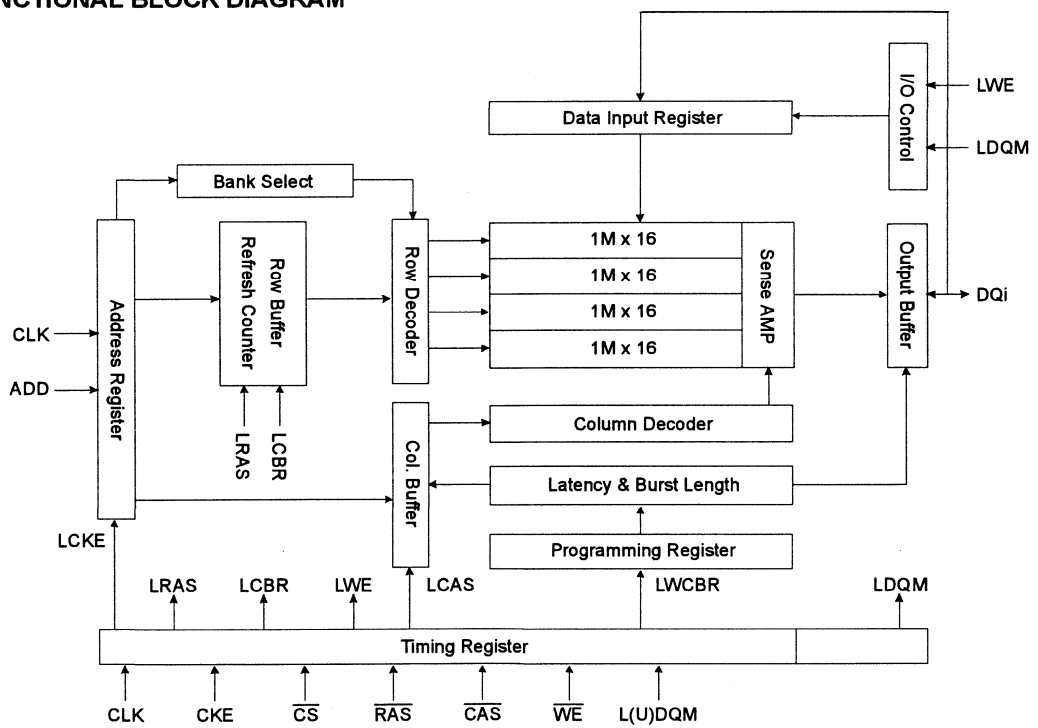
GENERAL DESCRIPTION

The K4S641632D is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 1,048,576 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
K4S641632D-TC/L75	133MHz(CL=3)	LVTTL	54 TSOP(II)
K4S641632D-TC/L80	125MHz(CL=3)		
K4S641632D-TC/L1H	100MHz(CL=2)		
K4S641632D-TC/L1L	100MHz(CL=3)		
K4S641632D-TC/L10	66MHz(CL=2 &3)		

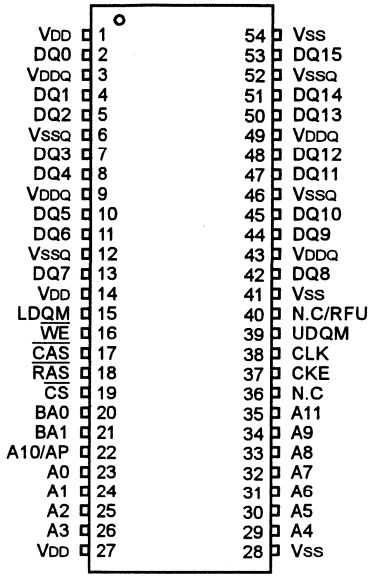
FUNCTIONAL BLOCK DIAGRAM



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SAMSUNG ELECTRONICS

PIN CONFIGURATION (Top view)



54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and L(U)DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{11}	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{11}, Column address : CA_0 ~ CA_7
BA_0 ~ BA_1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
L(U)DQM	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when L(U)DQM active.
$DQ_{0 \sim 15}$	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data output power/ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No connection /reserved for future use*	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	C_{CLK}	2.5	4.0	pF	1
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM	C_{IN}	2.5	5.0	pF	2
Address	C_{ADD}	2.5	5.0	pF	2
DQ_0 ~ DQ_{15}	C_{OUT}	4.0	6.5	pF	3

Notes : 1. -75 only specify a maximum value of 3.5pF
2. -75 only specify a maximum value of 3.8pF
3. -75 only specify a maximum value of 6.0pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition		Version					Unit	Note
				-75	-80	-1H	-1L	-10		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA		110	110	100	100	100	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		1					mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		1						
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		15					mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		6						
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		3					mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		3						
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		25					mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		15						
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks Activated t_{CCD} = 2CLKs		135	130	110	110	110	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		135	130	125	125	125	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	C	1					mA	3
			L	400					uA	4

Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

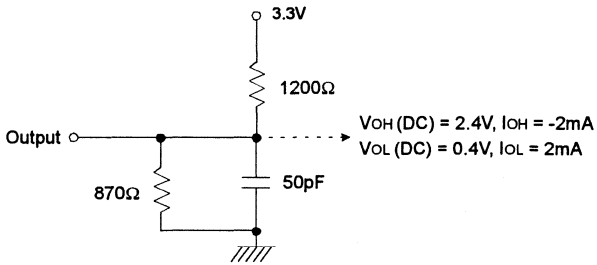
3. K4S641632D-TC**

4. K4S641632D-TL**

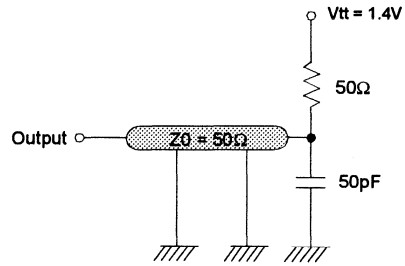
5. Unless otherwise noted, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ})

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version					Unit	Note
			-75	-80	-1H	-1L	-10		
Row active to row active delay		tRRD(min)	15	16	20	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	20	24	ns	1
Row precharge time		tRP(min)	20	20	20	20	24	ns	1
Row active time		tRAS(min)	45	48	50	50	50	ns	1
		tRAS(max)	100					us	
Row cycle time		tRC(min)	65	68	70	70	80	ns	1
Last data in to row precharge		tRDL(min)	2					CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns					-	5
Last data in to new col. address delay		tCDL(min)	1					CLK	2
Last data in to burst stop		tBDL(min)	1					CLK	2
Col. address to col. address delay		tCCD(min)	1					CLK	3
Number of valid output data	CAS latency=3		2					ea	4
	CAS latency=2		-		1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -80/1H/1L/10, tRDL=1CLK and tDAL=1CLK+20ns is also supported . SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-75		-80		-1H		-1L		-10		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	8	1000	10	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		-		10		12		13			
CLK to valid output delay	CAS latency=3	tSAC		5.4		6		6		6		7	ns	1,2
	CAS latency=2			-		-		6		7		7		
Output data hold time	CAS latency=3	tOH	2.7		3		3		3		3		ns	2
	CAS latency=2		-		-		3		3		3			
CLK high pulse width		tCH	2.5		3		3		3		3.5		ns	3
CLK low pulse width		tCL	2.5		3		3		3		3.5		ns	3
Input setup time		tSS	1.5		2		2		2		2.5		ns	3
Input hold time		tSH	0.8		1		1		1		1.5		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4		6		6		6		7	ns	
	CAS latency=2			-		-		6		7		7		

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	1.37		4.37	Volts/ns	3
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	2.0	2.9	5.0	Volts/ns	1,2

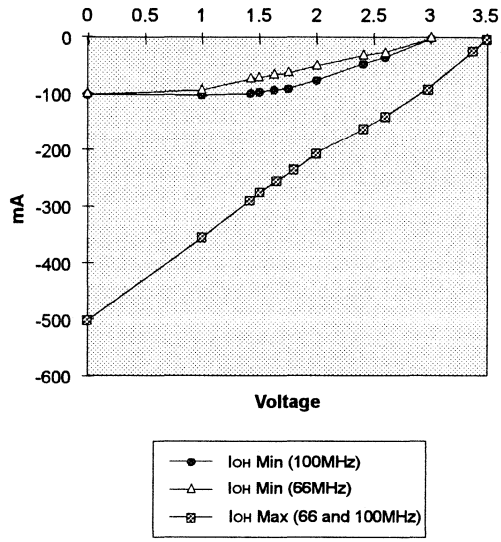
Notes : 1. Rise time specification based on 0pF + 50 Ω to VSS, use these values to design to.
2. Fall time specification based on 0pF + 50 Ω to VDD, use these values to design to.
3. Measured into 50pF only, use these values to characterize to.
4. All measurements done with respect to VSS.

IBIS SPECIFICATION

I_{OH} Characteristics (Pull-up)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
3.45		-2.4	
3.3		-27.3	
3.0	0.0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197.0	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73.0	-248.0	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0.0	-93.0	-502.4	-93.0

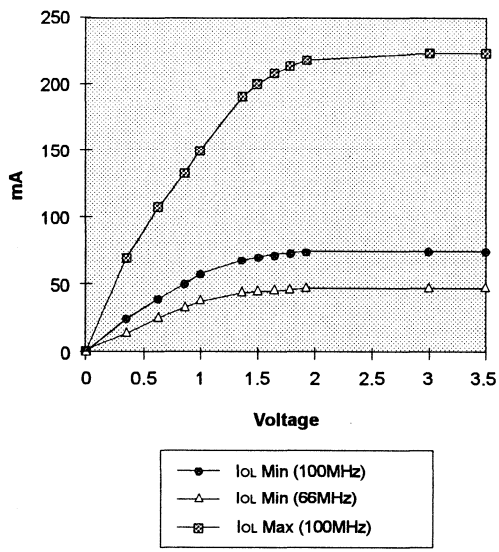
66MHz and 100MHz Pull-up



I_{OL} Characteristics (Pull-down)

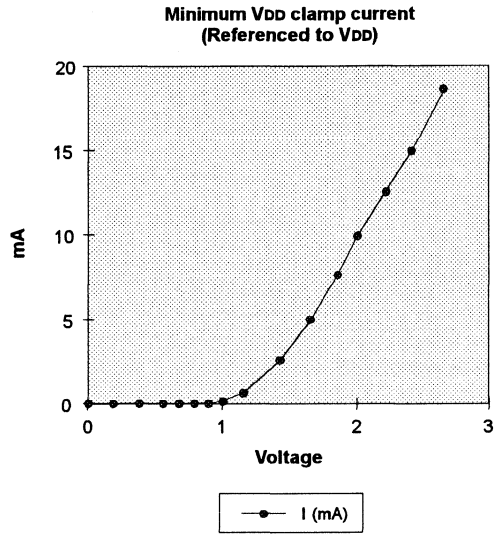
Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
0.0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1.0	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3.0	80.3	219.6	54.2
3.45	81.4	222.6	54.9

66MHz and 100MHz Pull-down



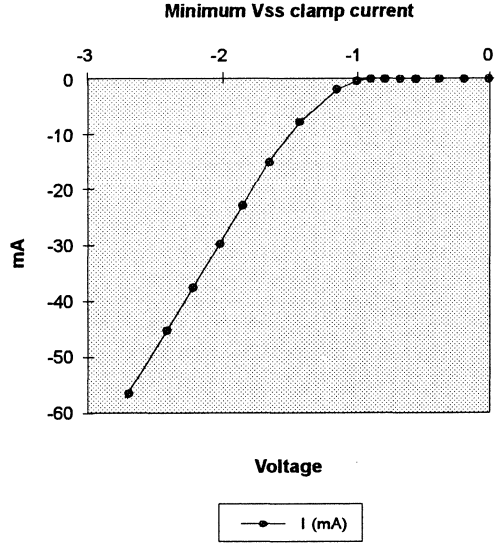
VDD Clamp @ CLK, CKE, $\overline{CS}$, DQM & DQ

VDD (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31



Vss Clamp @ CLK, CKE, $\overline{CS}$, DQM & DQ

Vss (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0



SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A7)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A7)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

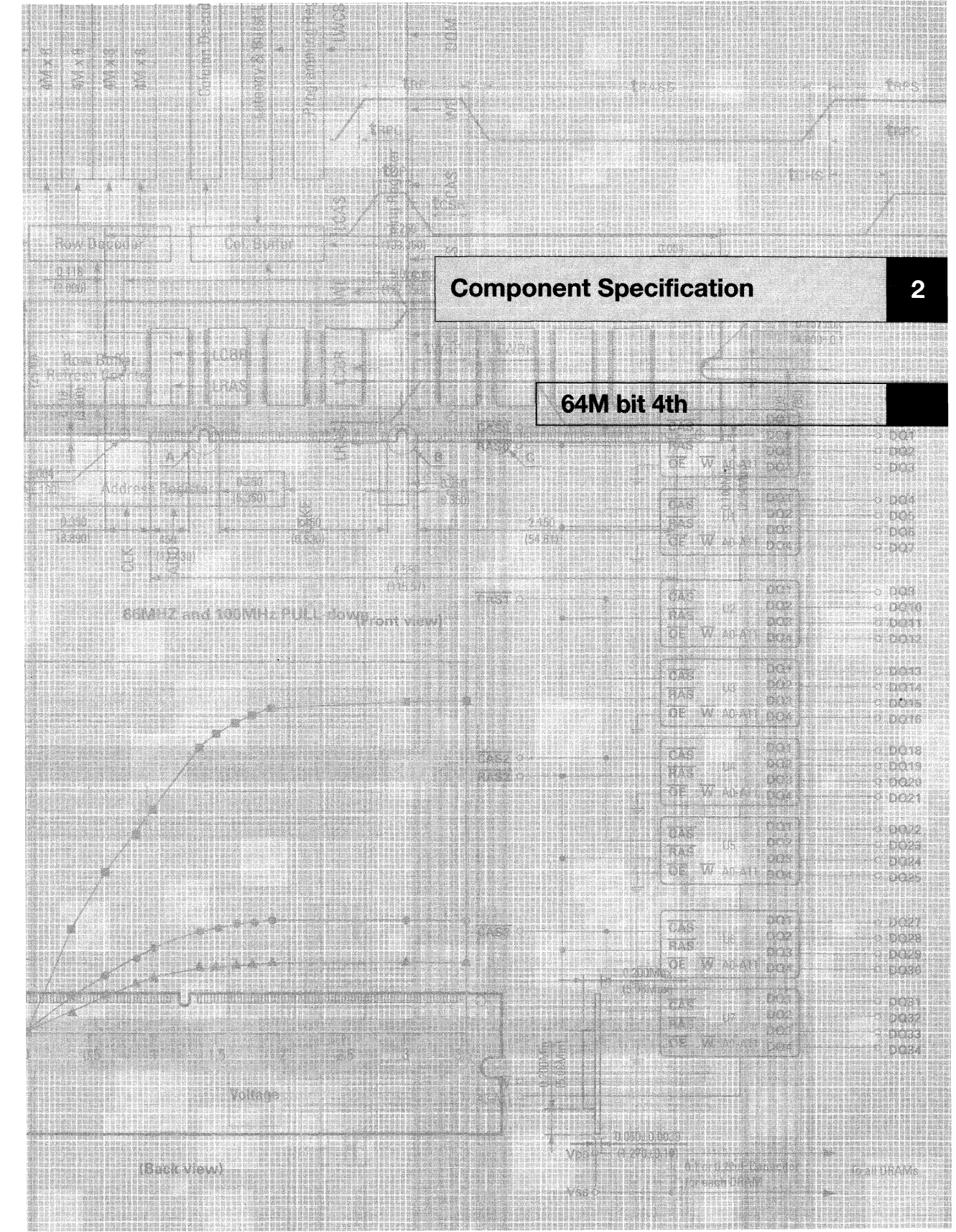
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

NOTES

Component Specification

2

64M bit 4th



4M x 4Bit x 4 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS latency (2 & 3)
  - -. Burst length (1, 2, 4, 8 & Full page)
  - -. Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

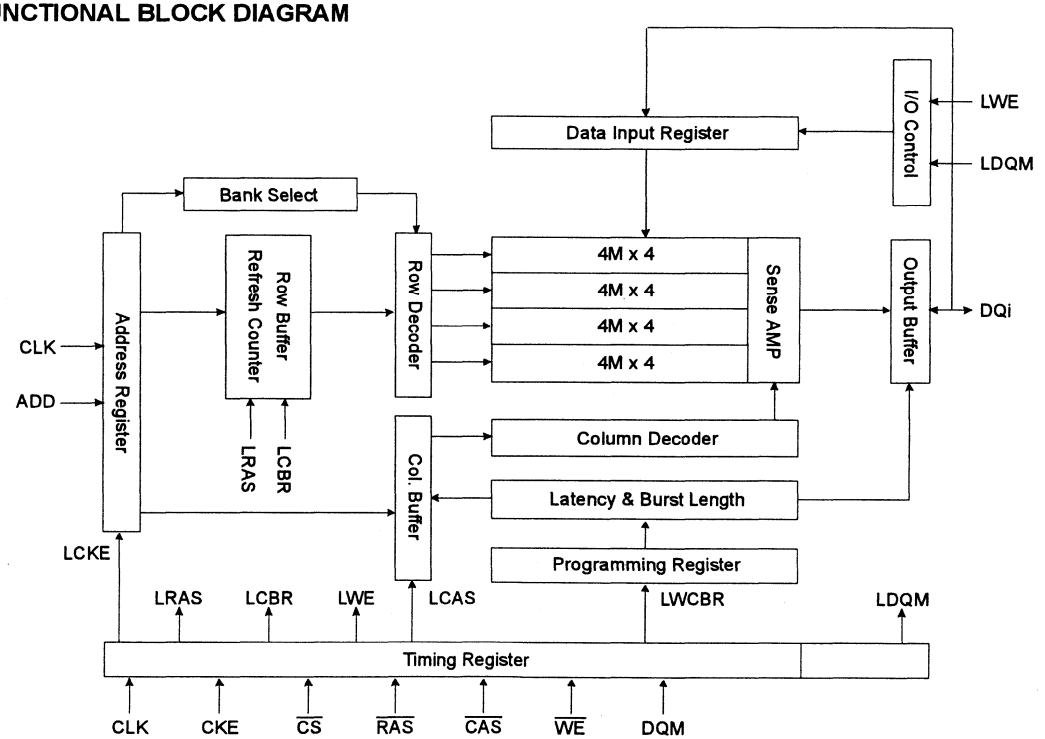
GENERAL DESCRIPTION

The K4S640432C is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 4,194,304 words by 4 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
K4S640432C-TC/L75	133MHz(CL=3)	LVTTL	54 TSOP(II)
K4S640432C-TC/L80	125MHz(CL=3)		
K4S640432C-TC/L1H	100MHz(CL=2)		
K4S640432C-TC/L1L	100MHz(CL=3)		
K4S640432C-TC/L10	66MHz(CL=2&3)		

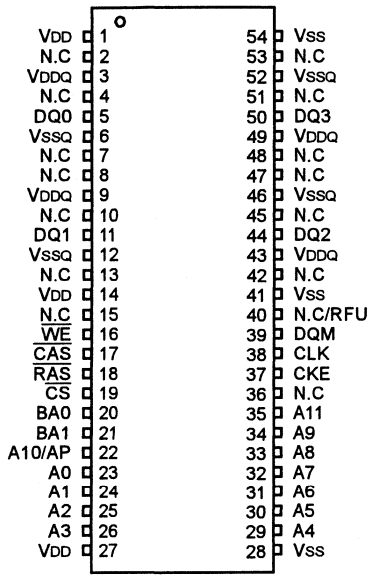
FUNCTIONAL BLOCK DIAGRAM



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SAMSUNG ELECTRONICS

PIN CONFIGURATION (Top view)



54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{11}	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{11}, Column address : CA_0 ~ CA_9
BA_0 ~ BA_1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.
DQ_0 ~ 3	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data output power/ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No connection /reserved for future use*	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ASOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-1	-	1	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC.The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Clock	C_{CLK}	2.5	4.0	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM	C_{IN}	2.5	5.0	pF
Address	C_{ADD}	2.5	5.0	pF
DQ_0 ~ DQ_3	C_{OUT}	4.0	6.5	pF

DC CHARACTERISTICS

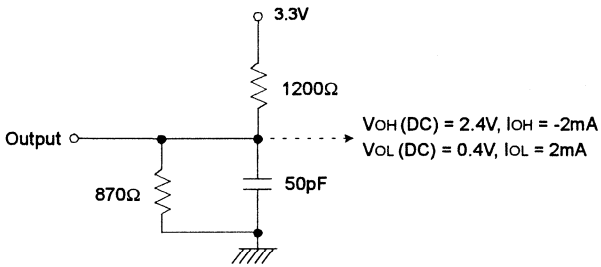
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version					Unit	Note
				-75	-80	-1H	-1L	-10		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		70	70	65	65	60	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		1					mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		1						
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		12					mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		6						
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		2					mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		2						
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		20					mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		10					mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	95	80	65	65	65	mA	1
			2	65	65	65	60	60		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		125				110	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	C	1					mA	3
			L	450					uA	4

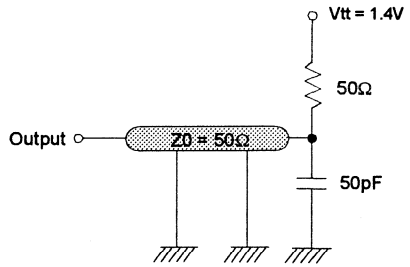
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. K4S640432C-TC**
4. K4S640432C-TL**

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version					Unit	Note
			-75	-80	-1H	-1L	-10		
Row active to row active delay		tRRD(min)	14	16	20	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	20	24	ns	1
Row precharge time		tRP(min)	20	20	20	20	24	ns	1
Row active time		tRAS(min)	48	48	50	50	50	ns	1
		tRAS(max)	100					us	
Row cycle time		tRC(min)	68	68	70	70	80	ns	1
Last data in to row precharge		tRDL(min)	7	8	10	10	12	ns	2
Last data in to new col. address delay		tCDL(min)	1					CLK	2
Last data in to burst stop		tBDL(min)	1					CLK	2
Col. address to col. address delay		tCCD(min)	1					CLK	3
Number of valid output data	CAS latency=3		2					ea	4
	CAS latency=2		1						

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-75		-80		-1H		-1L		-10		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	7	1000	8	1000	10	1000	10	1000	10	1000	ns	1
	CAS latency=2		10		10		10		12		13			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6		6		7	ns	1,2
	CAS latency=2			6		6		6		7		7		
Output data hold time	CAS latency=3	tOH	3		3		3		3		3		ns	2
	CAS latency=2		3		3		3		3		3			
CLK high pulse width		tCH	3		3		3		3		3.5		ns	3
CLK low pulse width		tCL	3		3		3		3		3.5		ns	3
Input setup time		tSS	2		2		2		2		2.5		ns	3
Input hold time		tSH	1		1		1		1		1.5		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6		6		7	ns	
	CAS latency=2			6		6		6		7		7		

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	1.37		4.37	Volts/ns	3
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	2.0	2.9	5.0	Volts/ns	1,2

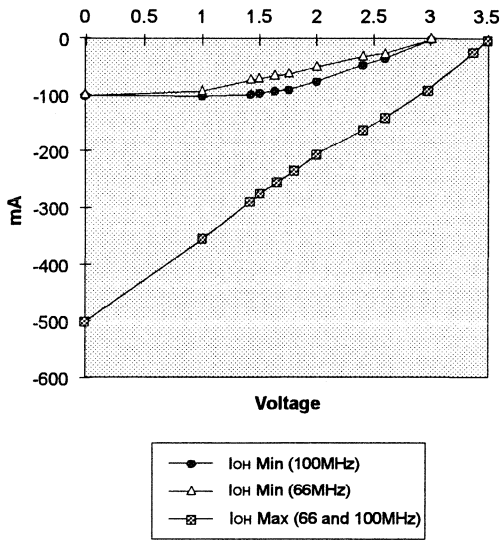
Notes : 1. Rise time specification based on 0pF + 50 Ω to VSS, use these values to design to.
2. Fall time specification based on 0pF + 50 Ω to VDD, use these values to design to.
3. Measured into 50pF only, use these values to characterize to.
4. All measurements done with respect to VSS.

IBIS SPECIFICATION

I_{OH} Characteristics (Pull-up)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
3.45		-2.4	
3.3		-27.3	
3.0	0.0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197.0	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73.0	-248.0	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0.0	-93.0	-502.4	-93.0

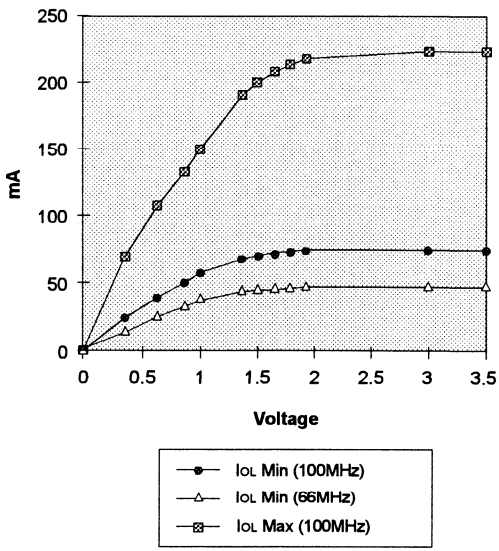
66MHz and 100MHz Pull-up



I_{OL} Characteristics (Pull-down)

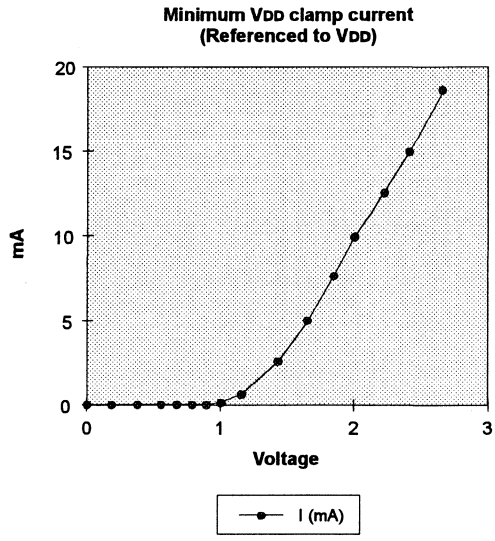
Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
0.0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1.0	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3.0	80.3	219.6	54.2
3.45	81.4	222.6	54.9

66MHz and 100MHz Pull-down



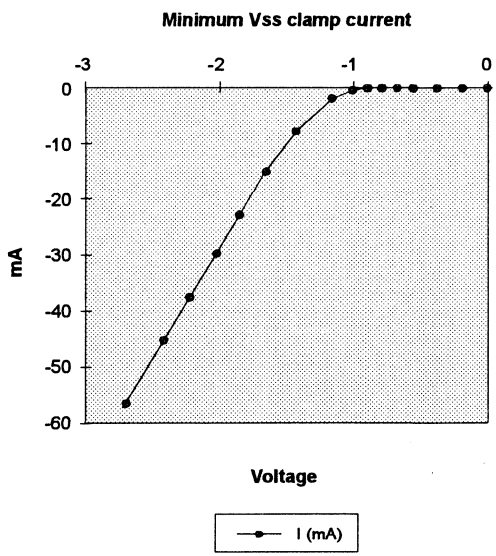
VDD Clamp @ CLK, CKE, $\overline{CS}$, DQM & DQ

VDD (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31



Vss Clamp @ CLK, CKE, $\overline{CS}$, DQM & DQ

Vss (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0



SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

2M x 8Bit x 4 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS latency (2 & 3)
  - -. Burst length (1, 2, 4, 8 & Full page)
  - -. Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K Cycle)

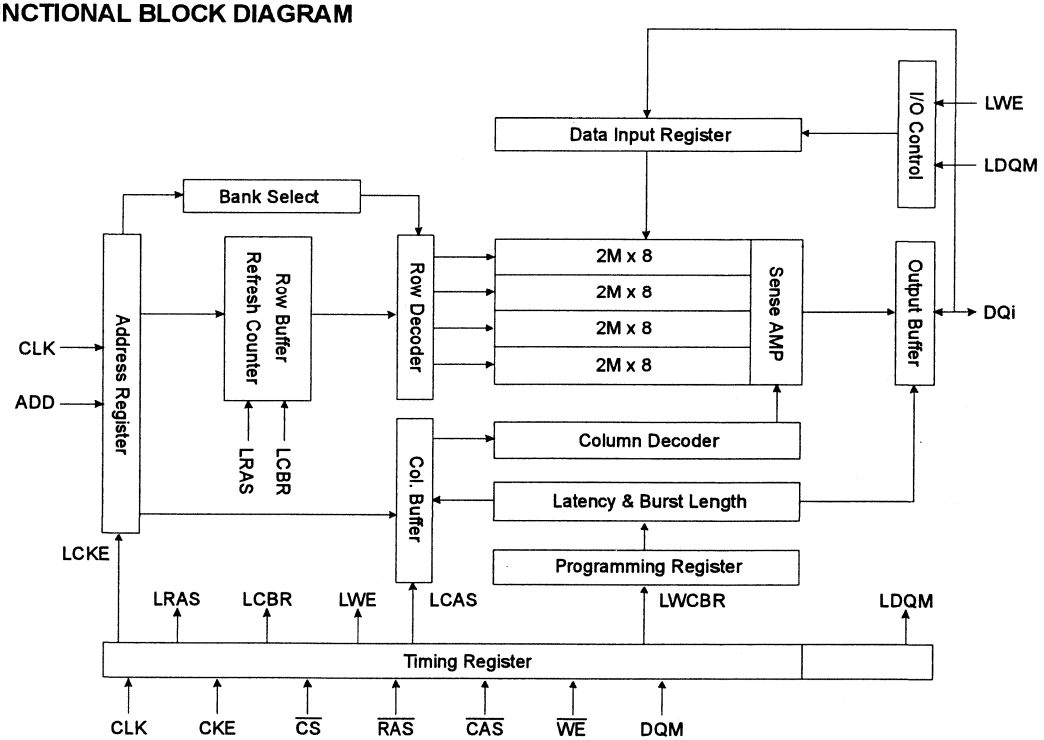
GENERAL DESCRIPTION

The K4S640832C is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 2,097,152 words by 8 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

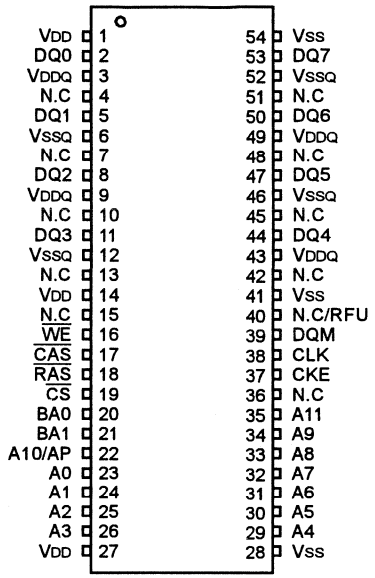
Part No.	Max Freq.	Interface	Package
K4S640832C-TC/L75	133MHz(CL=3)	LVTTL	54 TSOP(II)
K4S640832C-TC/L80	125MHz(CL=3)		
K4S640832C-TC/L1H	100MHz(CL=2)		
K4S640832C-TC/L1L	100MHz(CL=3)		
K4S640832C-TC/L10	66MHz(CL=2&3)		

FUNCTIONAL BLOCK DIAGRAM



* Samsung Electronics reserves the right to change products or specification without notice.

PIN CONFIGURATION (Top view)



54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{11}	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{11}, Column address : CA_0 ~ CA_8
BA_0 ~ BA_1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.
$DQ_{0 \sim 7}$	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data output power/ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No connection /reserved for future use*	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-1	-	1	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Clock	C_{CLK}	2.5	4.0	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM	C_{IN}	2.5	5.0	pF
Address	C_{ADD}	2.5	5.0	pF
DQ_0 ~ DQ_7	C_{OUT}	4.0	6.5	pF

DC CHARACTERISTICS

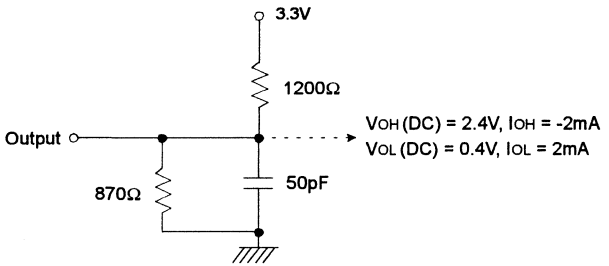
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version					Unit	Note
				-75	-80	-1H	-1L	-10		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		75	75	70	70	65	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		1					mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		1						
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		12					mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		6						
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		2					mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		2						
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		20					mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		10					mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	110	95	75	75	75	mA	1
			2	75	75	75	70	70		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		125				110	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	C	1					mA	3
			L	450					uA	4

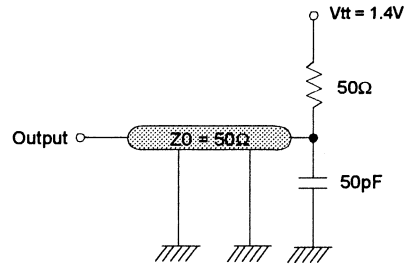
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. K4S640832C-TC**
4. K4S640832C-TL**

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version					Unit	Note
			-75	-80	-1H	-1L	-10		
Row active to row active delay		tRRD(min)	14	16	20	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	20	24	ns	1
Row precharge time		tRP(min)	20	20	20	20	24	ns	1
Row active time		tRAS(min)	48	48	50	50	50	ns	1
		tRAS(max)	100					us	
Row cycle time		tRC(min)	68	68	70	70	80	ns	1
Last data in to row precharge		tRDL(min)	7	8	10	10	12	ns	2
Last data in to new col. address Delay		tCDL(min)	1					CLK	2
Last data in to burst stop		tBDL(min)	1					CLK	2
Col. address to col. address delay		tCCD(min)	1					CLK	3
Number of valid output data	CAS latency=3		2					ea	4
	CAS latency=2		1						

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-75		-80		-1H		-1L		-10		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	7	1000	8	1000	10	1000	10	1000	10	1000	ns	1
	CAS latency=2		10		10		10		12		13			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6		6		7	ns	1,2
	CAS latency=2			6		6		6		7		7		
Output data hold time	CAS latency=3	tOH	3		3		3		3		3		ns	2
	CAS latency=2		3		3		3		3		3			
CLK high pulse width		tCH	3		3		3		3		3.5		ns	3
CLK low pulse width		tCL	3		3		3		3		3.5		ns	3
Input setup time		tSS	2		2		2		2		2.5		ns	3
Input hold time		tSH	1		1		1		1		1.5		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6		6		7	ns	
	CAS latency=2			6		6		6		7		7		

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

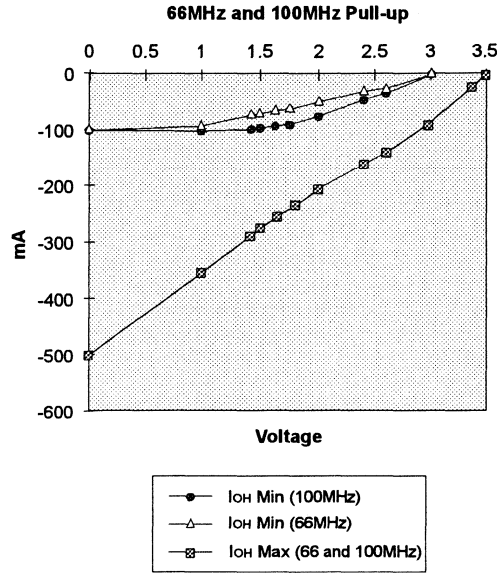
Parameter	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output rise time	trh	Measure in linear region : 1.2V ~1.8V	1.37		4.37	Volts/ns	3
Output fall time	tfh	Measure in linear region : 1.2V ~1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tfh	Measure in linear region : 1.2V ~1.8V	2.0	2.9	5.0	Volts/ns	1,2

Notes : 1. Rise time specification based on 0pF + 50 Ohms to VSS, use these values to design to.
2. Fall time specification based on 0pF + 50 Ohms to VDD, use these values to design to.
3. Measured into 50pF only, use these values to characterize to.
4. All measurements done with respect to VSS.

IBIS SPECIFICATION

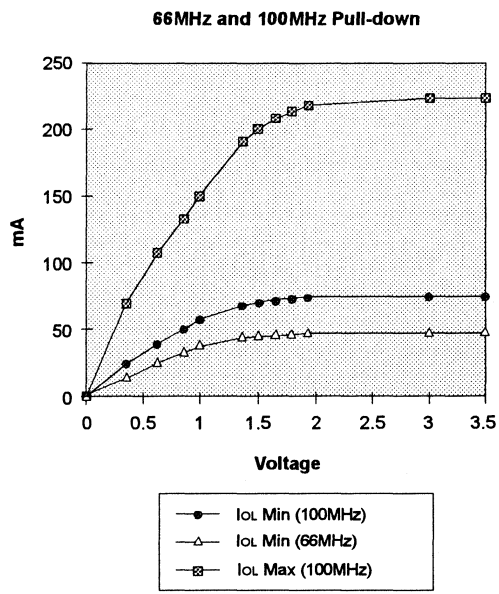
I_{OH} Characteristics (Pull-up)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
3.45		-2.4	
3.3		-27.3	
3.0	0.0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197.0	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73.0	-248.0	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0.0	-93.0	-502.4	-93.0



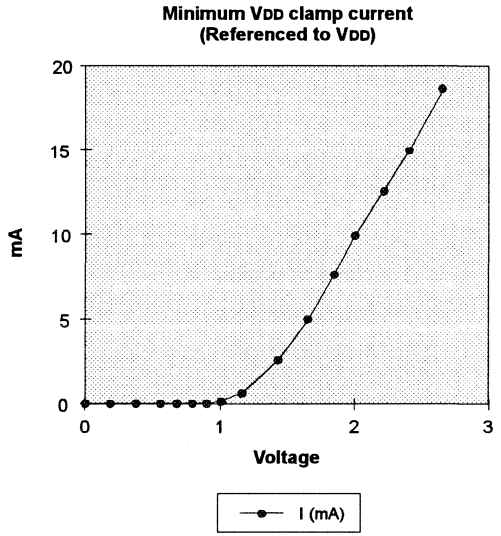
I_{OL} Characteristics (Pull-down)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3	80.3	219.6	54.2
3.45	81.4	222.6	54.9



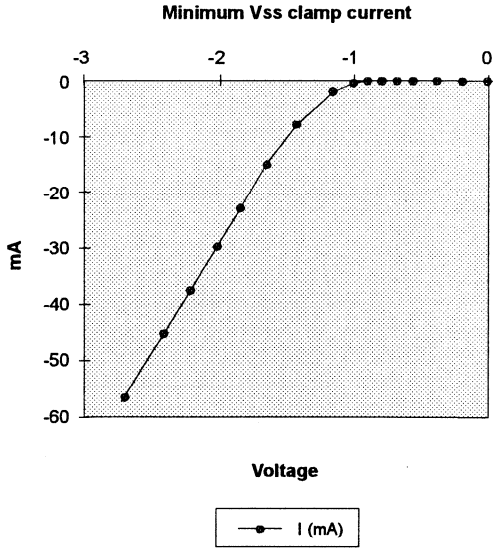
V_{DD} Clamp @ CLK, CKE, $\overline{CS}$, DQM & DQ

V_{DD} (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31



Vss Clamp @ CLK, CKE, $\overline{CS}$, DQM & DQ

Vss (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0



SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_9 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & Column Address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_9 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

1M x 16Bit x 4 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS latency (2 & 3)
  - -. Burst length (1, 2, 4, 8 & Full page)
  - -. Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

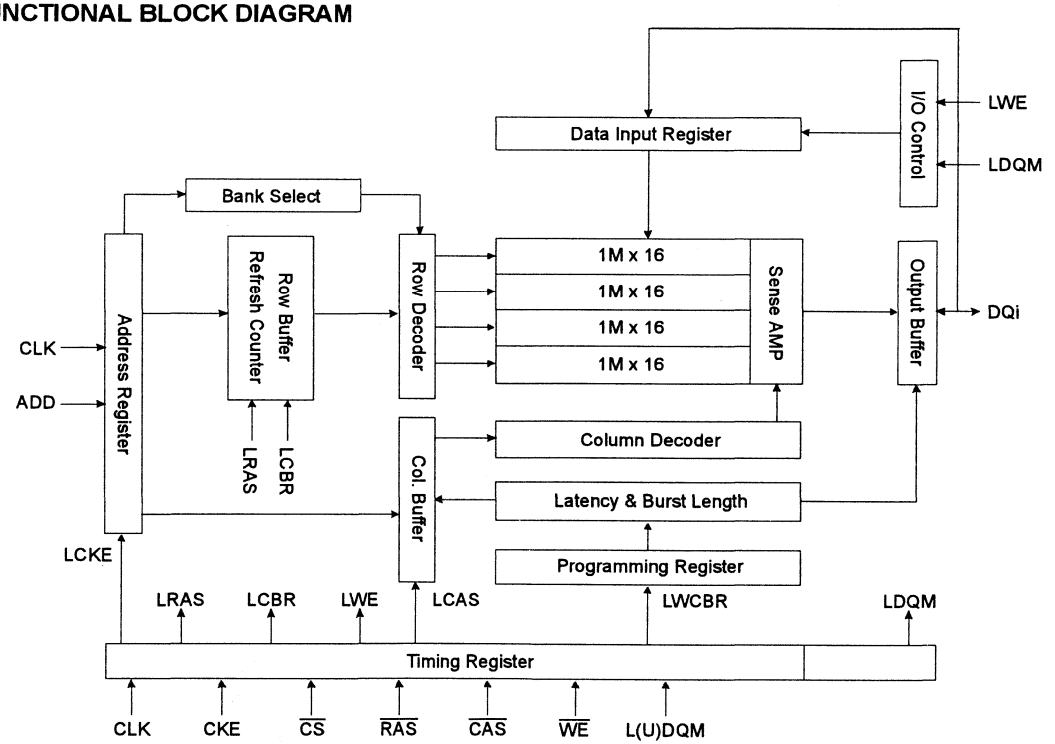
GENERAL DESCRIPTION

The K4S641632C is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 1,048,576 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

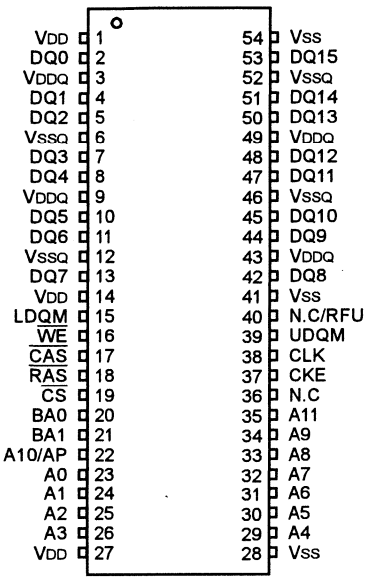
Part No.	Max Freq.	Interface	Package
K4S641632C-TC/L75	133MHz(CL=3)	LVTTL	54 TSOP(II)
K4S641632C-TC/L80	125MHz(CL=3)		
K4S641632C-TC/L1H	100MHz(CL=2)		
K4S641632C-TC/L1L	100MHz(CL=3)		
K4S641632C-TC/L10	66MHz(CL=2&3)		

FUNCTIONAL BLOCK DIAGRAM



* Samsung Electronics reserves the right to change products or specification without notice.

PIN CONFIGURATION (Top view)



54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and L(U)DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{11}	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{11}, Column address : CA_0 ~ CA_7
BA_0 ~ BA_1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
L(U)DQM	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when L(U)DQM active.
$DQ_{0 \sim 15}$	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data output power/ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No connection /reserved for future use*	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-1	-	1	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Clock	C_{CLK}	2.5	4.0	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, L(U)DQM	C_{IN}	2.5	5.0	pF
Address	C_{ADD}	2.5	5.0	pF
DQ_0 ~ DQ_{15}	C_{OUT}	4.0	6.5	pF

DC CHARACTERISTICS

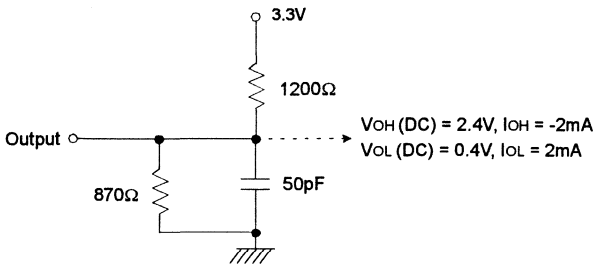
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version					Unit	Note
				-75	-80	-1H	-1L	-10		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		75	75	70	70	65	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		1					mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		1						
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		12					mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		6						
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		2					mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		2						
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		20					mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		10					mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	130	115	90	90	90	mA	1
			2	90	90	90	85	85		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		125				110	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	C	1					mA	3
			L	450					uA	4

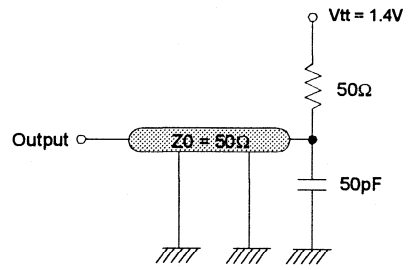
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. K4S641632C-TC**
4. K4S641632C-TL**

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version					Unit	Note
			-75	-80	-1H	-1L	-10		
Row active to row active delay		tRRD(min)	14	16	20	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	20	24	ns	1
Row precharge time		tRP(min)	20	20	20	20	24	ns	1
Row active time		tRAS(min)	48	48	50	50	50	ns	1
		tRAS(max)	100					us	
Row cycle time		tRC(min)	68	68	70	70	80	ns	1
Last data in to row precharge		tRDL(min)	7	8	10	10	12	ns	2
Last data in to new col. address Delay		tCDL(min)	1					CLK	2
Last data in to burst stop		tBDL(min)	1					CLK	2
Col. address to col. address delay		tCCD(min)	1					CLK	3
Number of valid output data	CAS latency=3		2					ea	4
	CAS latency=2		1						

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-75		-80		-1H		-1L		-10		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	7	1000	8	1000	10	1000	10	1000	10	1000	ns	1
	CAS latency=2		10		10		10		12		13			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6		6		7	ns	1,2
	CAS latency=2			6		6		6		7		7		
Output data hold time	CAS latency=3	tOH	3		3		3		3		3		ns	2
	CAS latency=2		3		3		3		3		3			
CLK high pulse width		tCH	3		3		3		3		3.5		ns	3
CLK low pulse width		tCL	3		3		3		3		3.5		ns	3
Input setup time		tSS	2		2		2		2		2.5		ns	3
Input hold time		tSH	1		1		1		1		1.5		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6		6		7	ns	
	CAS latency=2			6		6		6		7		7		

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	1.37		4.37	Volts/ns	3
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	2.0	2.9	5.0	Volts/ns	1,2

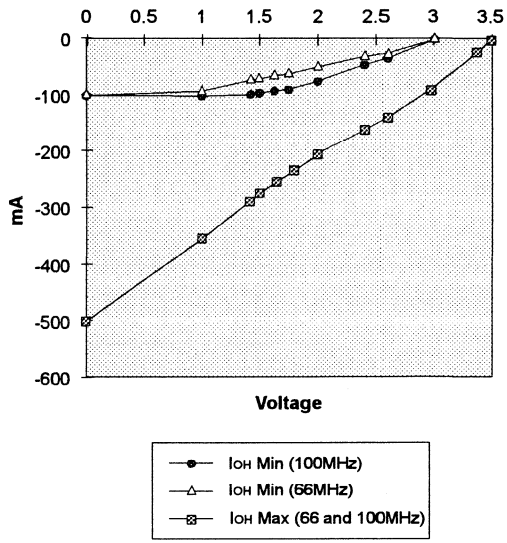
Notes : 1. Rise time specification based on 0pF + 50 Ω to VSS, use these values to design to.
2. Fall time specification based on 0pF + 50 Ω to VDD, use these values to design to.
3. Measured into 50pF only, use these values to characterize to.
4. All measurements done with respect to VSS.

IBIS SPECIFICATION

I_{OH} Characteristics (Pull-up)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
3.45		-2.4	
3.3		-27.3	
3.0	0.0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197.0	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73.0	-248.0	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0.0	-93.0	-502.4	-93.0

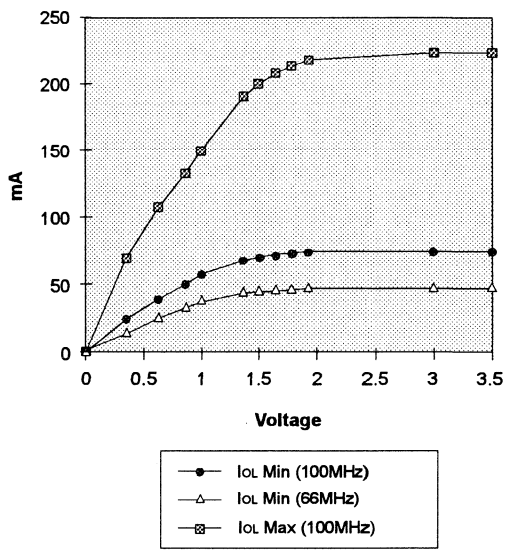
66MHz and 100MHz Pull-up



I_{OL} Characteristics (Pull-down)

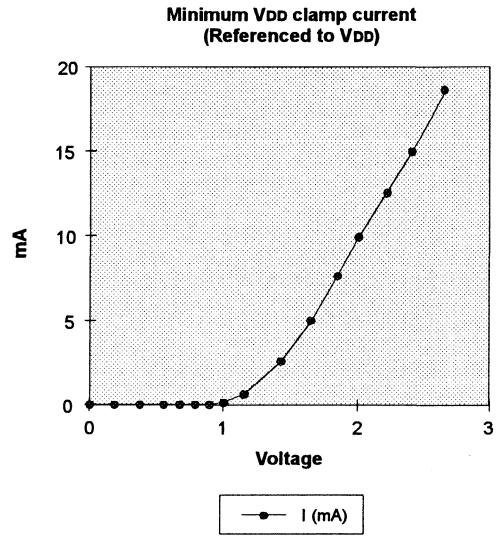
Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
0.0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1.0	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3.0	80.3	219.6	54.2
3.45	81.4	222.6	54.9

66MHz and 100MHz Pull-down



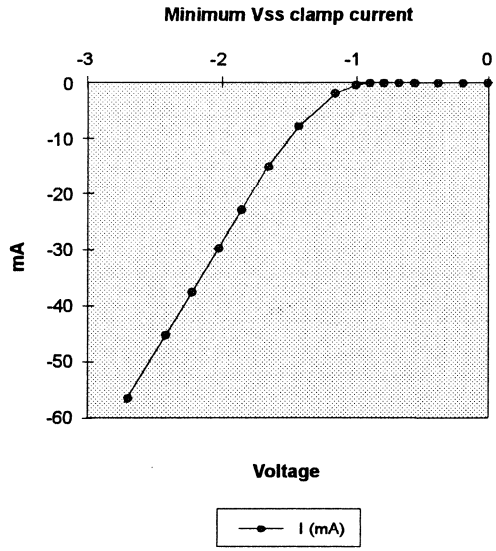
VDD Clamp @ CLK, CKE, $\overline{CS}$, DQM & DQ

VDD (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31



Vss Clamp @ CLK, CKE, $\overline{CS}$, DQM & DQ

VSS (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0



SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

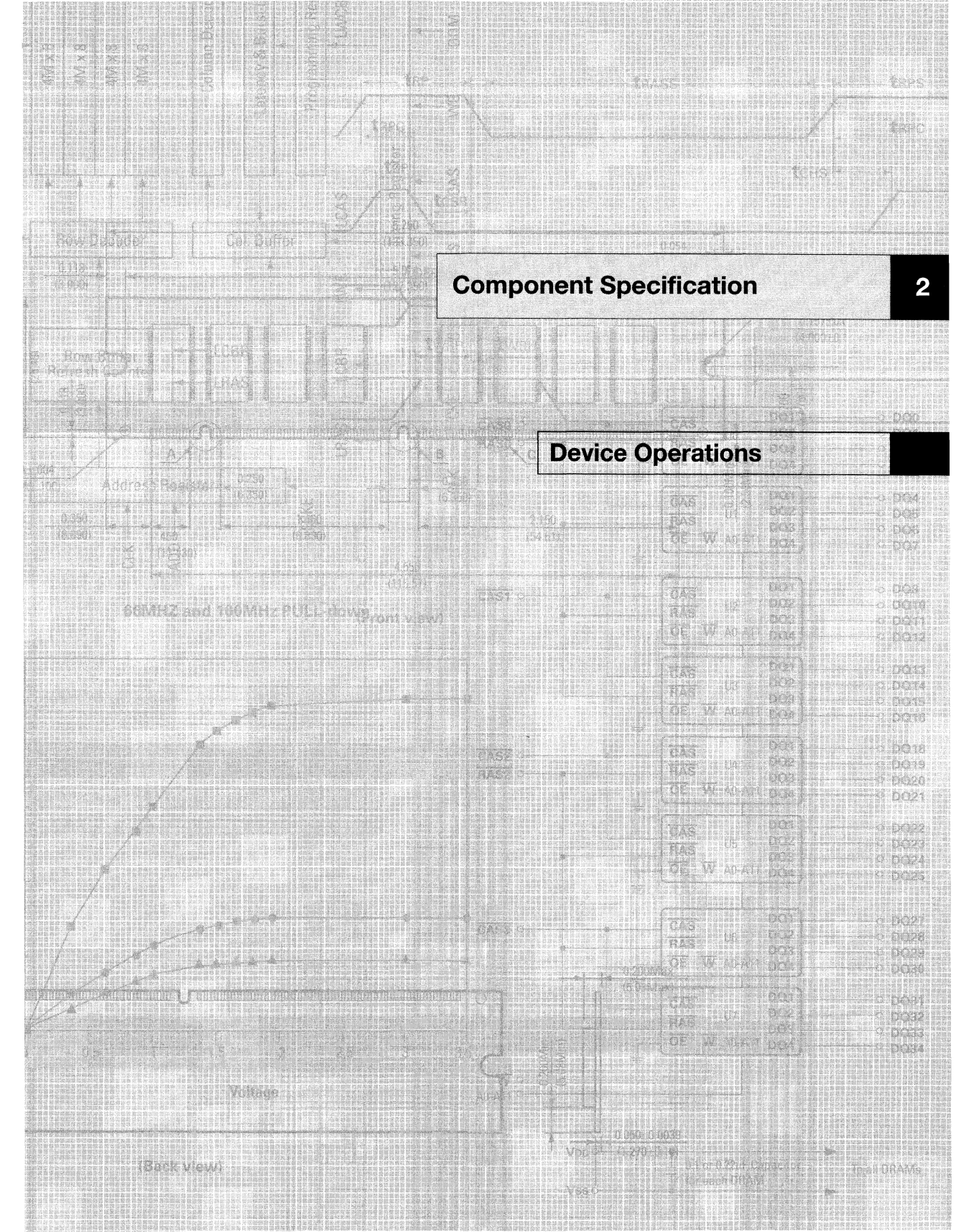
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

NOTES

Component Specification 2

Device Operations



A. MODE REGISTER FIELD TABLE TO PROGRAM

Register Programmed with MRS

Address	BA0 ~ BA1	A11 ~ A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	RFU	RFU	W.B.L	TM		CAS Latency			BT	Burst Length		

Test Mode			CAS Latency				Burst Type		Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type	A2	A1	A0	BT = 0	BT = 1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	1
0	1	Reserved	0	0	1	Reserved	1	Interleave	0	0	1	2	2
1	0	Reserved	0	1	0	2			0	1	0	4	4
1	1	Reserved	0	1	1	3			0	1	1	8	8
Write Burst Length			1	0	0	Reserved			1	0	0	Reserved	Reserved
A9		Length	1	0	1	Reserved			1	0	1	Reserved	Reserved
0		Burst	1	1	0	Reserved			1	1	0	Reserved	Reserved
1		Single Bit	1	1	1	Reserved			1	1	1	Full Page	Reserved

Full Page Length : x4 (1024), x8 (512), x16 (256)

B. POWER UP SEQUENCE

1. Apply power and start clock, Attempt to maintain CKE= "H", DQM= "H" and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

cf.) Sequence of 4 & 5 is regardless of the order.

The device is now ready for normal operation.

Note : 1. If A9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.
2. RFU (Reserved for future use) should stay "0" during MRS cycle.

C. BURST SEQUENCE

1. BURST LENGTH = 4

Initial Address		Sequential				Interleave			
A_1	A_0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

2. BURST LENGTH = 8

Initial Address			Sequential								Interleave							
A_2	A_1	A_0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

D. DEVICE OPERATIONS

CLOCK (CLK)

The clock input is used as the reference for all SDRAM operations. All operations are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between V_{IL} and V_{IH}. During operation with CKE high all inputs are assumed to be in a valid state (low or high) for the duration of set-up and hold time around positive edge of the clock in order to function well Q perform and I_{CC} specifications.

CLOCK ENABLE (CKE)

The clock enable(CKE) gates the clock onto SDRAM. If CKE goes low synchronously with clock (set-up and hold time are the-same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When all banks are in the idle state and CKE goes low synchronously with clock, the SDRAM enters the power down mode from the next clock cycle. The SDRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "1CLK + t_{SS}" before the high going edge of the clock, then the SDRAM becomes active from the same clock edge accepting all the input commands.

BANK ADDRESSES (BA0 ~ BA1)

: In case x 4

This SDRAM is organized as four independent banks of 4,194,304 words x 4 bits memory arrays. The BA_0 ~ BA_1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA_0 ~ BA_1 are latched at bank active, read, write, mode register set and precharge operations.

: In case x 8

This SDRAM is organized as four independent banks of 2,097,152 words x 8 bits memory arrays. The BA_0 ~ BA_1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA_0 ~ BA_1 are latched at bank active, read, write, mode register set and precharge operations.

: In case x 16

This SDRAM is organized as four independent banks of 1,048,576 words x 16 bits memory arrays. The BA_0 ~ BA_1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA_0 ~ BA_1 are latched at bank active, read, write, mode register set and precharge operations.

ADDRESS INPUTS (A0 ~ A11)

: In case x 4

The 22 address bits are required to decode the 4,194,304 word locations are multiplexed into 12 address input pins (A_0 ~ A_{11}). The 12 bit row addresses are latched along with $\overline{RAS}$ and BA_0 ~ BA_1 during bank activate command. The 10 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA_0 ~ BA_1 during read or write command.

: In case x 8

The 21 address bits are required to decode the 2,097,152 word locations are multiplexed into 12 address input pins (A_0 ~ A_{11}). The 12 bit row addresses are latched along with $\overline{RAS}$ and BA_0 ~ BA_1 during bank activate command. The 9 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA_0 ~ BA_1 during read or write command.

: In case x 16

The 20 address bits are required to decode the 1,048,576 word locations are multiplexed into 12 address input pins (A_0 ~ A_{11}). The 12 bit row addresses are latched along with $\overline{RAS}$ and BA_0 ~ BA_1 during bank activate command. The 8 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA_0 ~ BA_1 during read or write command.

NOP and DEVICE DESELECT

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high, the SDRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock cycle like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and all the address inputs are ignored.

POWER-UP

1. Apply power and start clock, Attempt to maintain CKE= "H", DQM= "H" and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
   cf.) Sequence of 4 & 5 is regardless of the order.

The device is now ready for normal operation.

D. DEVICE OPERATIONS (Continued)

MODE REGISTER SET (MRS)

The mode register stores the data for controlling the various operating modes of SDRAM. It programs the CAS latency, burst type, burst length, test mode and various vendor specific options to make SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The SDRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A_0 ~ A_{11} and BA_0 ~ BA_1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is the data written in the mode register. Two clock cycles is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on the fields of functions. The burst length field uses A_0 ~ A_2, burst type uses A_3, CAS latency (read latency from column address) use A_4 ~ A_6, vendor specific options or test mode use A_7 ~ A_8, A_{10}/AP ~ A_{11} and BA_0 ~ BA_1. The write burst length is programmed using A_9. A_7 ~ A_8, A_{10}/AP ~ A_{11} and BA_0 ~ BA_1 must be set to low for normal SDRAM operation. Refer to the table for specific codes for various burst length, burst type and CAS latencies.

BANK ACTIVATE

The bank activate command is used to select a random row in an idle bank. By asserting low on $\overline{RAS}$ and $\overline{CS}$ with desired row and bank address, a row access is initiated. The read or write operation can occur after a time delay of t_{RCD}(min) from the time of bank activation. t_{RCD} is an internal timing parameter of SDRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing t_{RCD}(min) with cycle time of the clock and then rounding off the result to the next higher integer. The SDRAM has four internal banks in the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of four banks simultaneously. Also the noise generated during sensing of each bank of SDRAM is high, requiring some time for power supplies to recover before another bank can be sensed reliably. t_{RRD}(min) specifies the minimum time required between activating different bank. The number of clock cycles required between different bank activation must be calculated similar to t_{RCD} specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by t_{RAS}(min). Every SDRAM bank activate command must satisfy t_{RAS}(min) specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by t_{RAS}(max). The number of cycles for both t_{RAS}(min) and t_{RAS}(max) can be calculated similar to t_{RCD} specification.

BURST READ

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The burst read command is issued by asserting low on $\overline{CS}$ and $\overline{CAS}$ with $\overline{WE}$ being high on the positive edge of the clock. The bank must be active for at least t_{RCD}(min) before the burst read command is issued. The first output appears in CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed. The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of the burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid at every page burst length.

BURST WRITE

The burst write command is similar to burst read command and is used to write data into the SDRAM on consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing can be completed yet. The writing can be completed by issuing a burst read and DQM for blocking data inputs or burst write in the same or another active bank. The burst stop command is valid at every burst length. The write burst can also be terminated by using DQM for blocking data and procreating the bank t_{RDL} after the last data input to be written into the active row. See DQM OPERATION also.

D. DEVICE OPERATIONS (Continued)

DQM OPERATION

The DQM is used to mask input and output operations. It works similar to $\overline{OE}$ during read operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock. The DQM signal is important during burst interruptions of write with read or precharge in the SDRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is not required. Please refer to DQM timing diagram also.

PRECHARGE

The precharge operation is performed on an active bank by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ and A_{10}/AP with valid BA_0 ~ BA_1 of the bank to be precharged. The precharge command can be asserted anytime after t_{RAS}(min) is satisfied from the bank active command in the desired bank. t_{RP} is defined as the minimum number of clock cycles required to complete row precharge is calculated by dividing t_{RP} with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by t_{RAS}(max). Therefore, each bank activate command. At the end of precharge, the bank enters the idle state and is ready to be activated again. Entry to Power down, Auto refresh, Self refresh and Mode register set etc. is possible only when all banks are in idle state.

AUTO PRECHARGE

The precharge operation can also be performed by using auto precharge. The SDRAM internally generates the timing to satisfy t_{RAS}(min) and "t_{RP}" for the programmed burst length and $\overline{CAS}$ latency. The auto precharge command is issued at the same time as burst read or burst write by asserting high on A_{10}/AP. If burst read or burst write by asserting high on A_{10}/AP, the bank is left active until a new command is asserted. Once auto precahrge command is given, no new commands are possible to that particular bank until the bank achieves idle state.

BOTH BANKS PRECHARGE

Both banks can be precharged at the same time by using Precharge all command. Asserting low on $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ with high on A_{10}/AP after all banks have satisfied t_{RAS}(min) requirement, performs precharge on all banks. At the end of t_{RP} after performing precharge to all the banks, both banks are in idle state.

AUTO REFRESH

The storage cells of SDRAM need to be refreshed every 64ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ with high on CKE and $\overline{WE}$. The auto refresh command can only be asserted with both banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle). The time required to complete the auto refresh operation is specified by t_{RC}(min). The minimum number of clock cycles required can be calculated by driving t_{RC} with clock cycle time and them rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. All banks will be in the idle state at the end of auto refresh operation. The auto refresh is the preferred refresh mode when the SDRAM is being used for normal data transactions. The auto refresh cycle can be performed once in 15.6us or a burst of 4096 auto refresh cycles once in 64ms.

SELF REFRESH

The self refresh is another refresh mode available in the SDRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SDRAM. In self refresh mode, the SDRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing are internally generated to reduce power consumption.

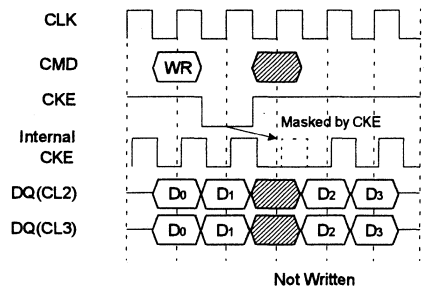
The self refresh mode is entered from all banks idle state by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE with high on $\overline{WE}$. Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including the clock are ignored in order to remain in the self refresh mode.

The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of t_{RC} before the SDRAM reaches idle state to begin normal operation. If the system uses burst auto refresh during normal operation, it is recommended to use burst 4096 auto refresh cycles immediately after exiting in self refresh mode.

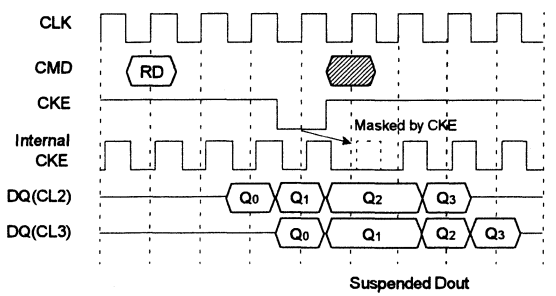
E. BASIC FEATURE AND FUNCTION DESCRIPTIONS

1. CLOCK Suspend

1) Clock Suspended During Write (BL=4

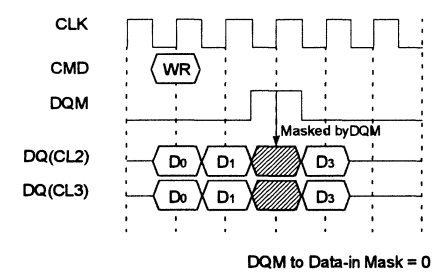


2) Clock Suspended During Read (BL=4)

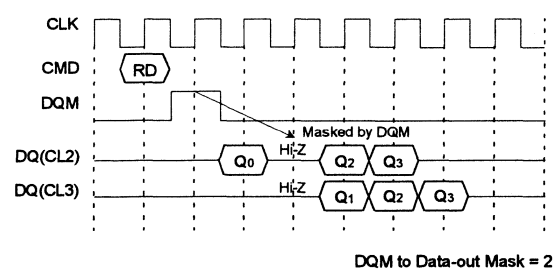


2. DQM Operation

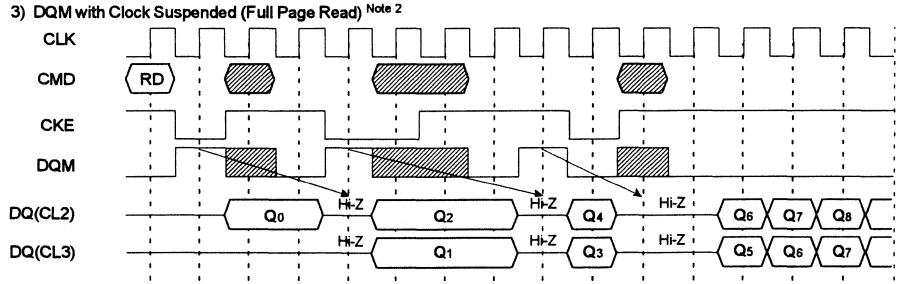
1) Write Mask (BL=4)



2) Read Mask (BL=4)



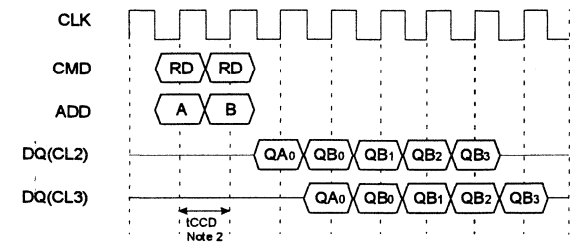
3) DQM with Clock Suspended (Full Page Read) Note 2



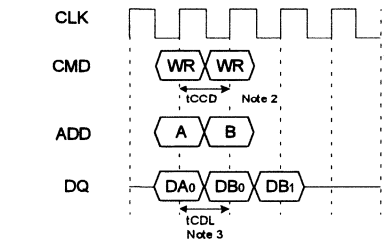
*Note : 1. CKE to CLK disable/enable = 1CLK.
2. DQM makes data out Hi-Z after 2CLKs which should masked by CKE " L"
3. DQM masks both data-in and data-out.

3. $\overline{CAS}$ Interrupt (I)

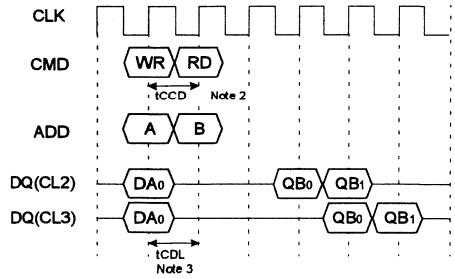
1) Read interrupted by Read (BL=4) Note 1



2) Write interrupted by Write (BL=2)



3) Write interrupted by Read (BL=2)

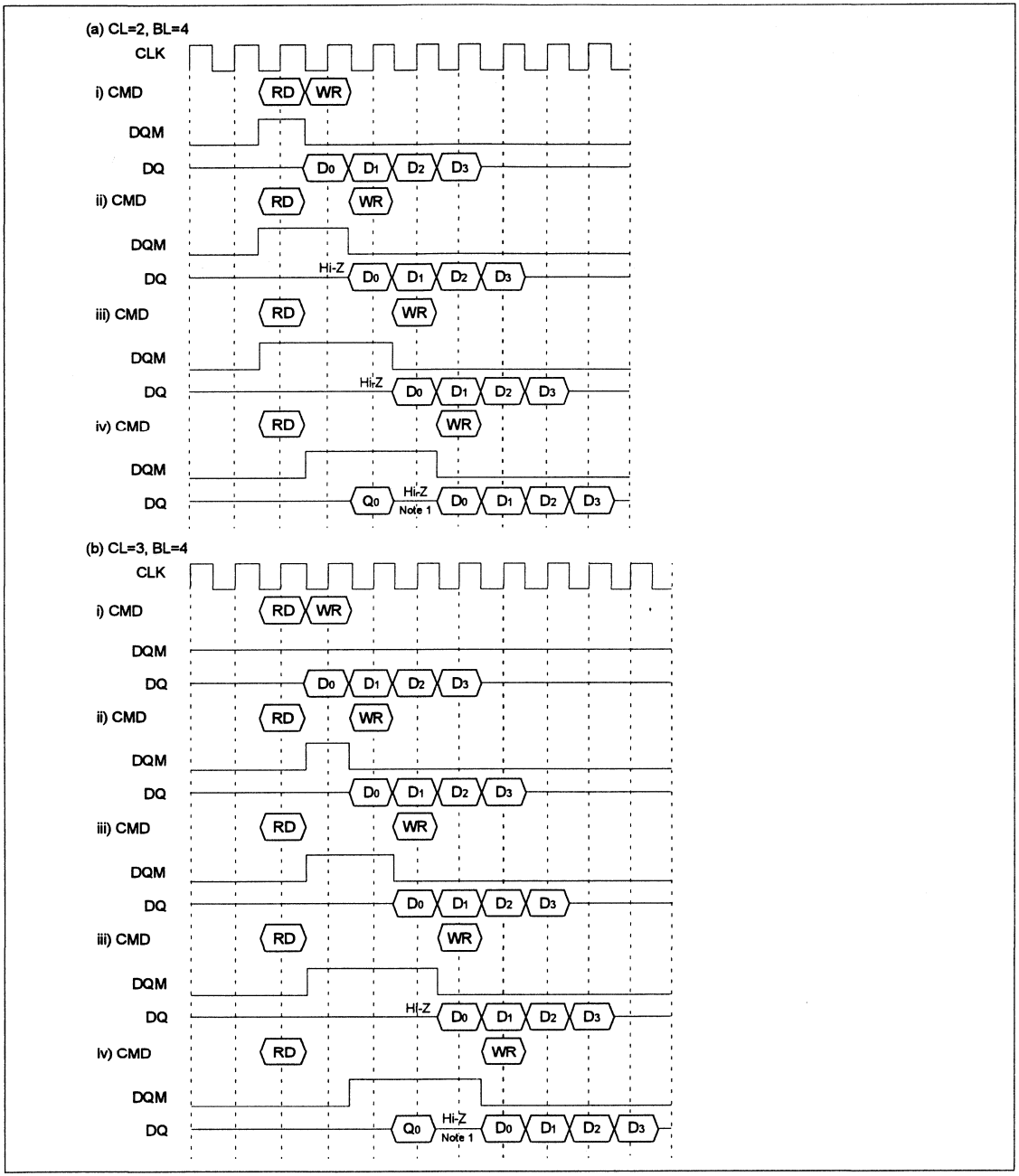


*Note : 1. By " Interrupt", It is meant to stop burst read/write by external command before the end of burst.
By "$\overline{CAS}$ Interrupt", to stop burst read/write by $\overline{CAS}$ access ; read and write.

2. t_{CCD} : $\overline{CAS}$ to $\overline{CAS}$ delay. (=1CLK)

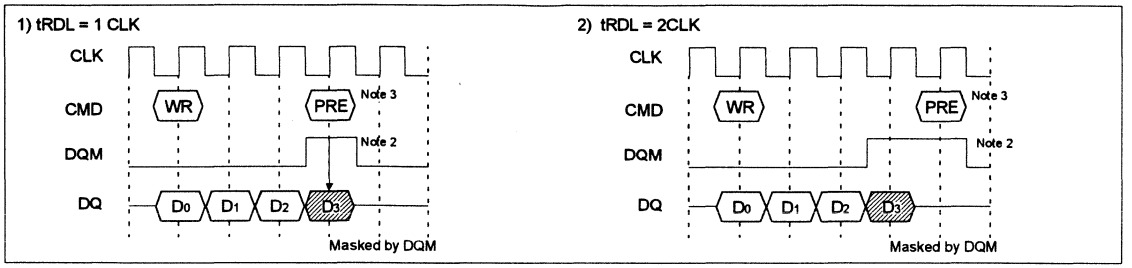
3. t_{CDL} : Last data in to new column address delay. (=1CLK)

4. $\overline{CAS}$ Interrupt (II) : Read Interrupted by Write & DQM



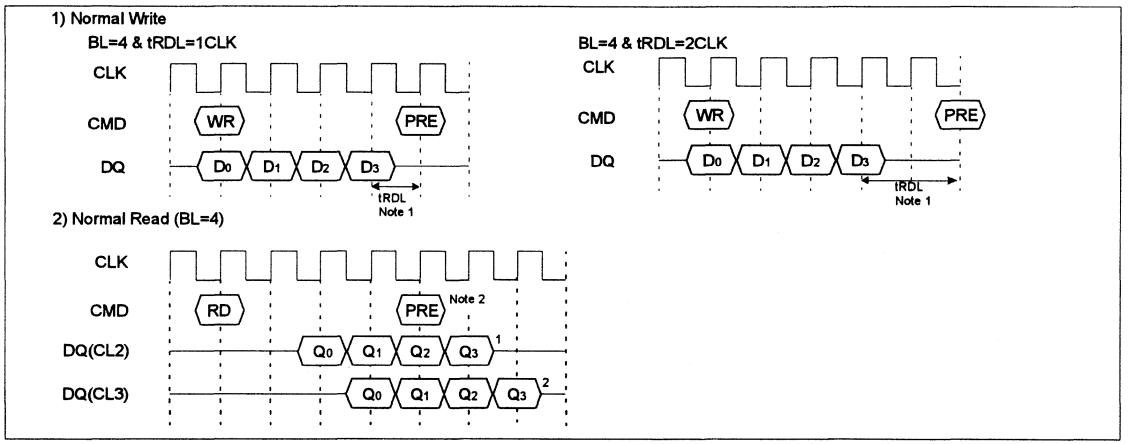
*Note : 1. To prevent bus contention, there should be at least one gap between data in and data out.

5. Write Interrupted by Precharge & DQM

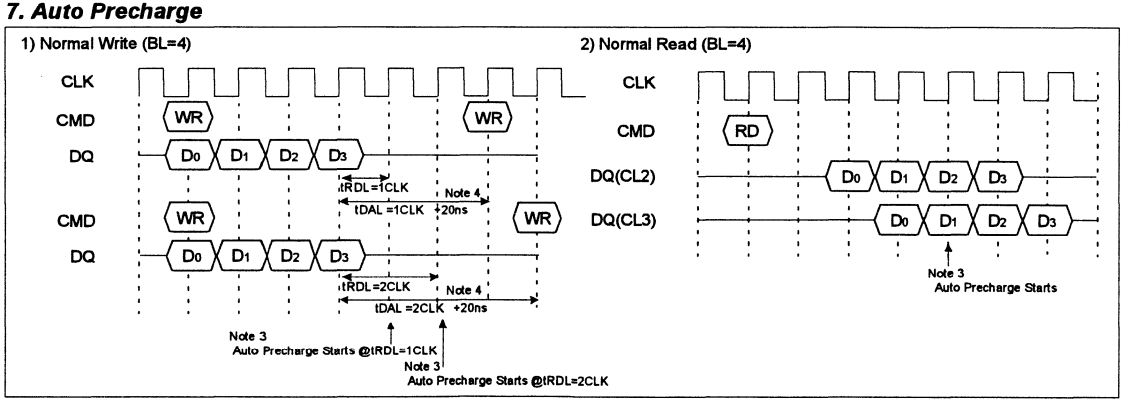


*Note : 1. To prevent bus contention, DQM should be issued which makes at least one gap between data in and data out.
2. To inhibit invalid write, DQM should be issued.
3. This precharge command and burst write command should be of the same bank, otherwise it is not precharge interrupt but only another bank precharge of four banks operation.

6. Precharge



7. Auto Precharge

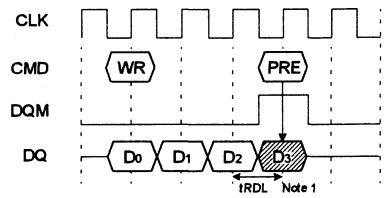


*Note : 1. SAMSUNG can support tRDL=1CLK and tRDL=2CLK for all memory devices. SAMSUNG recommands tRDL=2 CLK.
2. Number of valid output data after row precharge : 1, 2 for CAS Latency = 2, 3 respectively.
3. The row active command of the precharge bank can be issued after tRP from this point.
The new read/write command of other activated bank can be issued from this point.
At burst read/write with auto precharge, CAS interrupt of the same bank is illegal
4. tDAL defined Last data in to Active delay. SAMSUNG can support tDAL=1CLK+20ns and 2CLK+20ns ,recommands tDAL=2CLK+20ns.

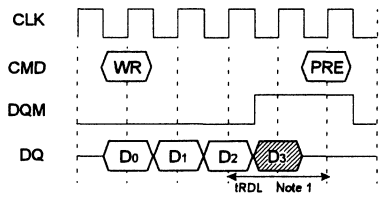
8. Burst Stop & Interrupted by Precharge

1) Normal Write

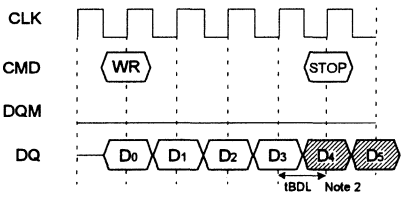
BL=4 & tRDL=1CLK



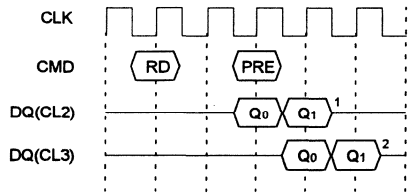
BL=4 & tRDL=2CLK



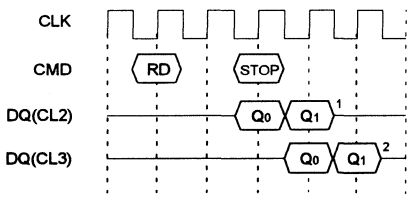
2) Write Burst Stop (BL=8)



3) Read Interrupted by Precharge (BL=4)

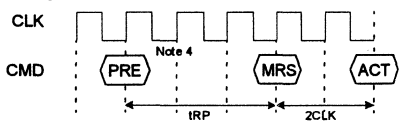


4) Read Burst Stop (BL=4)



9. MRS

1) Mode Register Set



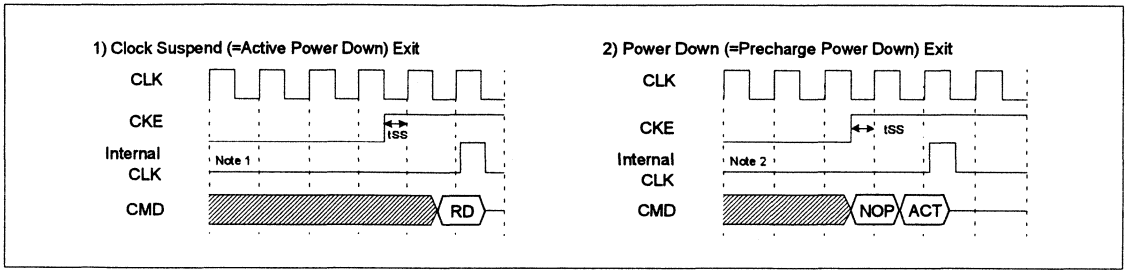
*Note : 1. SAMSUNG can support tRDL=1CLK and tRDL=2CLK for all memory devices. SAMSUNG recommands tRDL=2 CLK.

2. tBDL : 1 CLK ; Last data in to burst stop delay.
   Read or write burst stop command is valid at every burst length.

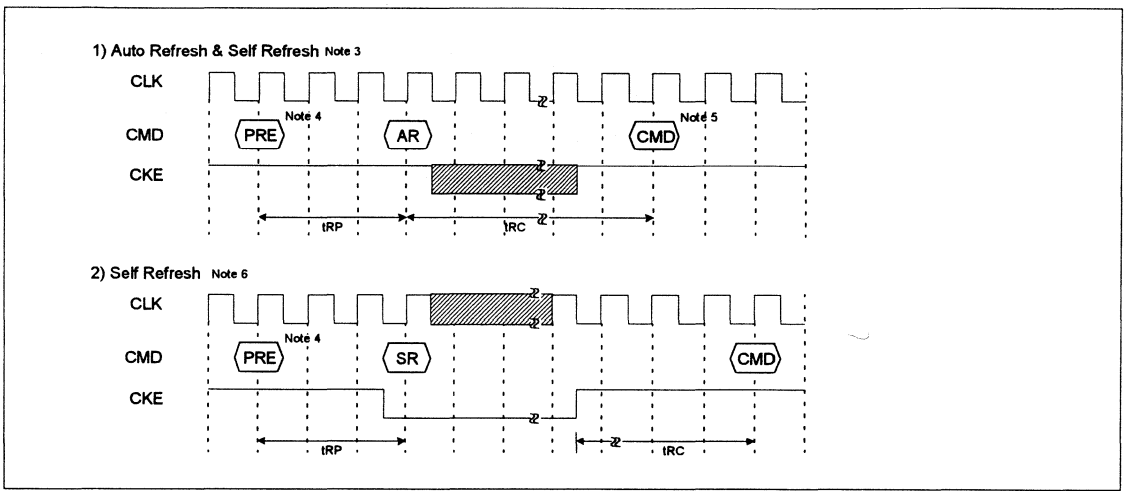
3. Number of valid output data after row precharge or burst stop : 1, 2 for CAS latency= 2, 3 respectively.

4. PRE : All banks precharge if necessary.
   MRS can be issued only at all banks precharge state.

10. Clock Suspend Exit & Power Down Exit



11. Auto Refresh & Self Refresh



*Note : 1. Active power down : one or more banks active state.
2. Precharge power down : all banks precharge state.
3. The auto refresh is the same as CBR refresh of conventional DRAM.
No precharge commands are required after auto refresh command.
During t_{RC} from auto refresh command, any other command can not be accepted.
4. Before executing auto/self refresh command, all banks must be idle state.
5. MRS, Bank Active, Auto/Self Refresh, Power Down Mode Entry.
6. During self refresh mode, refresh interval and refresh operation are performed internally.
After self refresh entry, self refresh mode is kept while CKE is low.
During self refresh mode, all inputs except CKE will be don't cared, and outputs will be in Hi-Z state.
For the time interval of t_{RC} from self refresh exit command, any other command can not be accepted.
Before/After self refresh mode, burst auto refresh cycle (4096 cycles) is recommended.

12. About Burst Type Control

Basic MODE	Sequential Counting	At MRS A_3 = "0". See the BURST SEQUENCE TABLE. (BL=4, 8) BL=1, 2, 4, 8 and full page.
	Interleave Counting	At MRS A_3 = "1". See the BURST SEQUENCE TABLE. (BL=4, 8) BL=4, 8. At BL=1, 2 Interleave Counting = Sequential Counting
Random MODE	Random column Access t_{CCD} = 1 CLK	Every cycle Read/Write Command with random column address can realize Random Column Access. That is similar to Extended Data Out (EDO) Operation of conventional DRAM.

13. About Burst Length Control

Basic MODE	1	At MRS $A_{2,1,0}$ = "000". At auto precharge, t_{RAS} should not be violated.
	2	At MRS $A_{2,1,0}$ = "001". At auto precharge, t_{RAS} should not be violated.
	4	At MRS $A_{2,1,0}$ = "010".
	8	At MRS $A_{2,1,0}$ = "011".
	Full Page	At MRS $A_{2,1,0}$ = "111". Wrap around mode(infinite burst length) should be stopped by burst stop. $\overline{RAS}$ interrupt or $\overline{CAS}$ interrupt
Special MODE	BRSW	At MRS A_9 = "1". Read burst =1, 2, 4, 8, full page write Burst =1 At auto precharge of write, t_{RAS} should not be violated.
Random MODE	Burst Stop	t_{BDL}= 1, Valid DQ after burst stop is 1, 2 for CAS latency 2, 3 respectively Using burst stop command, any burst length control is possible.
Interrupt MODE	$\overline{RAS}$ Interrupt (Interrupted by Precharge)	Before the end of burst, Row precharge command of the same bank stops read/write burst with Row precharge. t_{RDL}= 2 with DQM, valid DQ after burst stop is 1, 2 for CAS latency 2, 3 respectively. During read/write burst with auto precharge, $\overline{RAS}$ interrupt can not be issued.
	$\overline{CAS}$ Interrupt	Before the end of burst, new read/write stops read/write burst and starts new read/write burst. During read/write burst with auto precharge, $\overline{CAS}$ interrupt can not be issued.

FUNCTION TRUTH TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	ACTION	Note
IDLE	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA, A_{10}/AP	ILLEGAL	2
	L	L	H	H	BA	RA	Row (& Bank) Active ; Latch RA	
	L	L	H	L	BA	A_{10}/AP	NOP	4
	L	L	L	H	X	X	Auto Refresh or Self Refresh	5
	L	L	L	L	OP code	OP code	Mode Register Access	5
Row Active	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	BA	CA, A_{10}/AP	Begin Read ; latch CA ; determine AP	
	L	H	L	L	BA	CA, A_{10}/AP	Begin Write ; latch CA ; determine AP	
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	Precharge	
	L	L	L	X	X	X	ILLEGAL	
Read	H	X	X	X	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	L	X	X	Term burst --> Row active	
	L	H	L	H	BA	CA, A_{10}/AP	Term burst, New Read, Determine AP	
	L	H	L	L	BA	CA, A_{10}/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	Term burst, Precharge timing for Reads	
	L	L	L	X	X	X	ILLEGAL	
Write	H	X	X	X	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	L	X	X	Term burst --> Row active	
	L	H	L	H	BA	CA, A_{10}/AP	Term burst, New read, Determine AP	3
	L	H	L	L	BA	CA, A_{10}/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	Term burst, precharge timing for Writes	3
	L	L	L	X	X	X	ILLEGAL	
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A_{10}/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA_{10}	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A_{10}/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA_{10}	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Pre-charging	H	X	X	X	X	X	NOP --> Idle after t_{RP}	
	L	H	H	H	X	X	NOP --> Idle after t_{RP}	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	NOP --> Idle after t_{RP}	4

FUNCTION TRUTH TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	ACTION	Note
Row Activating	L	L	L	X	X	X	ILLEGAL	
	H	X	X	X	X	X	NOP --> Row Active after t_{RCD}	
	L	H	H	H	X	X	NOP --> Row Active after t_{RCD}	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Refreshing	H	X	X	X	X	X	NOP --> Idle after t_{RC}	
	L	H	H	X	X	X	NOP --> Idle after t_{RC}	
	L	H	L	X	X	X	ILLEGAL	
	L	L	H	X	X	X	ILLEGAL	
	L	L	L	X	X	X	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	X	NOP --> Idle after 2 clocks	
	L	H	H	H	X	X	NOP --> Idle after 2 clocks	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	ILLEGAL	

Abbreviations : RA = Row Address BA = Bank Address
NOP = No Operation Command CA = Column Address AP = Auto Precharge

***Note :** 1. All entries assume the CKE was active (High) during the precharge clock and the current clock cycle.
2. Illegal to bank in specified state ; Function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA (and A_{10}/AP).
5. Illegal if any bank is not idle.

FUNCTION TRUTH TABLE (TABLE 2)

Current State	CKE (n-1)	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	ACTION	Note
Self Refresh	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh --> Idle after t_{RFC} (ABI)	6
	L	H	L	H	H	H	X	Exit Self Refresh --> Idle after t_{RFC} (ABI)	6
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)	
All Banks Precharge Power Down	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Power Down --> ABI	
	L	H	L	H	H	H	X	Exit Power Down --> ABI	7
	L	H	L	H	H	L	X	ILLEGAL	7
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Low Power Mode)	
All Banks Idle	H	H	X	X	X	X	X	Refer to Table 1	
	H	L	H	X	X	X	X	Enter Power Down	
	H	L	L	H	H	H	X	Enter Power Down	8
	H	L	L	H	H	L	X	ILLEGAL	8
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	H	H	RA	Row (& Bank) Active	
	H	L	L	L	L	H	X	Enter Self Refresh	8
	H	L	L	L	L	L	OP Code	Mode Register Access	
	L	L	X	X	X	X	X	NOP	
Any State other than Listed above	H	H	X	X	X	X	X	Refer to Operations in Table 1	
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle	9
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	9
	L	L	X	X	X	X	X	Maintain Clock Suspend	

Abbreviations : ABI = All Banks Idle, RA = Row Address

*Note : 6. CKE low to high transition is asynchronous.

7. CKE low to high transition is asynchronous if restarts internal clock.
   A minimum setup time 1CLK + tss must be satisfied before any command other than exit.

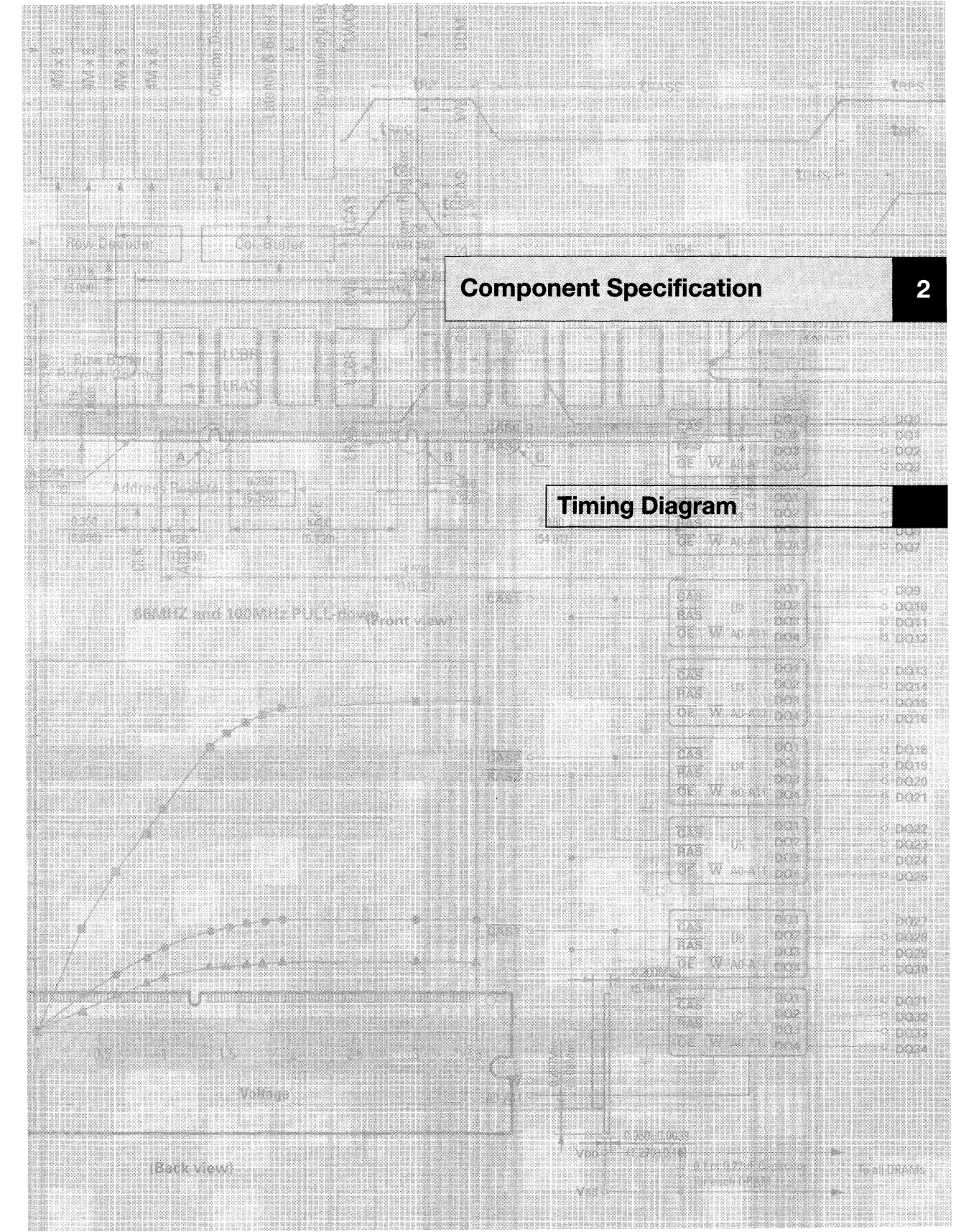
8. Power down and self refresh can be entered only from the both banks idle state.

9. Must be a legal command.

NOTES

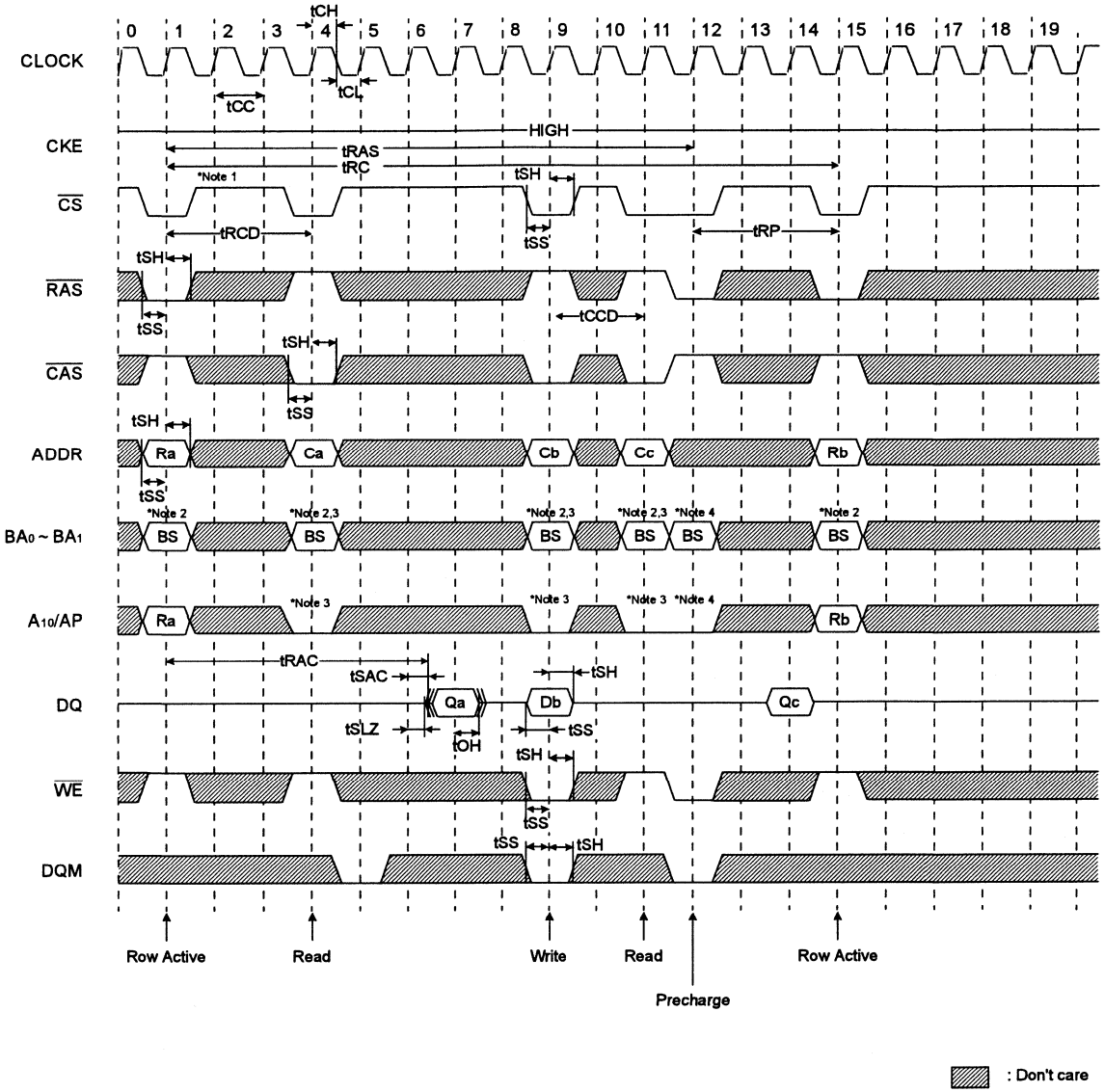
Component Specification 2

Timing Diagram



Single Bit Read - Write - Read Cycle(Same Page) @CAS Latency=3, Burst Length=1
Power Up Sequence
Read & Write Cycle at Same Bank @Burst Length=4, tRDL=1CLK
Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK
Page Read & Write Cycle at Same Bank @Burst Length=4, tRDL=1CLK
Page Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK
Page Read Cycle at Different Bank @Burst Length=4
Page Write Cycle at Different Bank @Burst Length=4, tRDL=1CLK
Page Write Cycle at Different Bank @Burst Length=4, tRDL=2CLK
Read & Write Cycle at Different Bank @Burst Length=4
Read & Write Cycle With Auto Precharge I @Burst Length=4
Read & Write Cycle With Auto Precharge II @Burst Length=4
Clock Suspension & DQM Operation Cycle @CAS Letency=2, Burst Length=4
Read Interrupted by Precharge Command & Read Burst Stop Cycle @ Full Page Burst
Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst, tRDL=1CLK
Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst, tRDL=2CLK
Burst Read Single bit Write Cycle @Burst Length =2
Active/precharge Power Dower Down Mode @CAS Latency=2 Burst Length=4
Self Refresh Entry & Exit Cycle & Exit Cycle
Mode Register Set Cycle
Auto Refresh Cycle

Single Bit Read-Write-Read Cycle(Same Page) @CAS Latency=3, Burst Length=1



*Note : 1. All input except CKE & DQM can be don't care when $\overline{CS}$ is high at the CLK high going edge.
2. Bank active & read/write are controlled by BA0~BA1.

BA0	BA1	Active & Read/Write
0	0	Bank A
0	1	Bank B
1	0	Bank C
1	1	Bank D

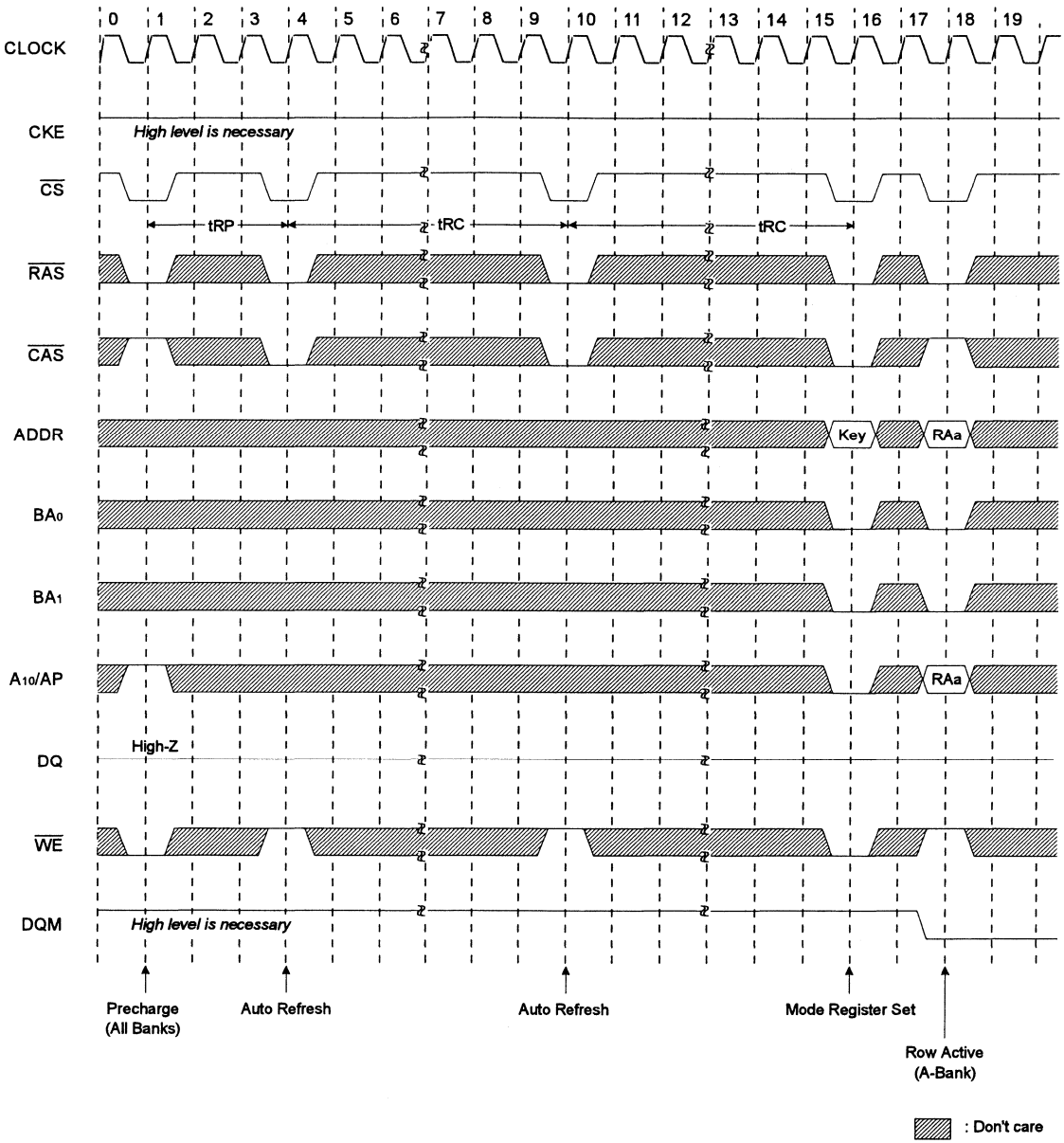
3. Enable and disable auto precharge function are controlled by A10/AP in read/write command

A10/AP	BA0	BA1	Operation
0	0	0	Disable auto precharge, leave bank A active at end of burst.
	0	1	Disable auto precharge, leave bank B active at end of burst.
	1	0	Disable auto precharge, leave bank C active at end of burst.
	1	1	Disable auto precharge, leave bank D active at end of burst.
1	0	0	Enable auto precharge, precharge bank A at end of burst.
	0	1	Enable auto precharge, precharge bank B at end of burst.
	1	0	Enable auto precharge, precharge bank C at end of burst.
	1	1	Enable auto precharge, precharge bank D at end of burst.

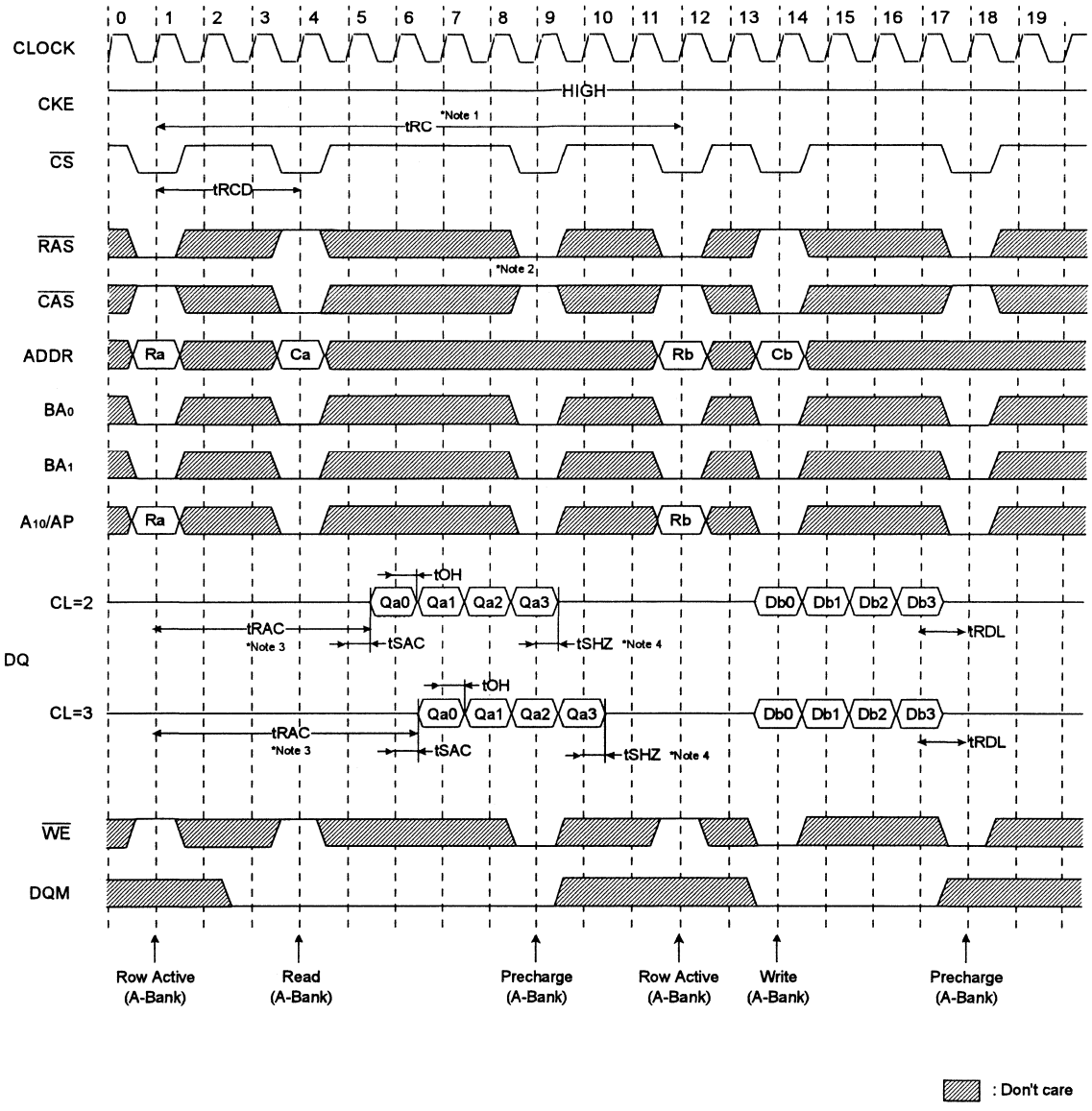
4. A10/AP and BA0~BA1 control bank precharge when precharge command is asserted.

A10/AP	BA0	BA1	Precharge
0	0	0	Bank A
0	0	1	Bank B
0	1	0	Bank C
0	1	1	Bank D
1	x	x	All Banks

Power Up Sequence



Read & Write Cycle at Same Bank @Burst Length=4, tRDL=1CLK



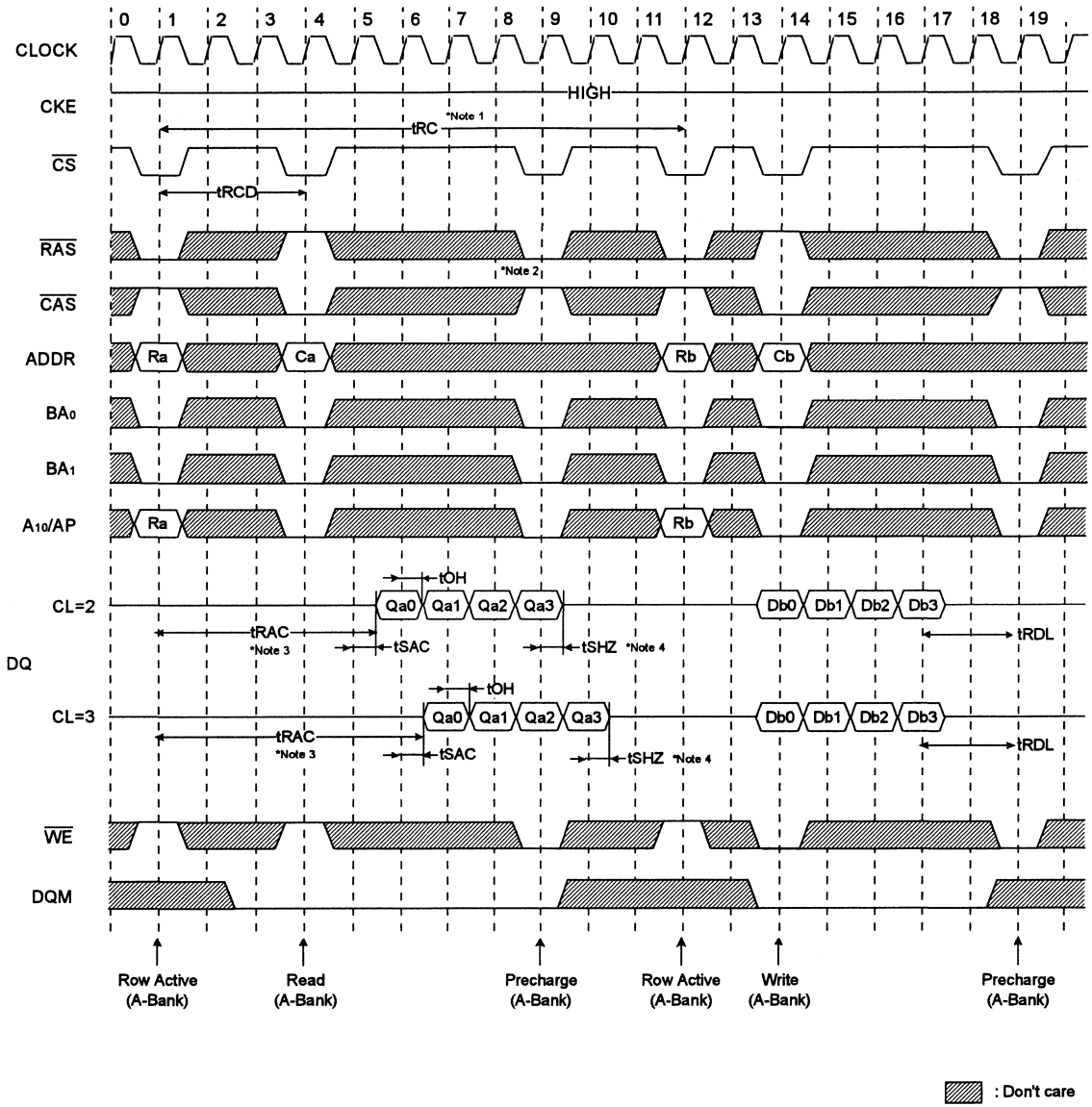
*Note : 1. Minimum row cycle times is required to complete internal DRAM operation.

2. Row precharge can interrupt burst on any cycle. [CAS Latency - 1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(t_{SHZ}) after the clcok.

3. Access time from Row active command. t_{CC} *(t_{RCD} + CAS latency - 1) + t_{SAC}

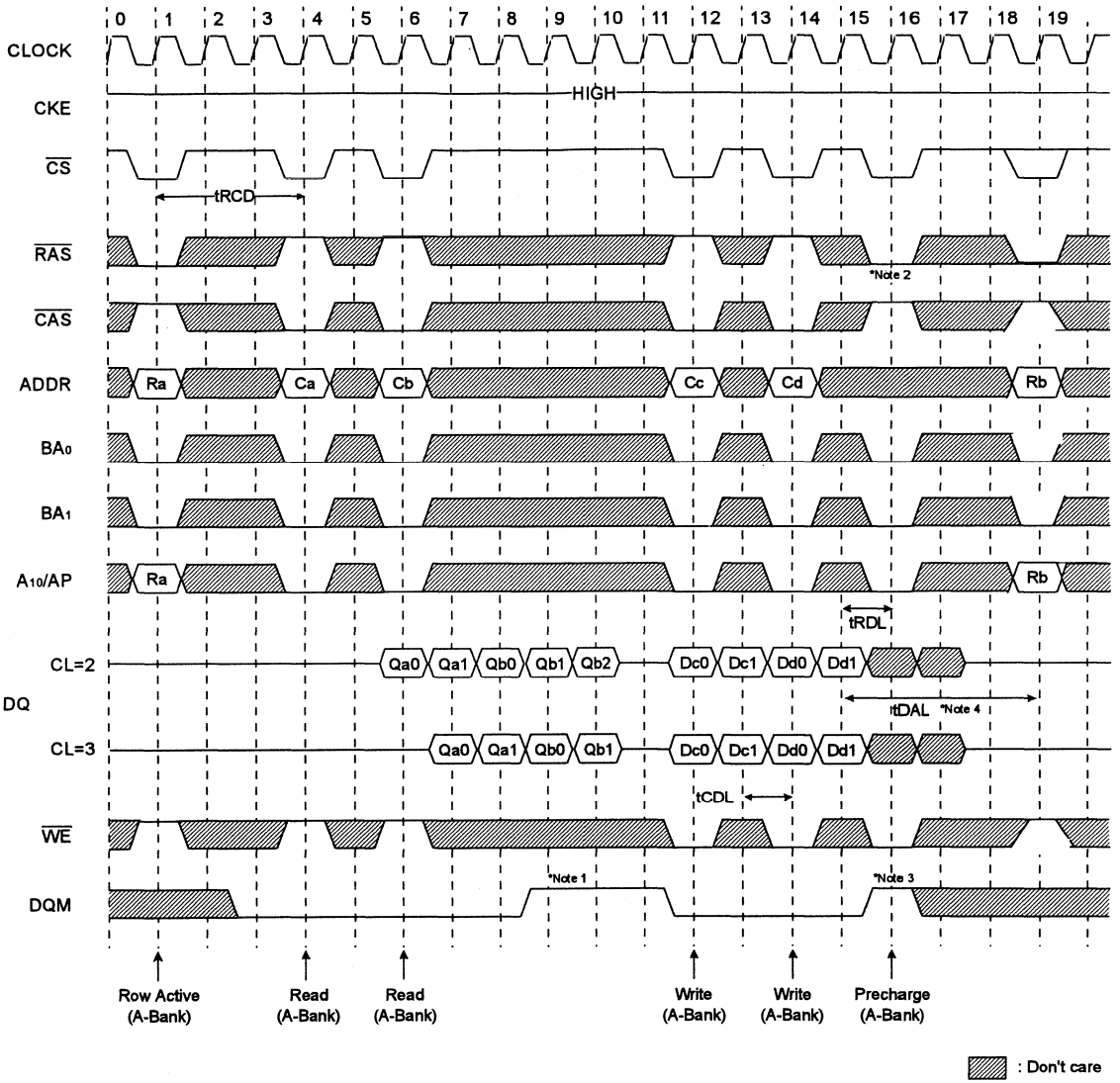
4. Ouput will be Hi-Z after the end of burst. (1, 2, 4, 8 & Full page bit burst)

Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK



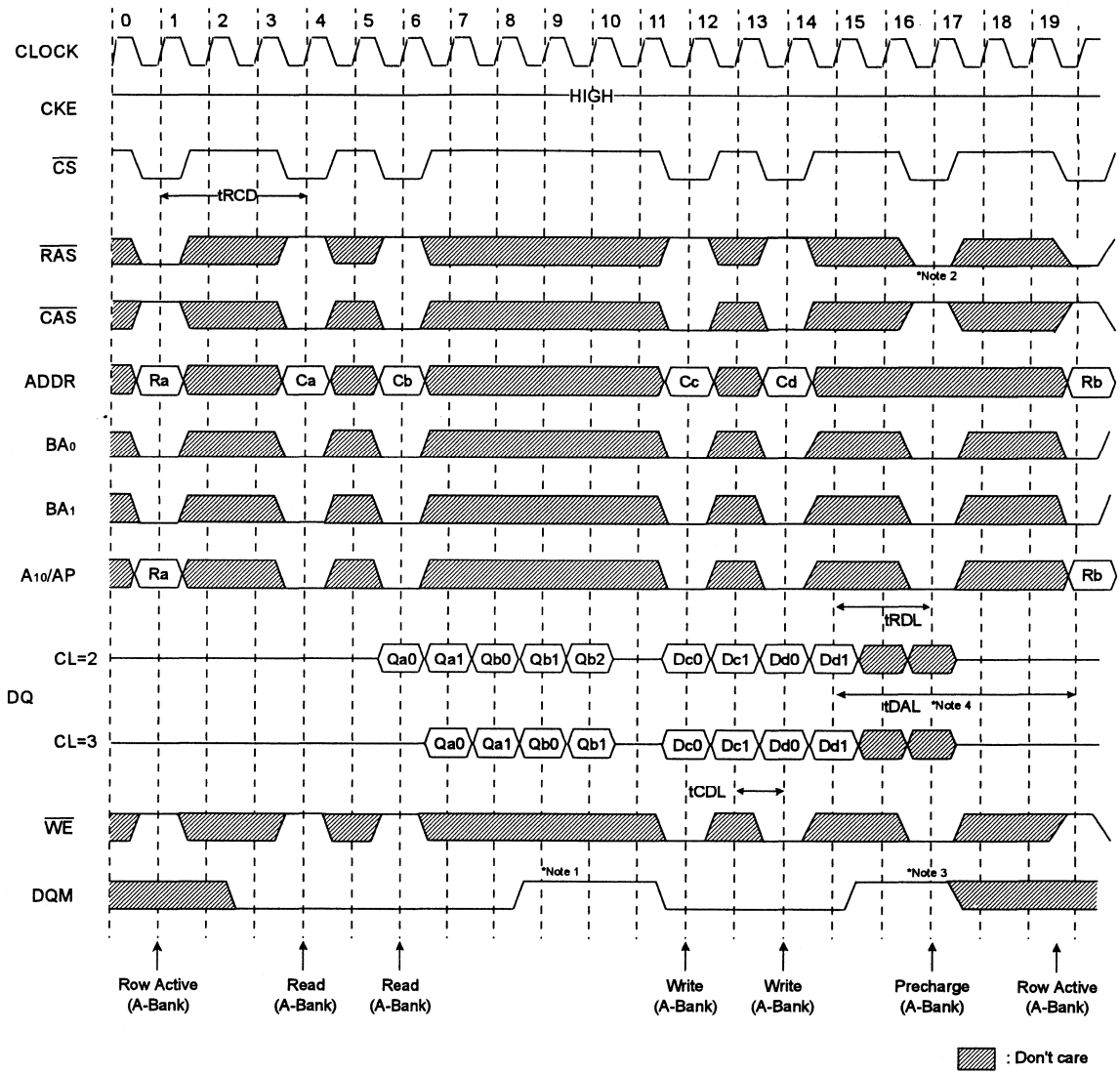
*Note : 1. Minimum row cycle times is required to complete internal DRAM operation.
2. Row precharge can interrupt burst on any cycle. [CAS Latency - 1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(tSHZ) after the clcok.
3. Access time from Row active command. tCC *(tRCD + CAS latency - 1) + tSAC
4. Ouput will be Hi-Z after the end of burst. (1, 2, 4, 8 & Full page bit burst)

Page Read & Write Cycle at Same Bank @Burst Length=4, tRDL=1CLK



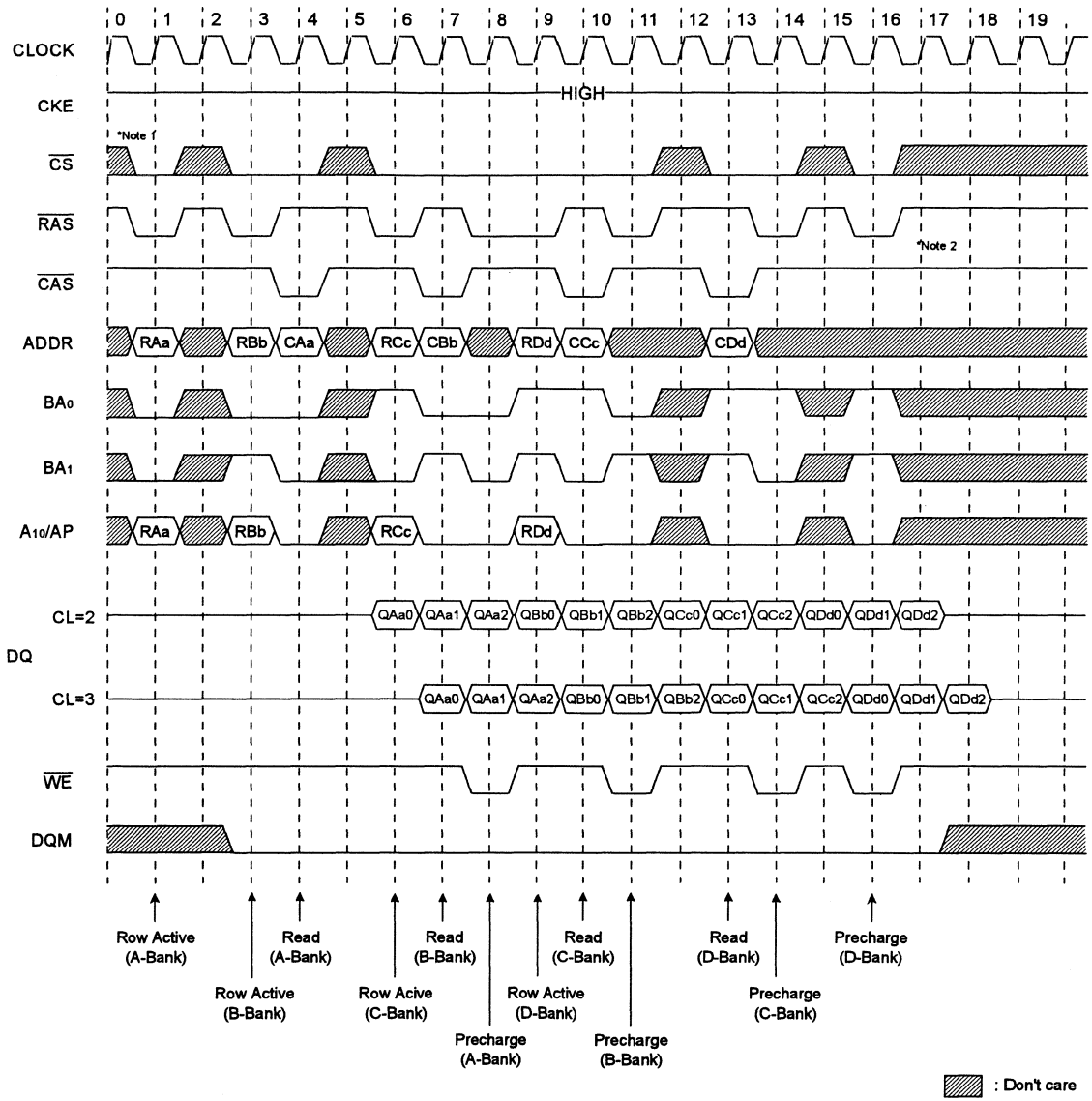
*Note :
1. To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.
2. Row precharge will interrupt writing. Last data input, tRDL before Row precharge, will be written.
3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
4. tDAL, last data in to active delay, is 1CLK + 20ns

Page Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK



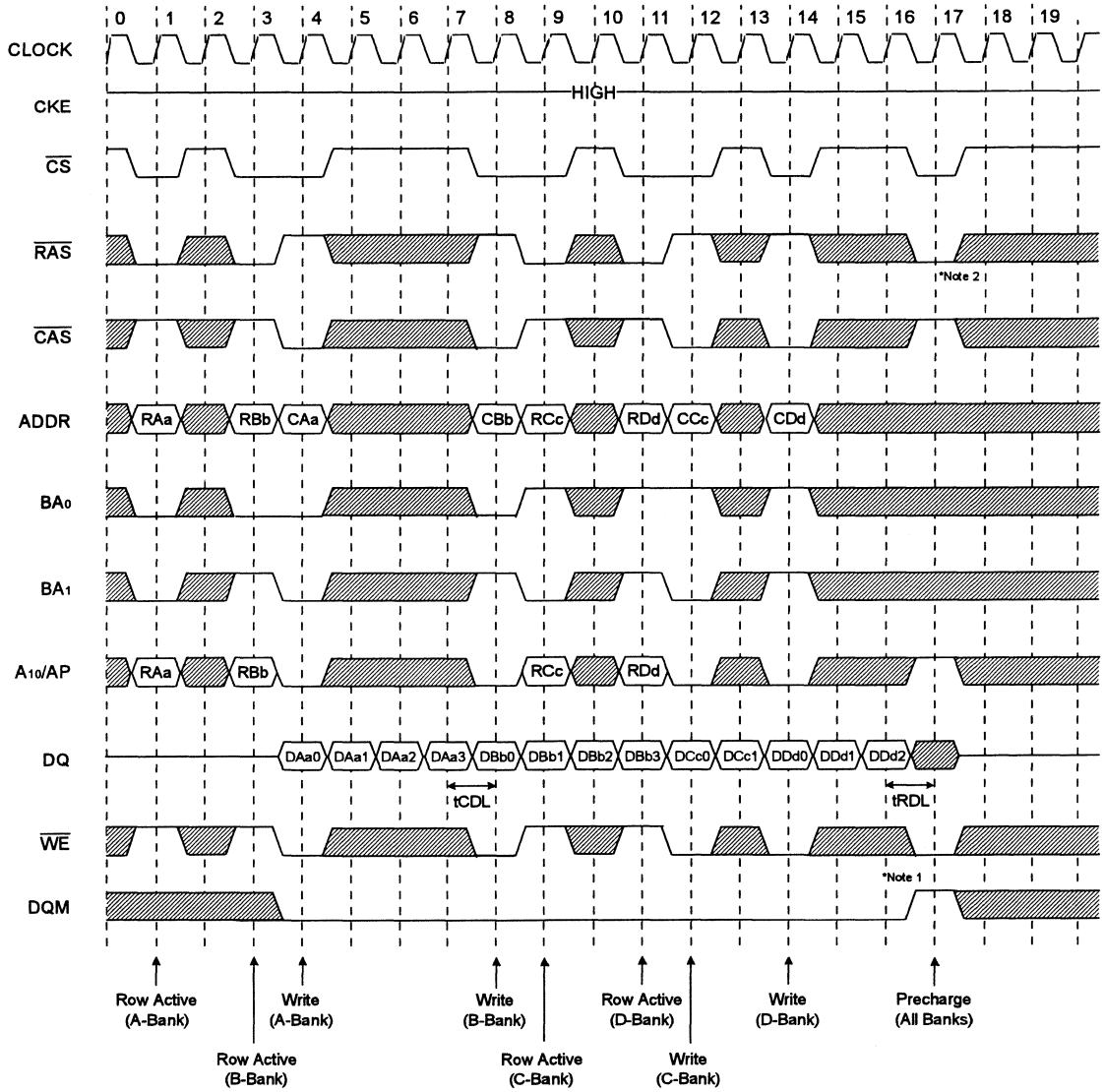
*Note :
1. To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.
2. Row precharge will interrupt writing. Last data input, tRDL before Row precharge, will be written.
3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
4. tDAL ,last data in to active delay, is 2CLK + 20ns.

Page Read Cycle at Different Bank @Burst Length=4



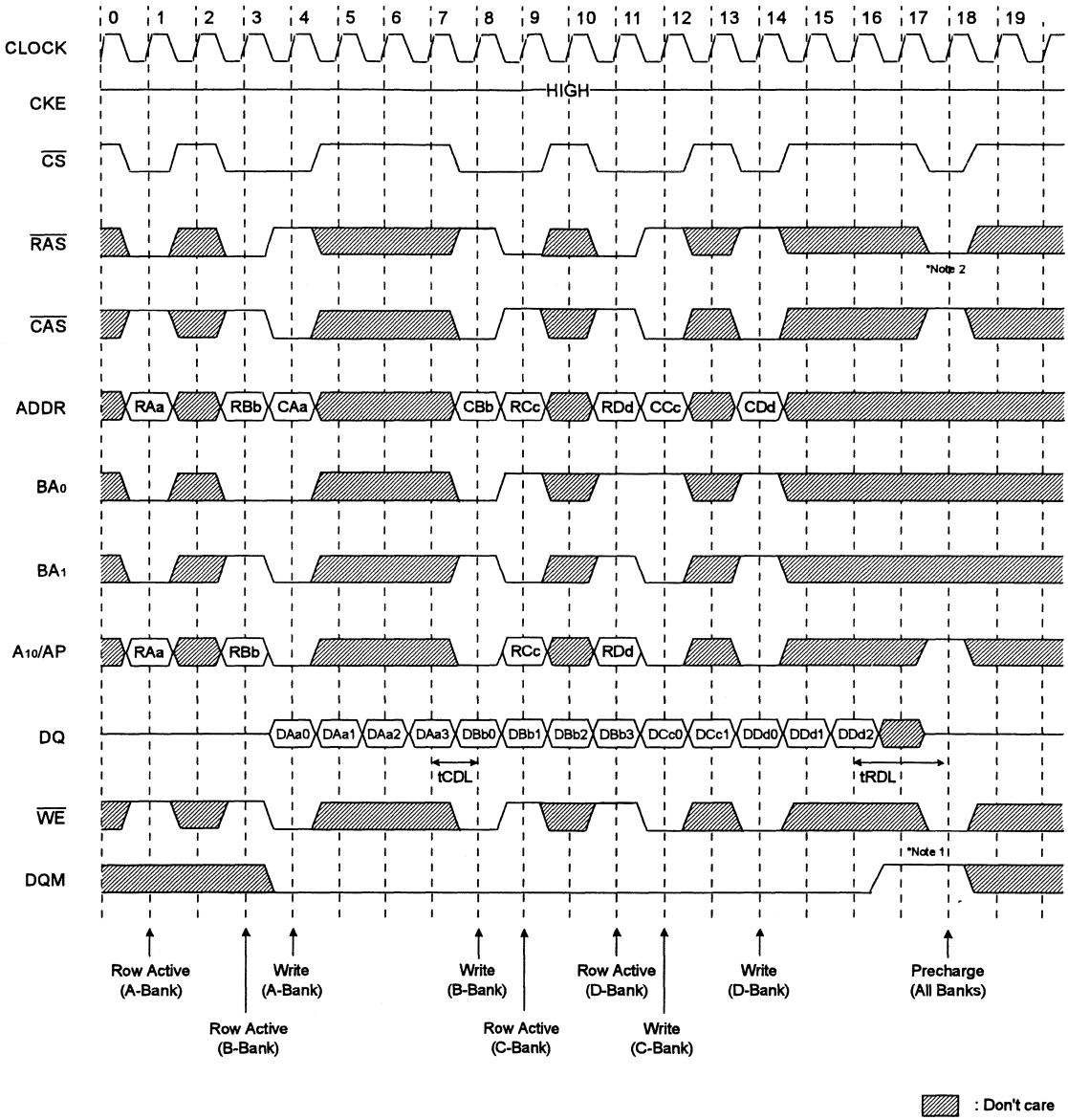
*Note : 1. $\overline{CS}$ can be don't cared when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high at the clock high going dege.
2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

Page Write Cycle at Different Bank @Burst Length=4, tRDL=1CLK



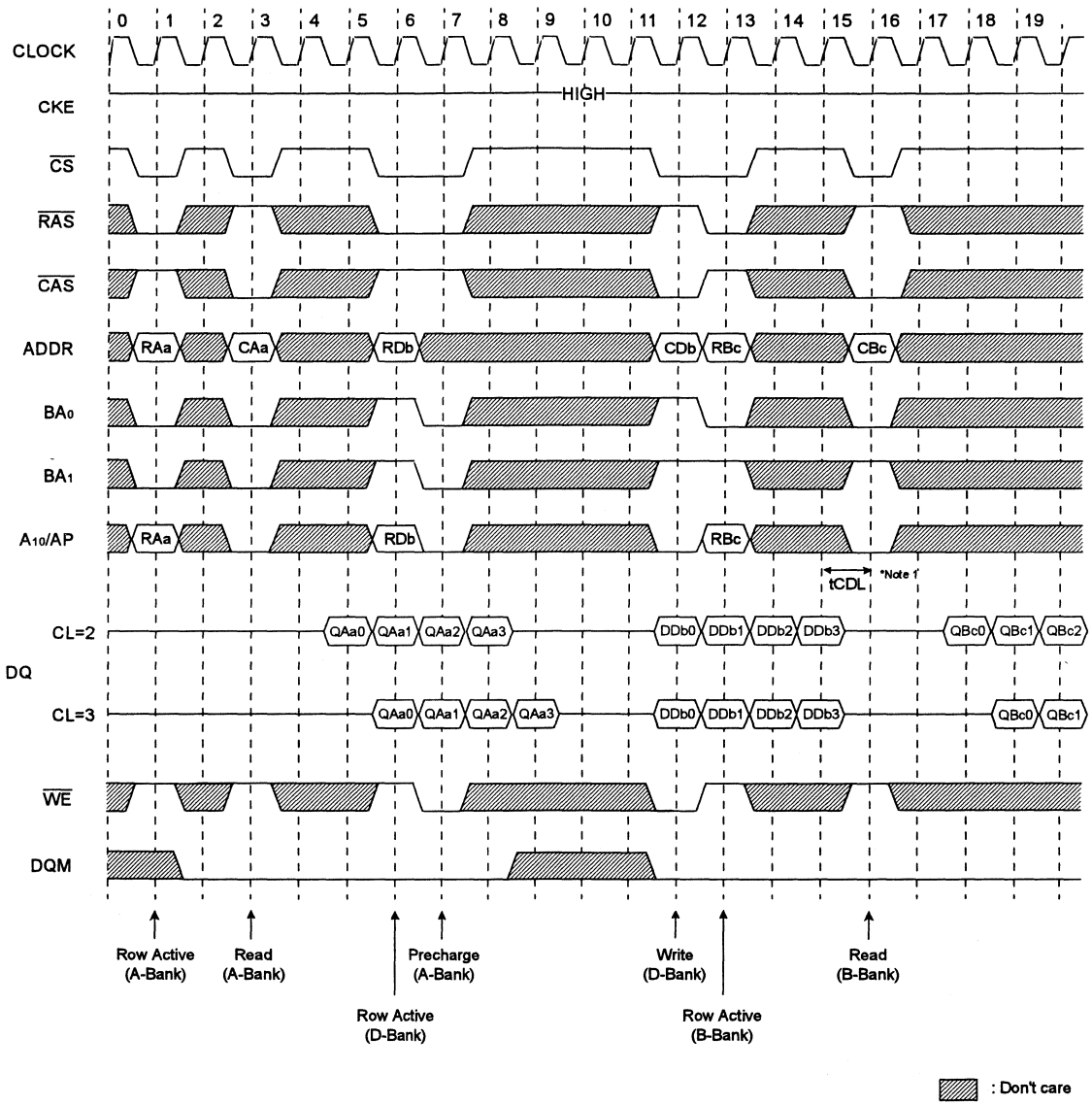
*Note : 1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
2. To interrupt burst write by Row precharge, both the write and the precharge banks must be the same.

Page Write Cycle at Different Bank @Burst Length=4, tRDL=2CLK



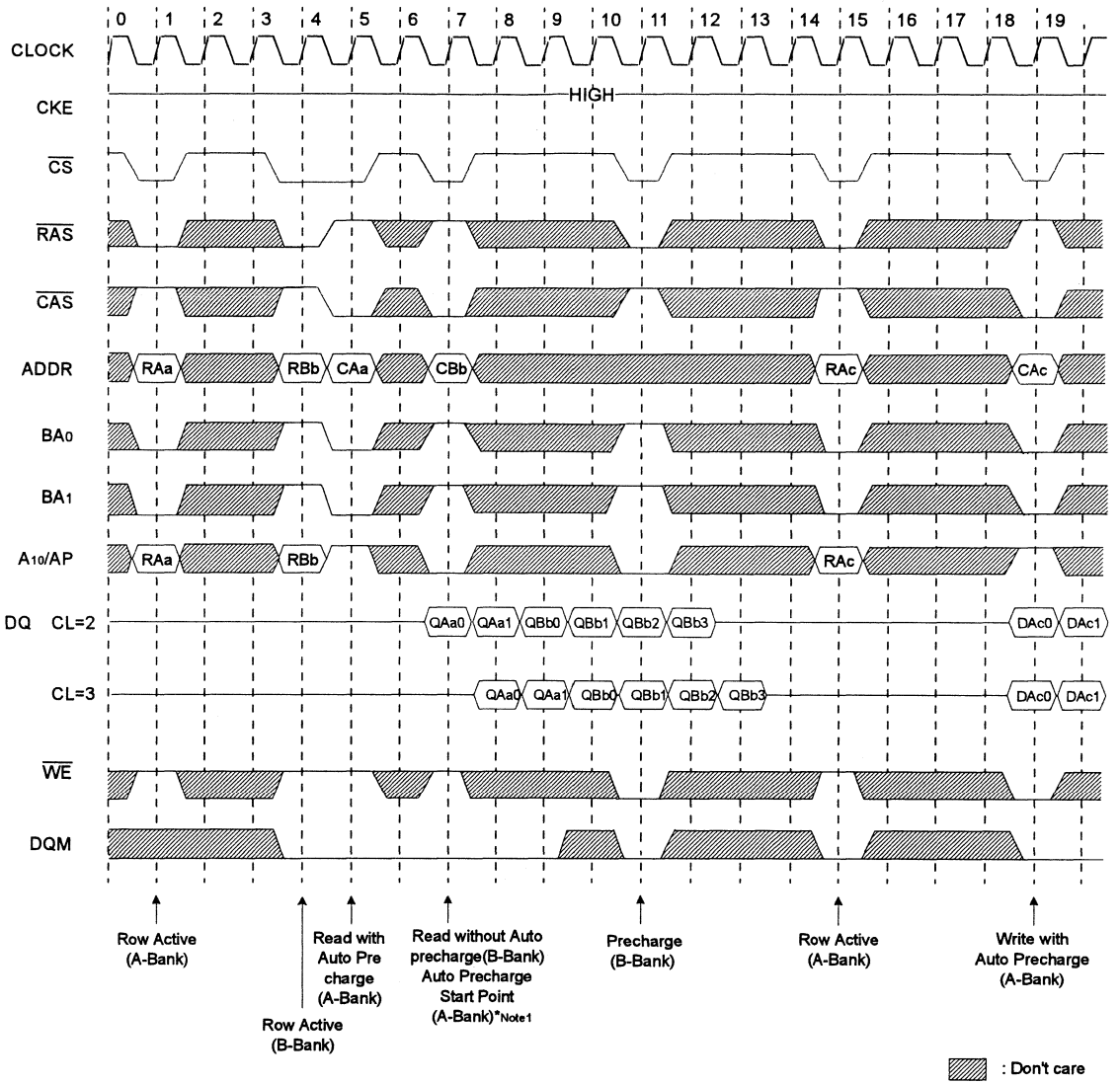
*Note : 1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
2. To interrupt burst write by Row precharge, both the write and the precharge banks must be the same.

Read & Write Cycle at Different Bank @Burst Length=4



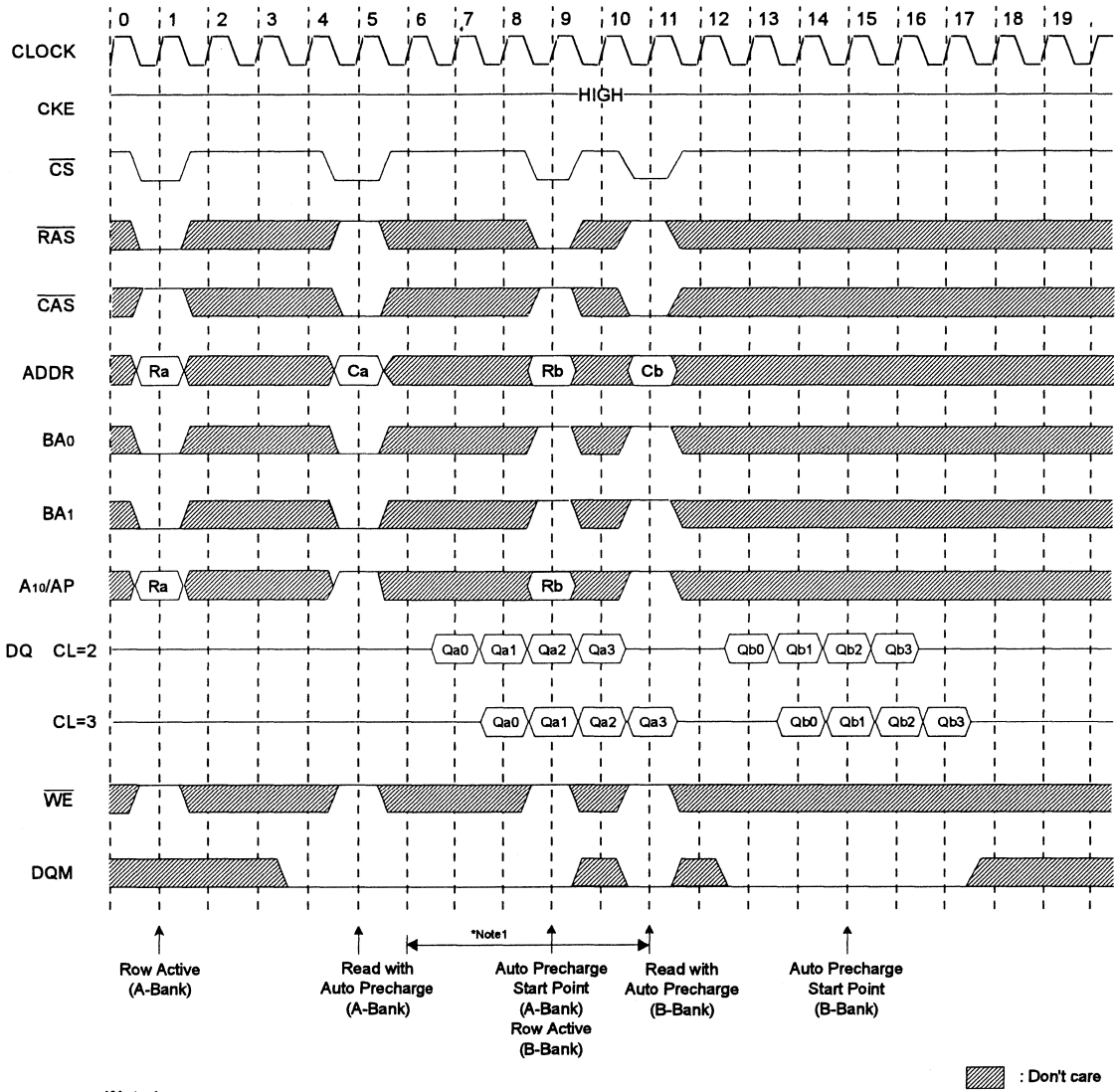
***Note :** 1. tCDL should be met to complete write.

Read & Write Cycle with Auto Precharge I @Burst Length=4



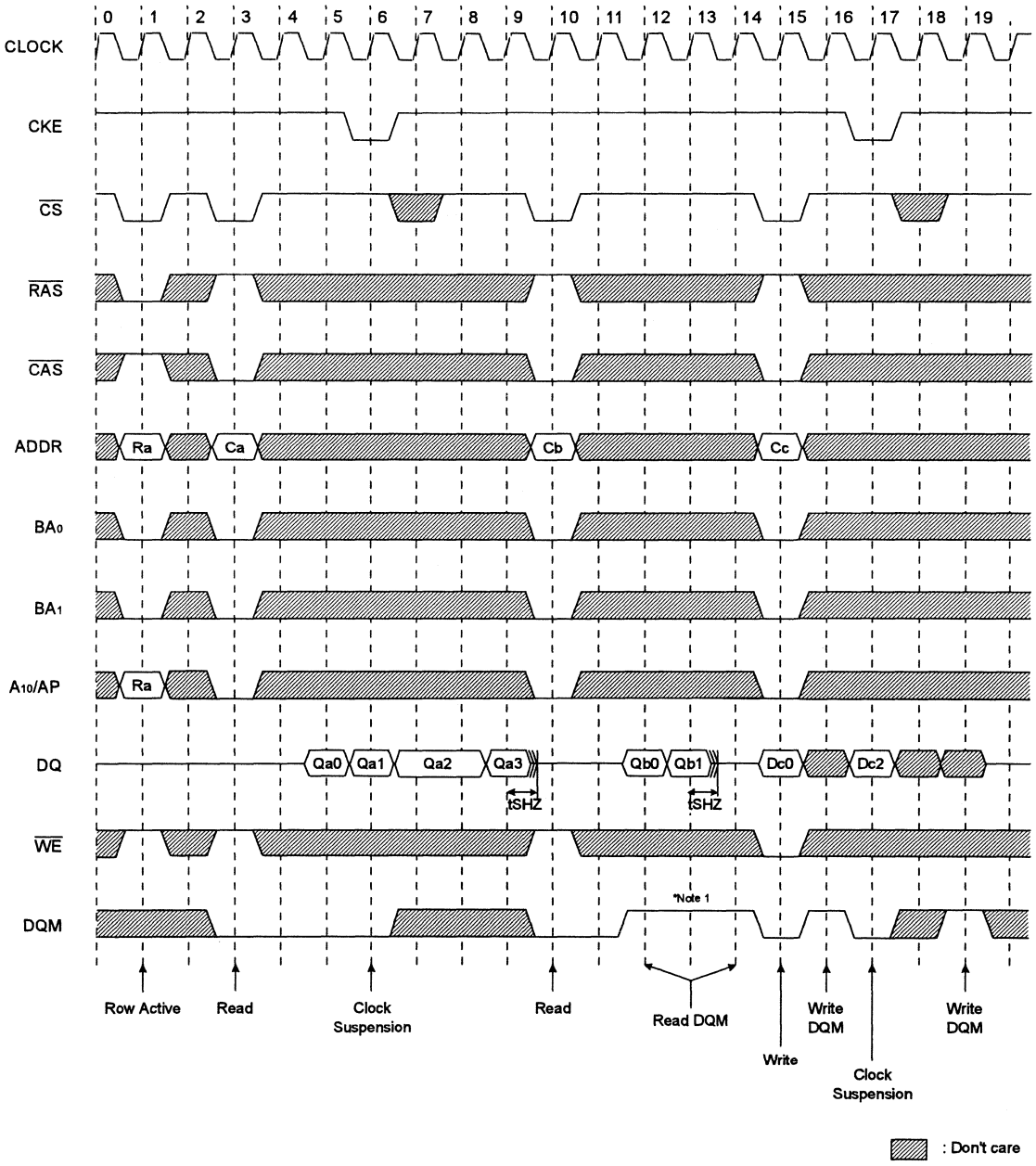
*Note1: When Read(Write) command with auto precharge is issued at A-Bank after A and B Bank activation.
- if Read(Write) command without auto precharge is issued at B-Bank before A-Bank auto precharge starts, A-Bank auto precharge will start at B-Bank read command input point .
- any command can not be issued at A-Bank during tRP after A-Bank auto precharge starts.

Read & Write Cycle with Auto Precharge II @Burst Length=4



*Note 1: Any command to A-bank is not allowed in this period.
tRP is determined from at auto precharge start point

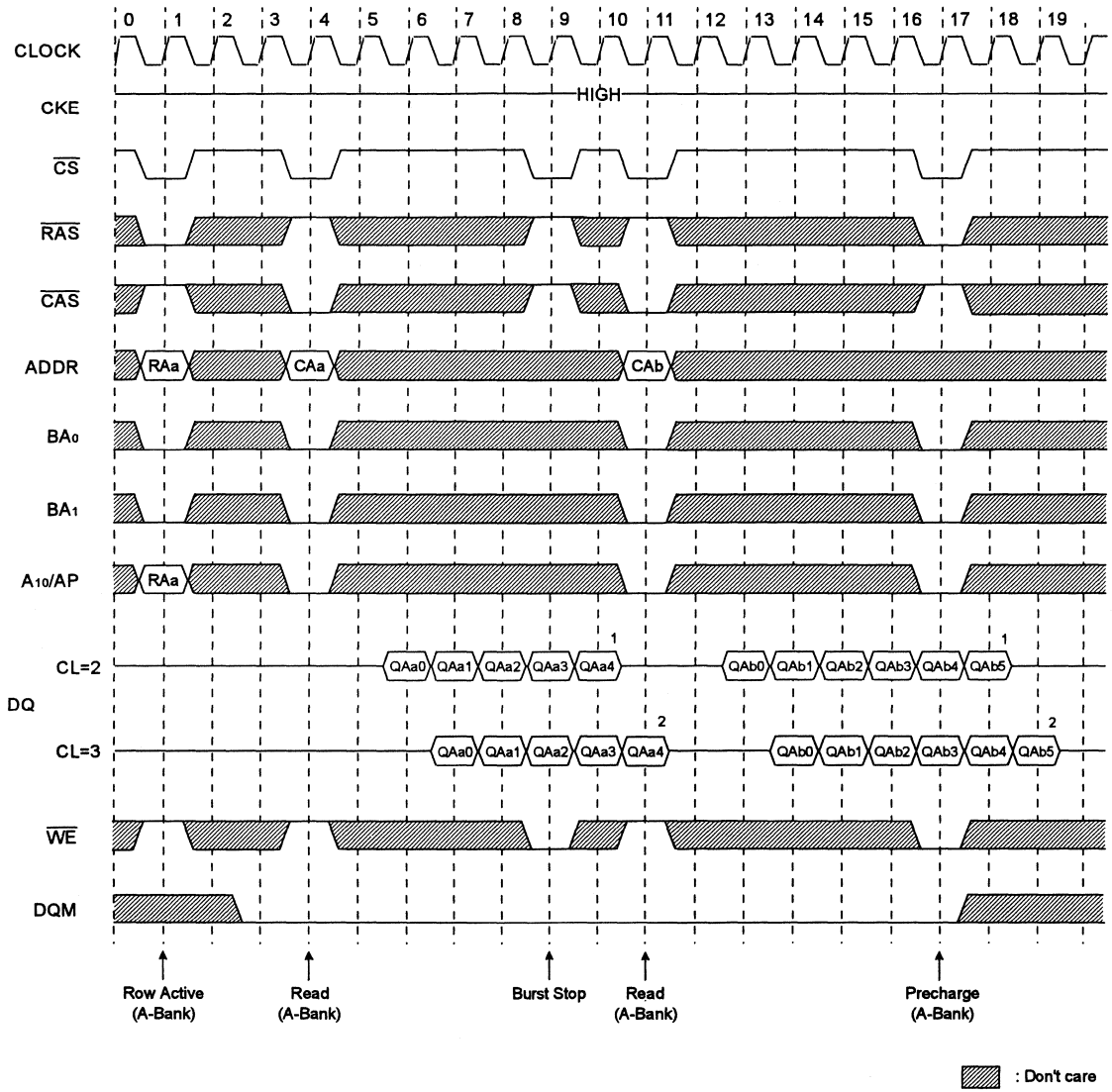
Clock Suspension & DQM Operation Cycle @CAS Latency=2, Burst Length=4



*Note1 : DQM is needed to prevent bus contention.

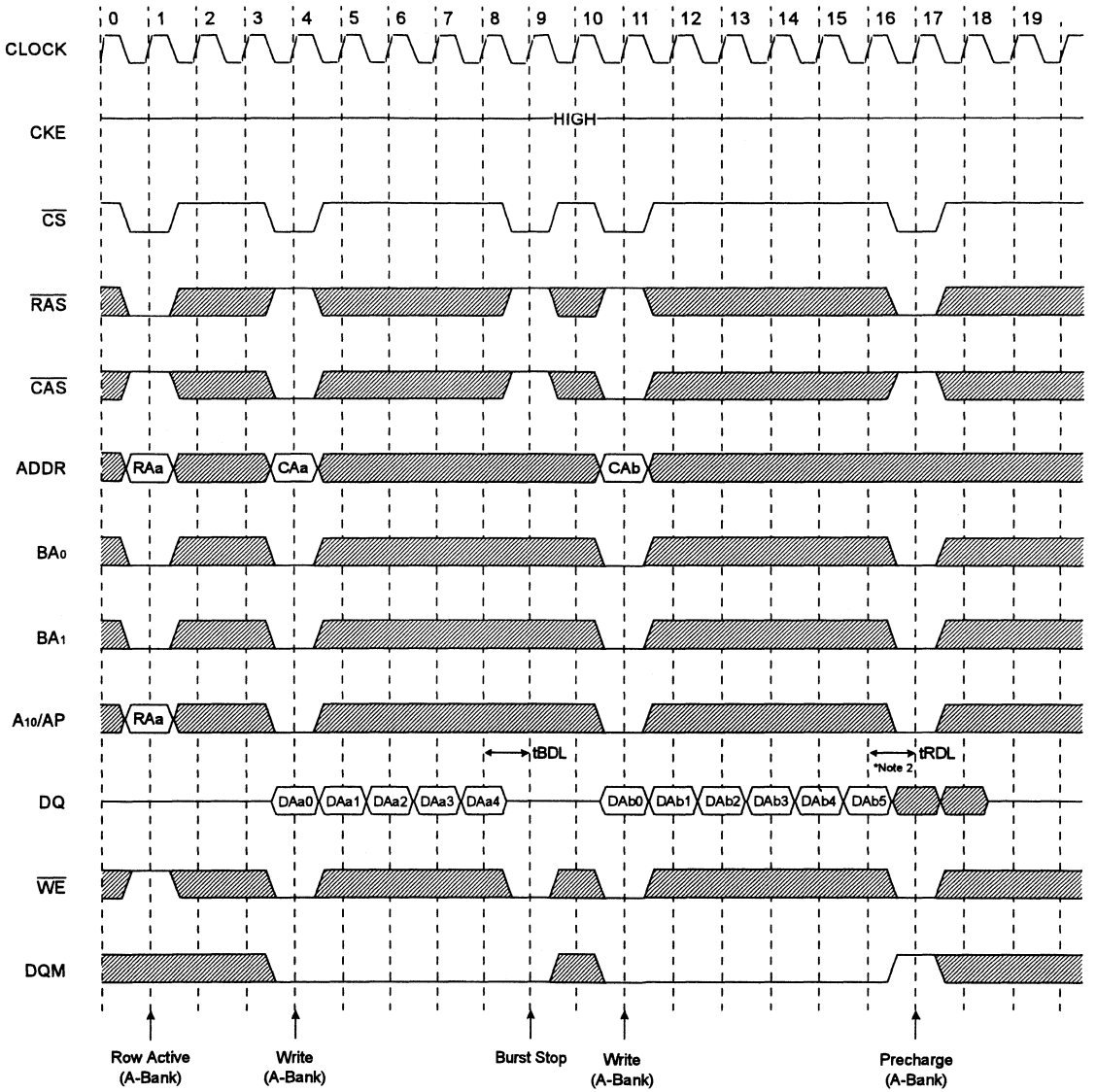
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Read Interrupted by Precharge Command & Read Burst Stop Cycle @ Full Page Burst



*Note : 1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
2. About the valid DQs after burst stop, it is same as the case of $\overline{RAS}$ interrupt.
Both cases are illustrated above timing diagram. See the label 1, 2 on them.
But at burst write, Burst stop and $\overline{RAS}$ interrupt should be compared carefully.
Refer the timing diagram of "Full page write burst stop cycle".
3. Burst stop is valid at every burst length.

Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst, tRDL=1CLK

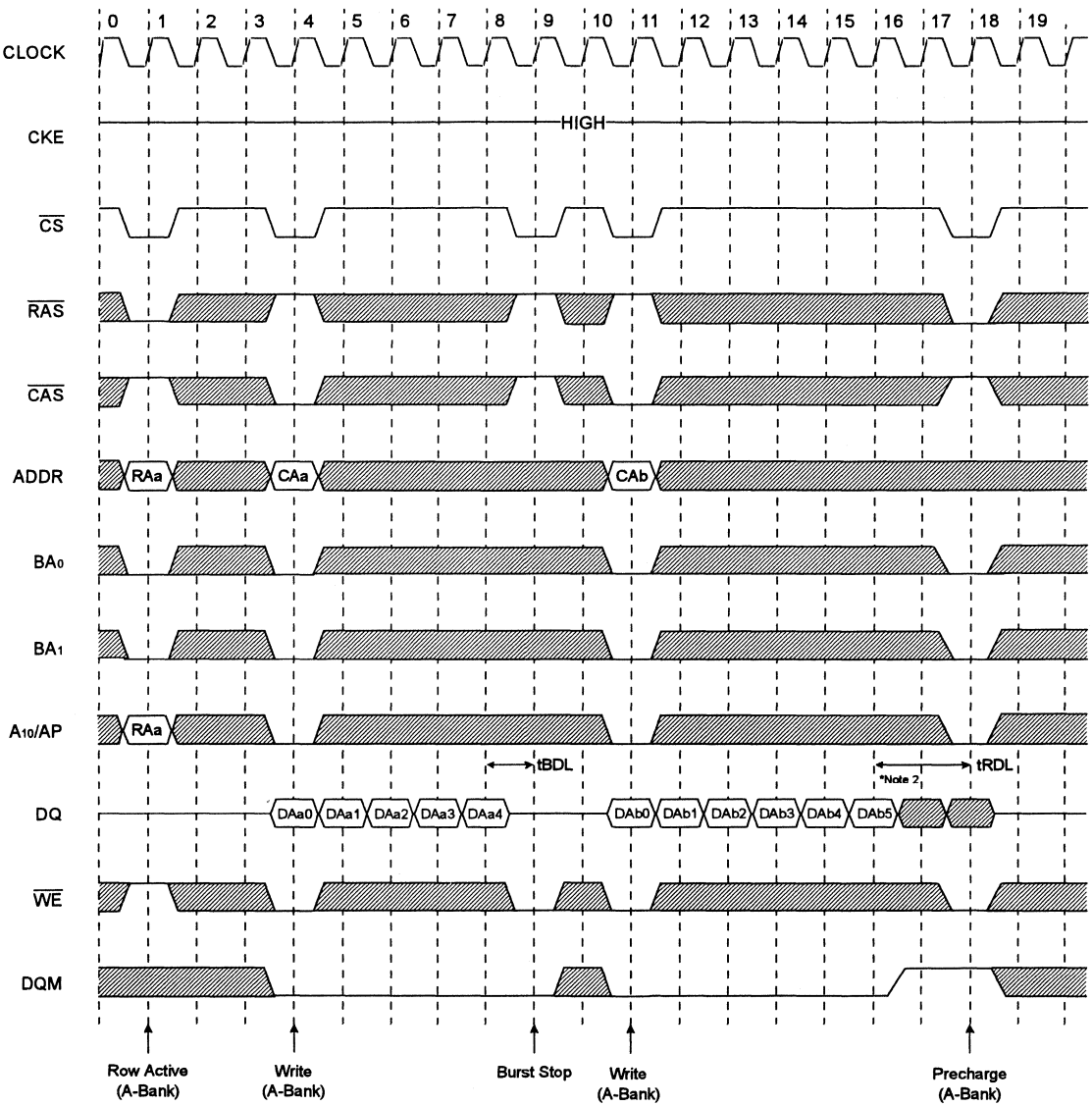


*Note : 1. At full page mode, burst is end at the end of burst. So auto precharge is possible.

2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of t_{RDL}.
DQM at write interrupted by precharge command is needed to prevent invalid write.
DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

3. Burst stop is valid at every burst length.

Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst, tRDL=2CLK

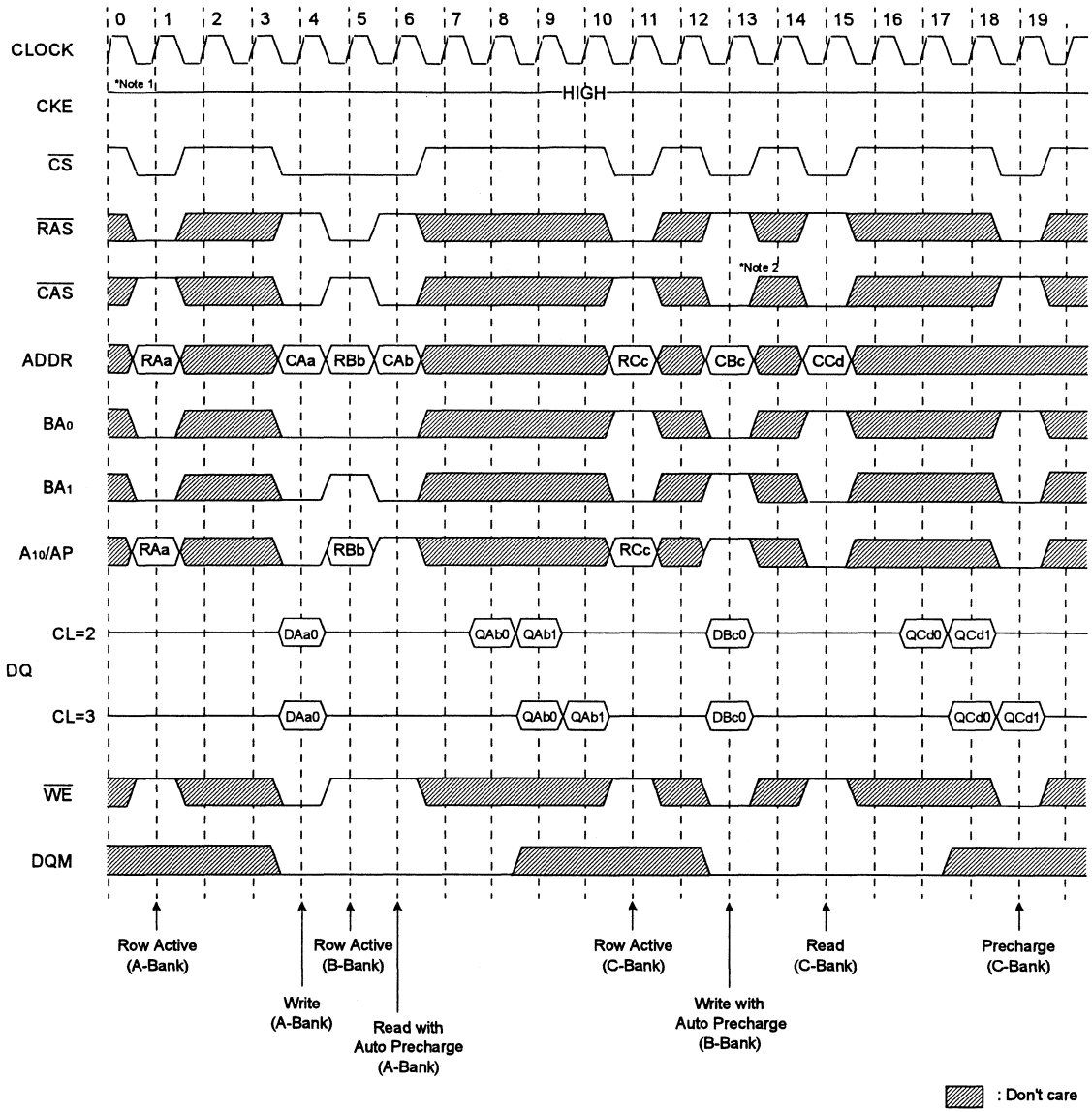


*Note : 1. At full page mode, burst is end at the end of burst. So auto precharge is possible.

2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of t_{RDL}.
DQM at write interrupted by precharge command is needed to prevent invalid write.
DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

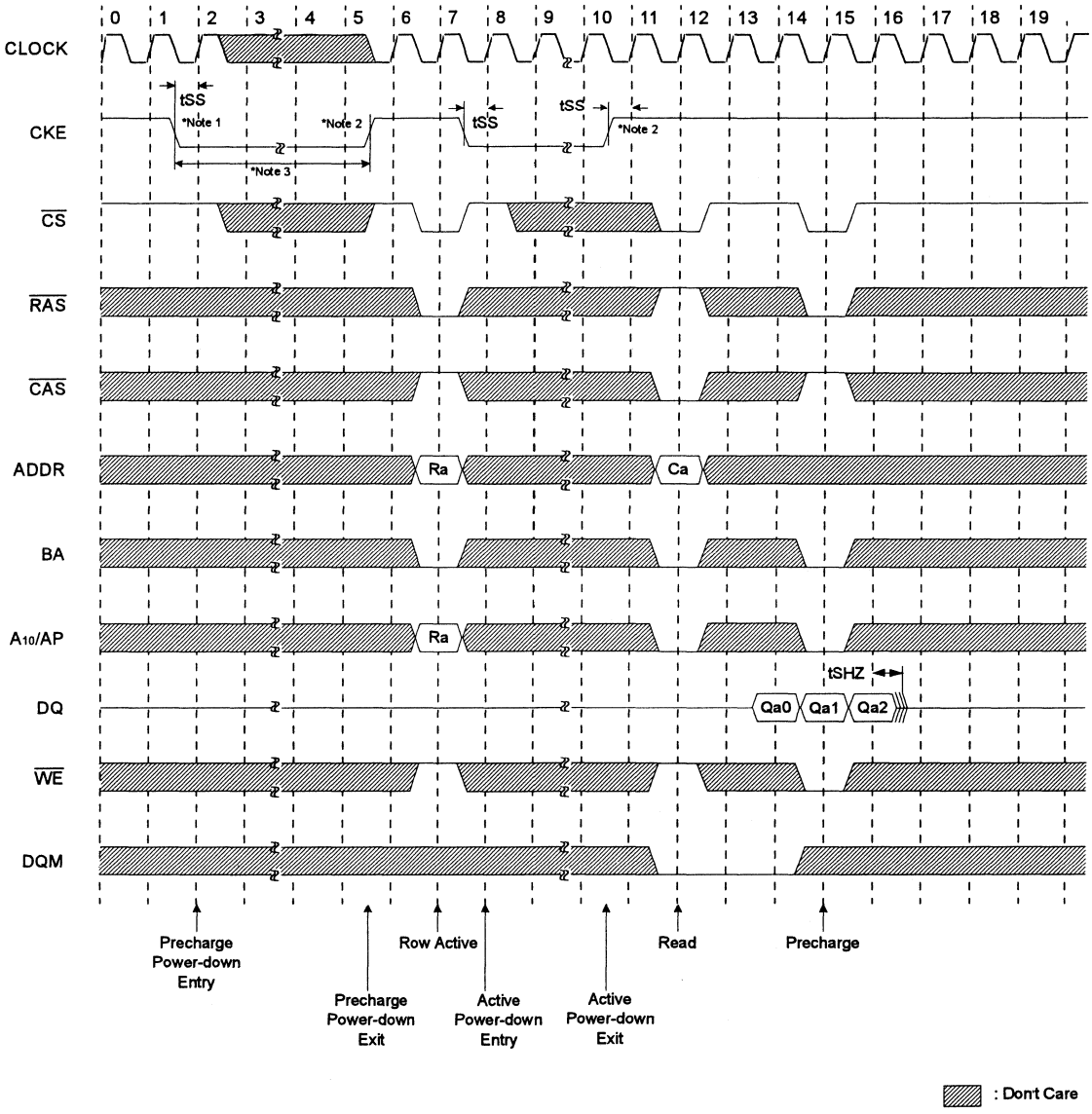
3. Burst stop is valid at every burst length.

Burst Read Single bit Write Cycle @Burst Length=2



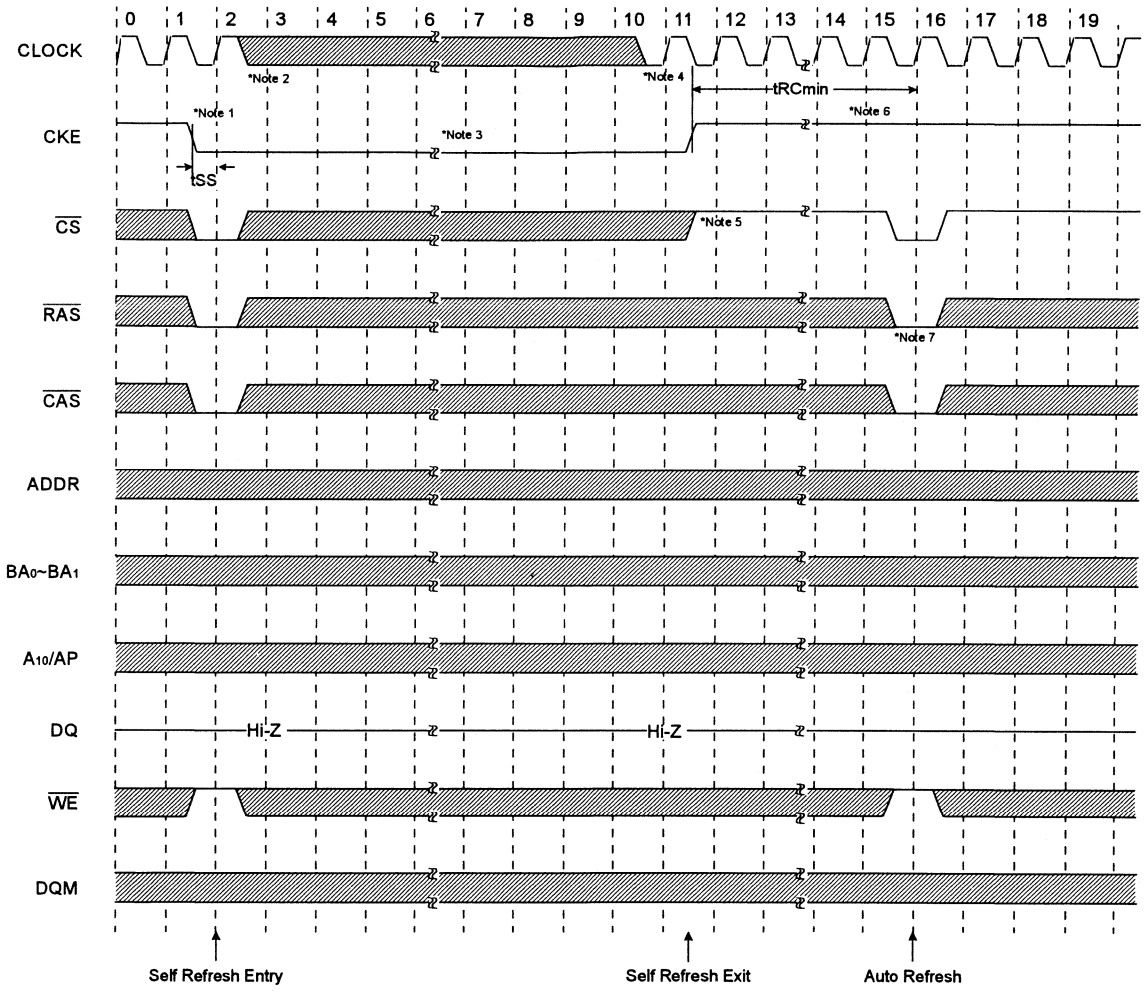
*Note : 1. BRSW modes is enabled by setting A9 "High" at MRS (Mode Register Set).
At the BRSW Mode, the burst length at write is fixed to "1" regardless of programmed burst length.
2. When BRSW write command with auto precharge is executed, keep it in mind that tRAS should not be violated.
Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command,
the next cycle starts the precharge.

Active/Precharge Power Down Mode @CAS Latency=2, Burst Length=4



*Note : 1. Both banks should be in idle state prior to entering precharge power down mode.
2. CKE should be set high at least 1CLK + tss prior to Row active command.
3. Can not violate minimum refresh specification. (64ms)

Self Refresh Entry & Exit Cycle



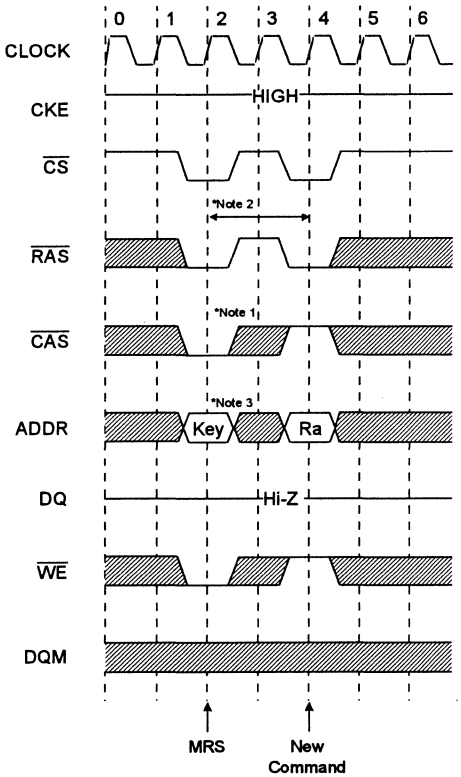
*Note : **TO ENTER SELF REFRESH MODE**

1. $\overline{CS}$, $\overline{RAS}$ & $\overline{CAS}$ with CKE should be low at the same clcok cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in self refresh mode as long as CKE stays "Low".
   cf.) Once the device enters self refresh mode, minimum t_{RAS} is required before exit from self refresh.

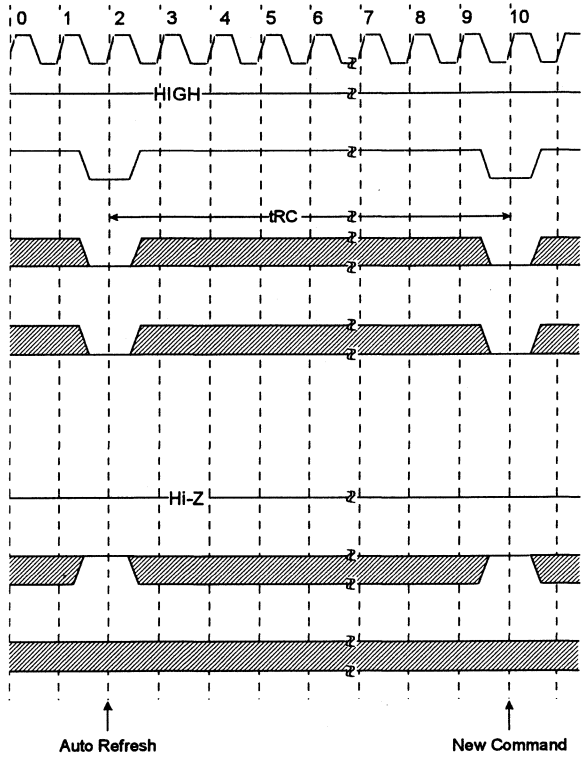
TO EXIT SELF REFRESH MODE

4. System colck restart and be stable before returning CKE high.
5. $\overline{CS}$ starts from high.
6. Minimum t_{RC} is required after CKE going high to complete self refresh exit.
7. 4K cycle(64Mb 5th, 128Mb 2nd/3rd) or 8K cycle(256Mb 2nd) of burst auto refresh is required before self refresh entry and after self refresh exit if the system uses burst refresh.

Mode Register Set Cycle



Auto Refresh Cycle

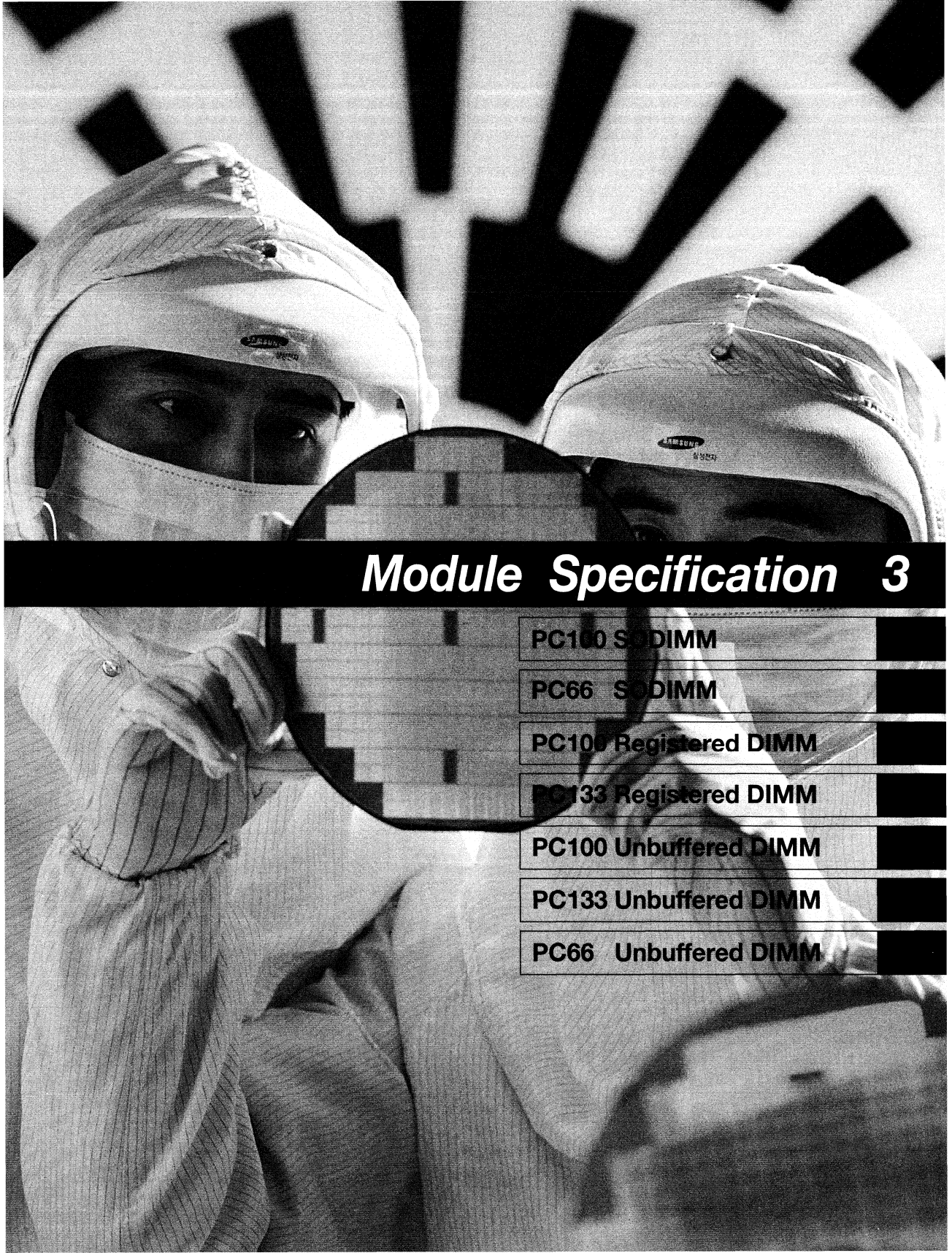


: Don't care

* All banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

MODE REGISTER SET CYCLE

*Note : 1. $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, & $\overline{WE}$ activation at the same clock cycle with address key will set internal mode register.
2. Minimum 2 clock cycles should be met before new $\overline{RAS}$ activation.
3. Please refer to Mode Register Set table.



Module Specification 3

PC100 SODIMM

PC66 SODIMM

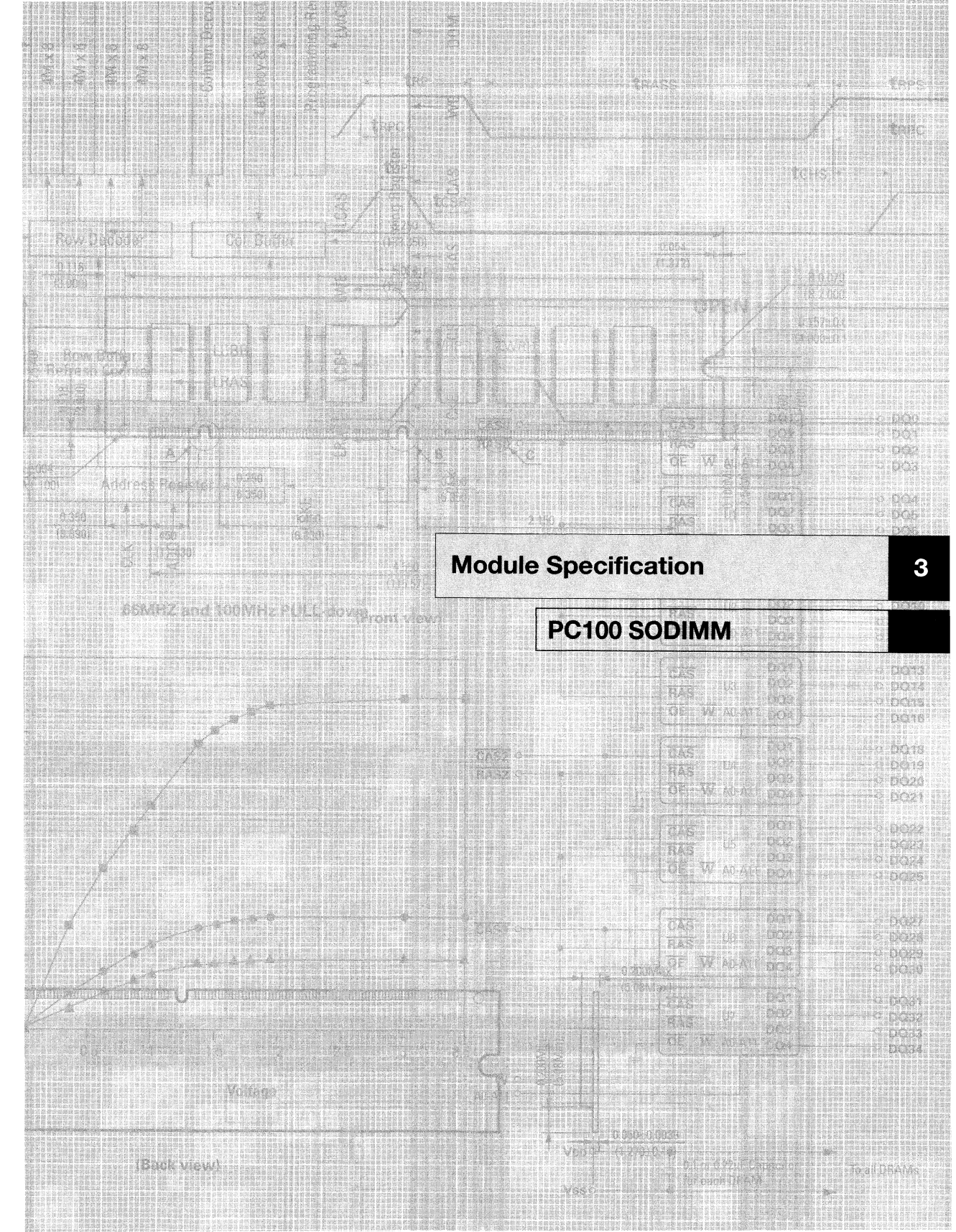
PC100 Registered DIMM

PC133 Registered DIMM

PC100 Unbuffered DIMM

PC133 Unbuffered DIMM

PC66 Unbuffered DIMM



Module Specification

3

PC100 SODIMM

M464S0424DT1 SDRAM SODIMM

4Mx64 SDRAM SODIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M464S0424DT1 is a 4M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M464S0424DT1 consists of four CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M464S0424DT1 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M464S0424DT1-L1H/C1H	100MHz (10ns @ CL=2)
M464S0424DT1-L1L/C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,000mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

1	VSS	2	VSS	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	VSS	56	VSS	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	VSS	108	VSS
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	VSS	22	VSS	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	*A12	119	VSS	120	VSS
27	VDD	28	VDD	71	*$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	*CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	VSS	76	VSS	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	VSS	36	VSS	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	VSS	140	VSS
47	DQ12	48	DQ44	91	VSS	92	VSS	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0	Clock input
CKE0	Clock enable input
$\overline{CS0}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

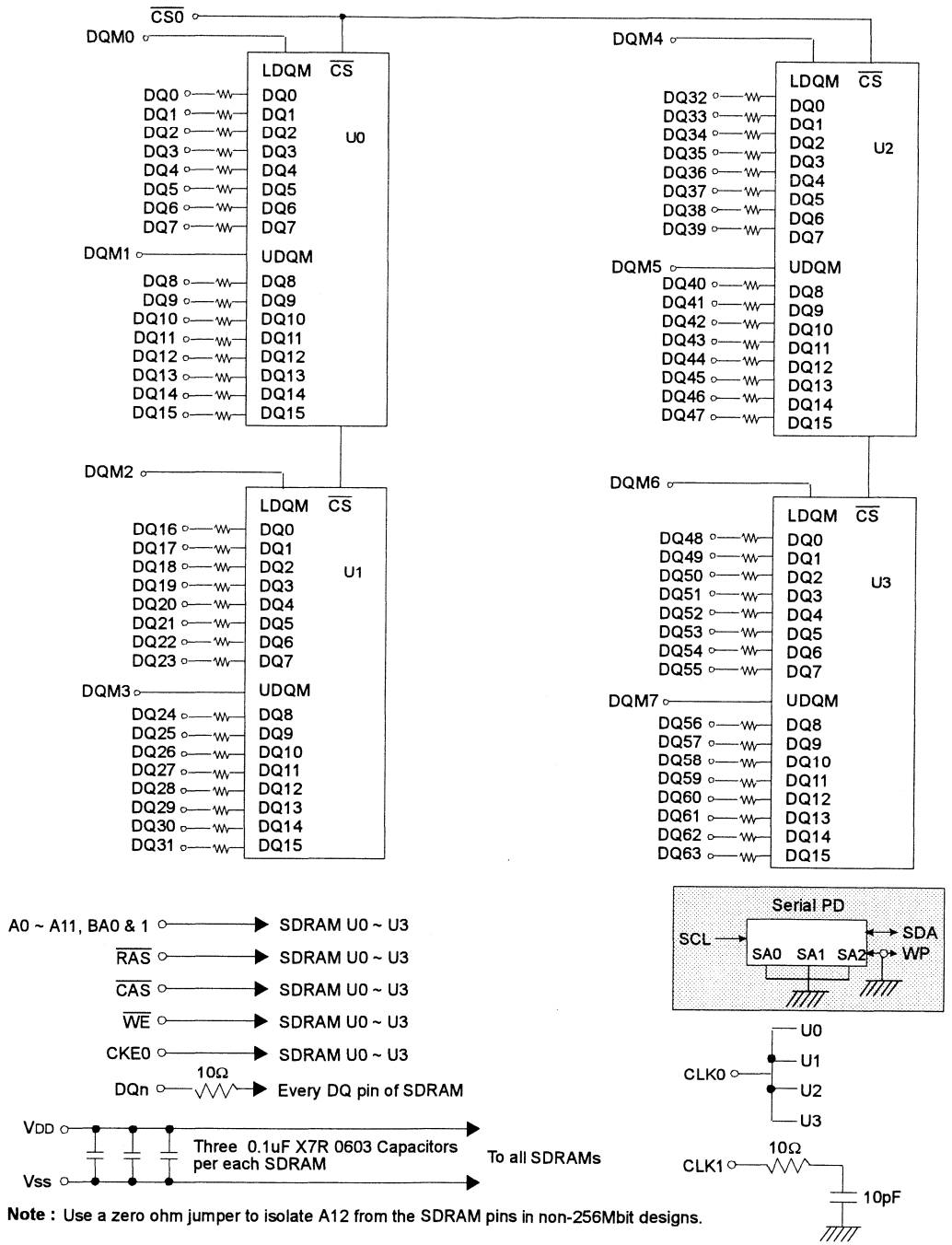
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+t_{SS} prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA7
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
$DQ_{0 \sim 63}$	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



Note : Use a zero ohm jumper to isolate A12 from the SDRAM pins in non-256Mbit designs.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	4	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC.The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	15	25	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	15	25	pF
Input capacitance (CKE0)	C_{IN3}	15	25	pF
Input capacitance (CLK0)	C_{IN4}	15	21	pF
Input capacitance ($\overline{CS0}$)	C_{IN5}	15	25	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	10	12	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	10	12	pF

DC CHARACTERISTICS

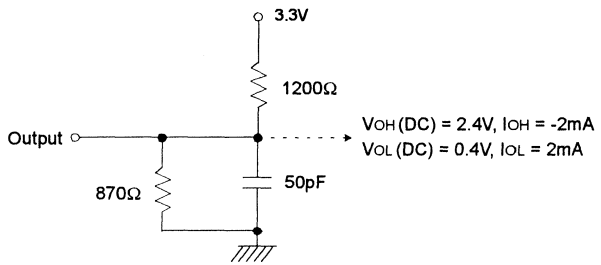
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition		Version		Unit	Note
				-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA		400		mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		4		mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} =∞		4			
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		60		mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		24			
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		12		mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} =∞		12			
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		100		mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		60		mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs		440		mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		500		mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	C	4		mA	
			L	1.6		mA	

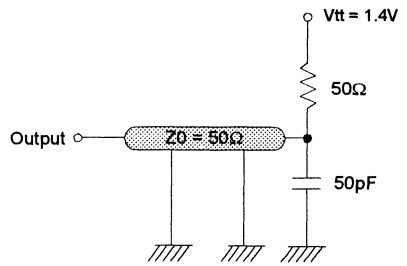
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to row precharge		tRDL(min)	2		CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns		-	5
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

Notes :
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -1H/ 1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported . SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, A_9 ~ A_0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A_0 ~ A_7)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A_0 ~ A_7)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
A_0 ~ A_{11} & BA_0 ~ BA_1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA_0 ~ BA_1 : Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

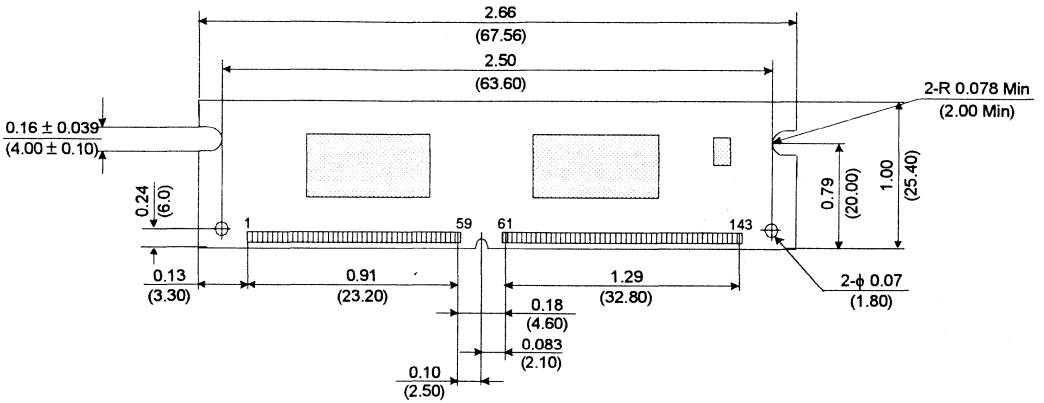
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

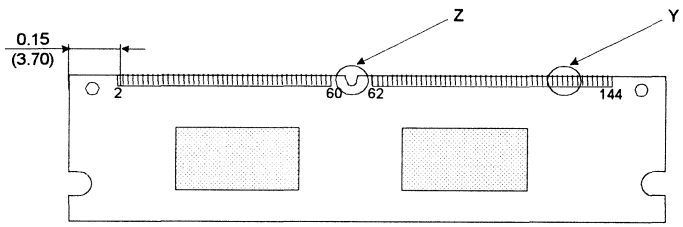
6. Burst stop command is valid at every burst length.

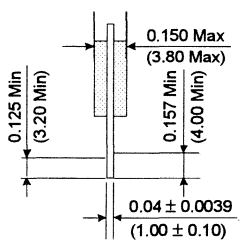
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

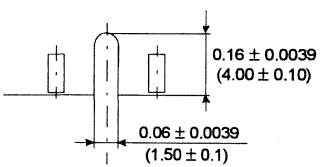
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

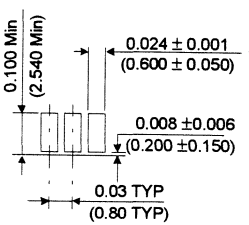








Detail Z



Detail Y

Tolerances : ± 0.006(.15) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : K4S641632D

M464S0424DT1-L1H/L1L, C1H/C1L

- Organization : 4MX64
- Composition : 4MX16 *4
- Used component part # : K4S641632D-TL1H/L1L, C1H/C1L
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,000 mil height & double sided component
- Refresh : 4K/64ms
- **Contents** :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	8		08h		1
5	# of module Rows on this assembly	1 Row		01h		
6	Data width of this assembly	64 bits		40h		
7	..... Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	Non parity		00h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x16		10h		
14	Error checking SDRAM width	None		00h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing		00h		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	1 Row of 32MB		08h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		04h	34h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	..... Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	4		34h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	..... Manufacturer part # (Data bits)	6		36h		
77	..... Manufacturer part # (Data bits)	4		34h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	Blank		20h		
80	..... Manufacturer part # (Module depth)	4		34h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	D		44h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	1		31h		
86	Manufacturer part # (Hyphen)	"-"		2Dh		
87	Manufacturer part # (Power)	L / C		4Ch / 43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	1		31h		
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)		44h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M464S0824DT1 SDRAM SODIMM

8Mx64 SDRAM SODIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M464S0824DT1 is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M464S0824DT1 consists of eight CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M464S0824DT1 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M464S0824DT1-L1H/C1H	100MHz (10ns @ CL=2)
M464S0824DT1-L1L/C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,250mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

1	VSS	2	VSS	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	VSS	56	VSS	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD					105	A8	106	BA0
13	DQ4	14	DQ36		Voltage Key			107	VSS	108	VSS
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	VSS	22	VSS	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	*A12	119	VSS	120	VSS
27	VDD	28	VDD	71	$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	VSS	76	VSS	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	VSS	36	VSS	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	VSS	140	VSS
47	DQ12	48	DQ44	91	VSS	92	VSS	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0 ~ CKE1	Clock enable input
$\overline{CS0}$ ~ $\overline{CS1}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

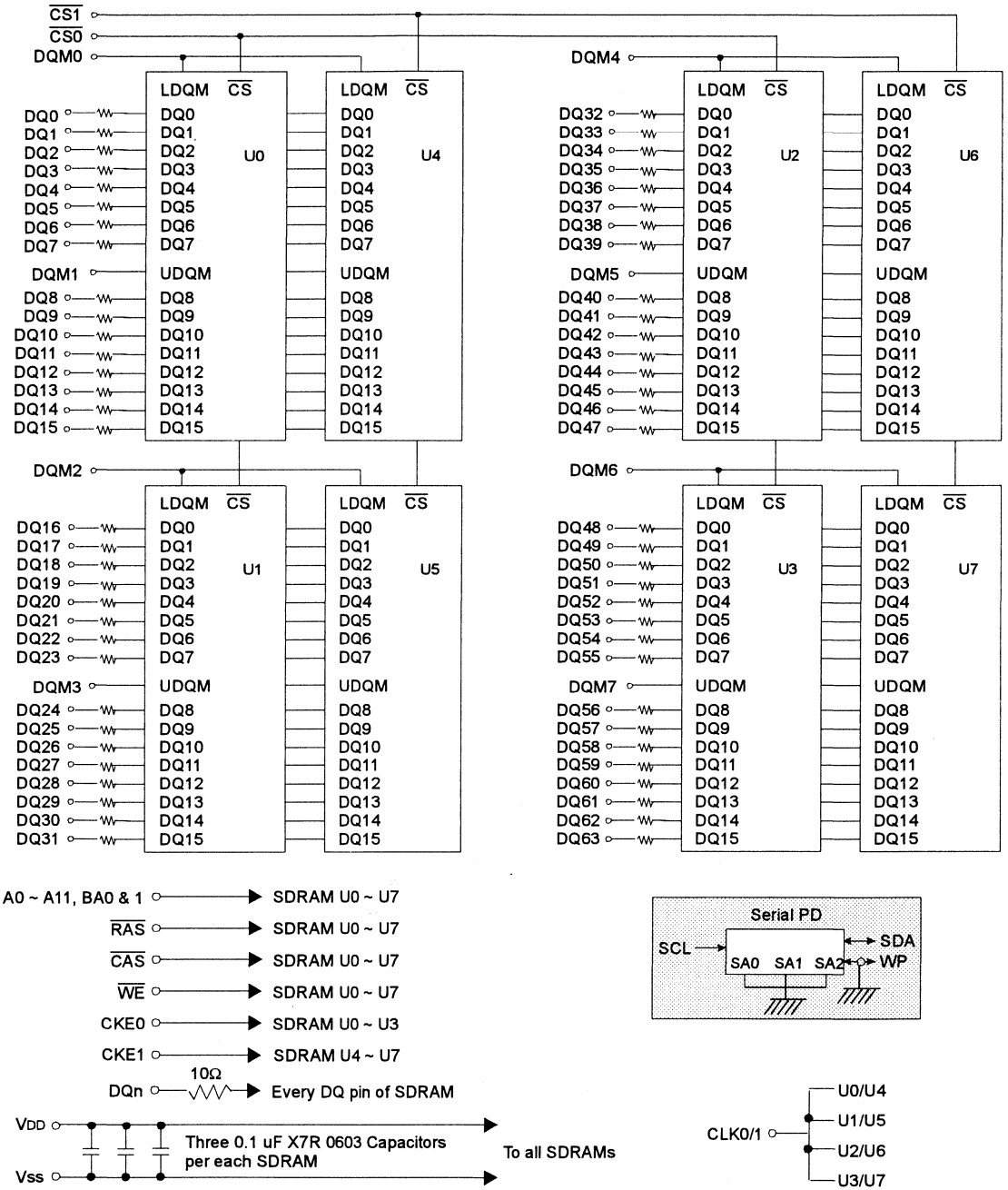
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+t_{SS} prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA7
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
$DQ_{0 \sim 63}$	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



Note : Use a zero ohm jumper to isolate A12 from the SDRAM pins in non-256Mbit designs.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC.The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	25	45	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	25	45	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	15	25	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	15	21	pF
Input capacitance ($\overline{CS0}$ ~ $\overline{CS1}$)	C_{IN5}	15	25	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	10	12	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	10	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition		Version		Unit	Note
				-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA		500		mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		8		mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} =∞		8			
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		120		mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		48			
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		24		mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} =∞		24			
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		200		mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		120		mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs		540		mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		600		mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	C	8		mA	
			L	3.2		mA	

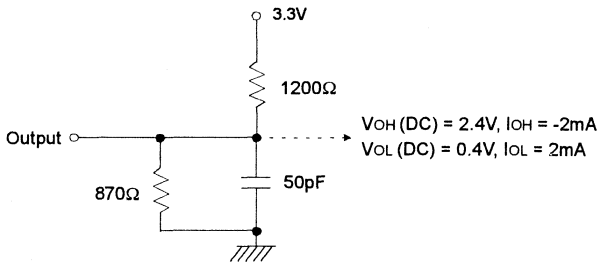
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

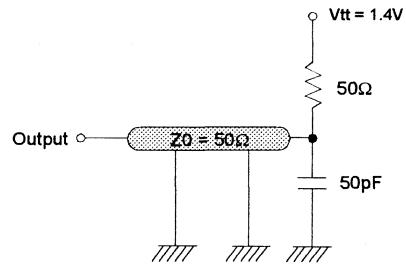
3. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to row precharge		tRDL(min)	2		CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns		-	5
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

Notes :
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -1H/ 1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
   SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

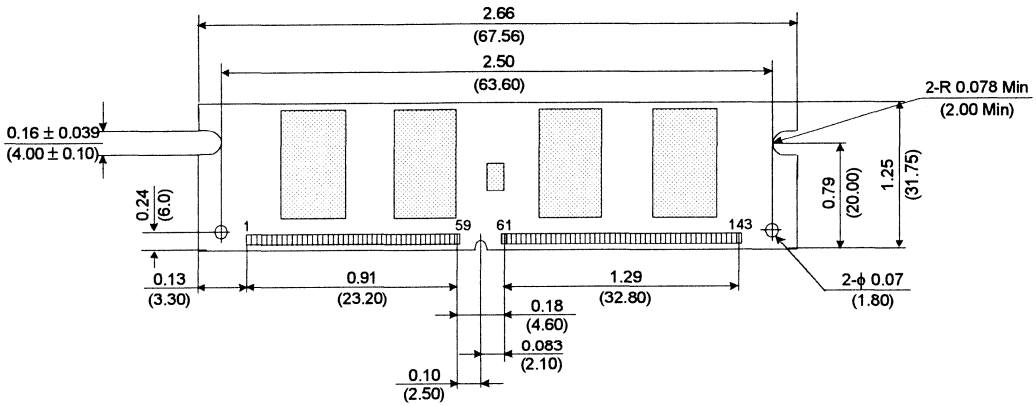
Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A7)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A7)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

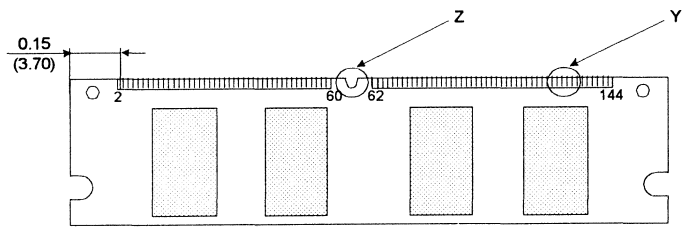
(V=Valid, X=Don't care, H=Logic high, L=Logic low)

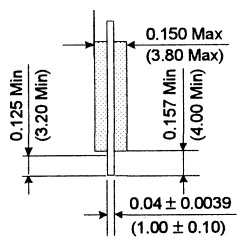
Notes : 1. OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

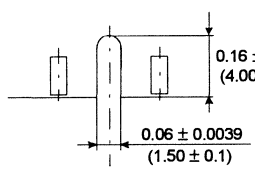
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

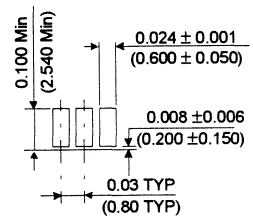








Detail Z



Detail Y

Tolerances : ±.006(.15) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : K4S641632D

M464S0824DT1-L1H/L1L, C1H/C1L

- Organization : 8MX64
- Composition : 4MX16 *8
- Used component part # : K4S641632D-TL1H/L1L, C1H/C1L
- # of rows in module : 2 rows
- # of banks in component : 4 banks
- Feature : 1,250 mil height & double sided component
- Refresh : 4K/64ms
- **Contents** :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	8		08h		1
5	# of module Rows on this assembly	2 Rows		02h		
6	Data width of this assembly	64 bits		40h		
7	..... Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	Non parity		00h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x16		10h		
14	Error checking SDRAM width	None		00h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing		00h		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	2 Rows of 32MB		08h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		05h	35h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	..... Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	4		34h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	..... Manufacturer part # (Data bits)	6		36h		
77	..... Manufacturer part # (Data bits)	4		34h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	0		30h		
80	..... Manufacturer part # (Module depth)	8		38h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	D		44h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	1		31h		
86	Manufacturer part # (Hyphen)	"-"		2Dh		
87	Manufacturer part # (Power)	L / C		4Ch / 43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	1		31h		
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)		44h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		CFh	CDh	
128+	Unused storage locations	Undefined		-		5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M464S0424CT1 SDRAM SODIMM

4Mx64 SDRAM SODIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M464S0424CT1 is a 4M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M464S0424CT1 consists of four CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M464S0424CT1 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M464S0424CT1-L1H	100MHz (10ns @ CL=2)
M464S0424CT1-L1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,000mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

1	VSS	2	VSS	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	VSS	56	VSS	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	VSS	108	VSS
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	VSS	22	VSS	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	*A12	119	VSS	120	VSS
27	VDD	28	VDD	71	*$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	*CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	VSS	76	VSS	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	VSS	36	VSS	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	VSS	140	VSS
47	DQ12	48	DQ44	91	VSS	92	VSS	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0	Clock input
CKE0	Clock enable input
$\overline{CS0}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

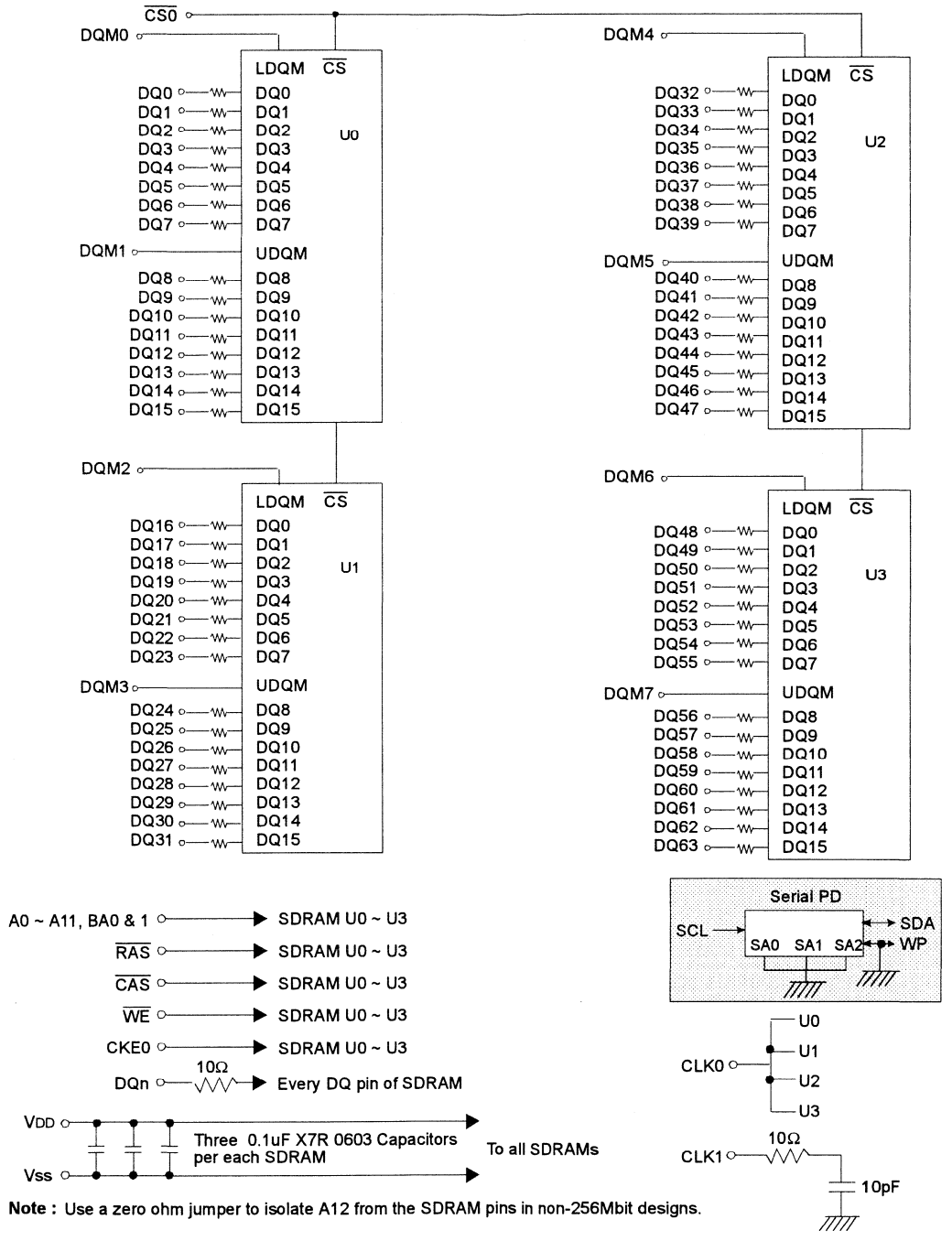
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+t_{SS} prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA7
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
$DQ_{0 \sim 63}$	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



Note : Use a zero ohm jumper to isolate A12 from the SDRAM pins in non-256Mbit designs.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	4	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-4	-	4	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC.The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	20	30	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	20	30	pF
Input capacitance (CKE0)	C_{IN3}	20	30	pF
Input capacitance (CLK0)	C_{IN4}	20	26	pF
Input capacitance ($\overline{CS0}$)	C_{IN5}	20	30	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	12	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	14	17	pF

DC CHARACTERISTICS

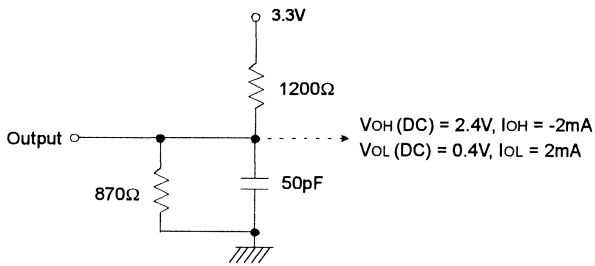
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -1H	Version -1L	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		280	280	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		4		mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} =∞		4			
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		48		mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		24			
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		8		mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} =∞		8			
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		80		mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		40		mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	360	360	mA	1
			2	360	340		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		500		mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		1.8		mA	

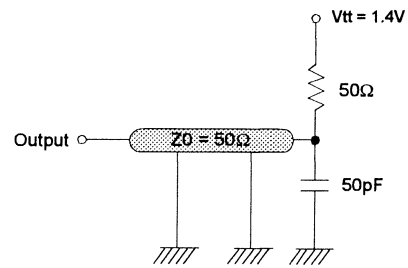
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to row precharge		tRDL(min)	1		CLK	2
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

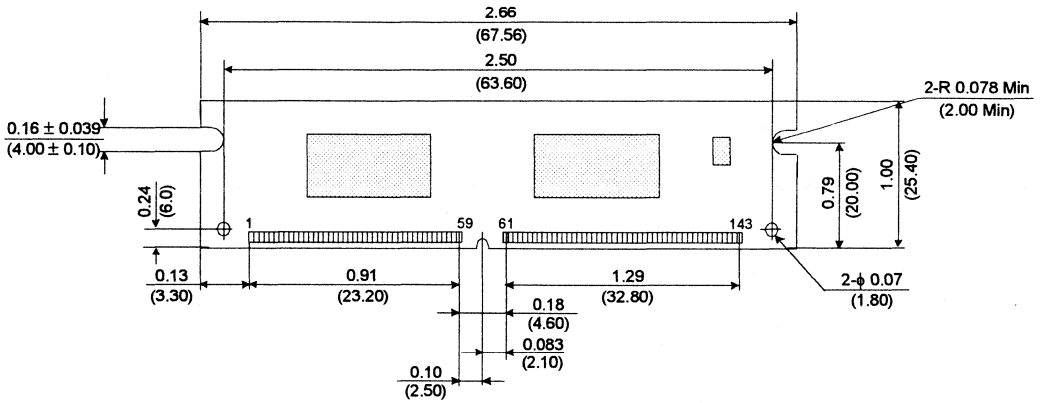
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

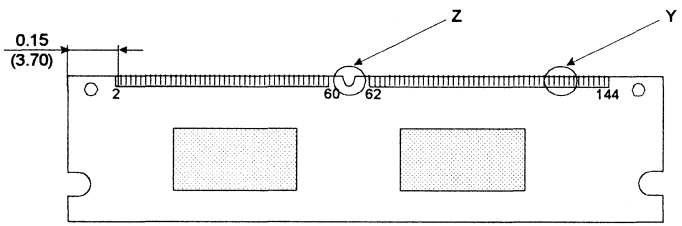
6. Burst stop command is valid at every burst length.

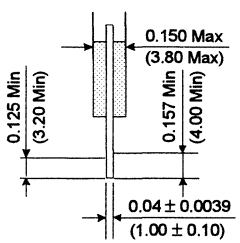
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

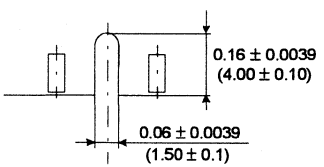
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

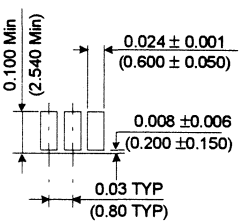








Detail Z



Detail Y

Tolerances : ± 0.006(.15) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : K4S641632C

M464S0424CT1-L1H/L1L

- Organization : 4MX64
- Composition : 4MX16 *4
- Used component part # : K4S641632C-TL1H/L1L
- # of banks in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,000 mil height & double sided component
- Refresh : 4K/64ms
- **Contents** :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	8		08h		1
5	# of module Rows on this assembly	1 Row		01h		
6	Data width of this assembly	64 bits		40h		
7	..... Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	Non parity		00h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x16		10h		
14	Error checking SDRAM width	None		00h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing		00h		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	1 Row of 32MB		08h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		04h	34h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	..... Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	4		34h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	..... Manufacturer part # (Data bits)	6		36h		
77	..... Manufacturer part # (Data bits)	4		34h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	0		30h		
80	..... Manufacturer part # (Module depth)	4		34h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	C		43h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	1		31h		
86	Manufacturer part # (Hyphen)	"-"		2Dh		
87	Manufacturer part # (Power)	L		4Ch		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	1		31h		
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)		43h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M464S0824CT1 SDRAM SODIMM

8Mx64 SDRAM SODIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M464S0824CT1 is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M464S0824CT1 consists of eight CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M464S0824CT1 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M464S0824CT1-L1H	100MHz (10ns @ CL=2)
M464S0824CT1-L1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,250mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

1	VSS	2	VSS	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	VSS	56	VSS	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	VSS	108	VSS
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	VSS	22	VSS	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	*A12	119	VSS	120	VSS
27	VDD	28	VDD	71	$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	VSS	76	VSS	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	VSS	36	VSS	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	VSS	140	VSS
47	DQ12	48	DQ44	91	VSS	92	VSS	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0 ~ CKE1	Clock enable input
$\overline{CS0}$ ~ $\overline{CS1}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

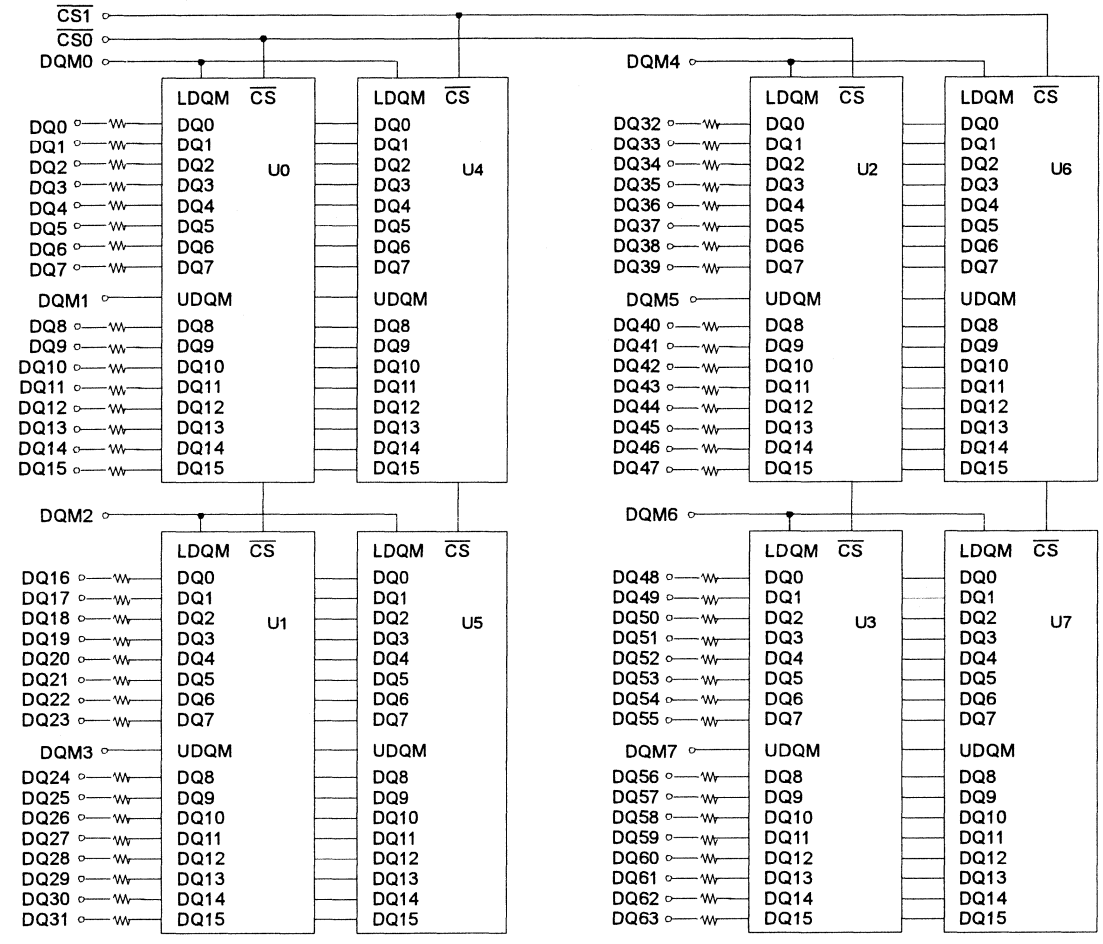
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA7
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



Note : Use a zero ohm jumper to isolate A12 from the SDRAM pins in non-256Mbit designs.

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-8	-	8	uA	3
Input leakage current (I/O pins)	I_{IL}	-3	-	3	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC.The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	30	50	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	30	50	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	20	30	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	20	26	pF
Input capacitance ($\overline{CS0}$ ~ $\overline{CS1}$)	C_{IN5}	20	30	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	15	20	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	18	23	pF

DC CHARACTERISTICS

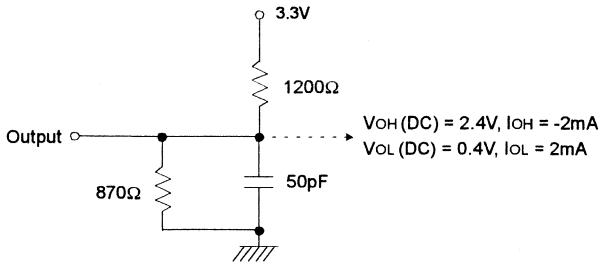
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -1H	Version -1L	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		360	360	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		8		mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} =∞		8			
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		96		mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		48			
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		16		mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} =∞		16			
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		160		mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		80		mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	440	440	mA	1
			2	440	420		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1000		mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		3.6		mA	

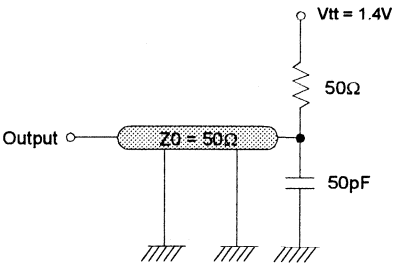
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to row precharge		tRDL(min)	1		CLK	2
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

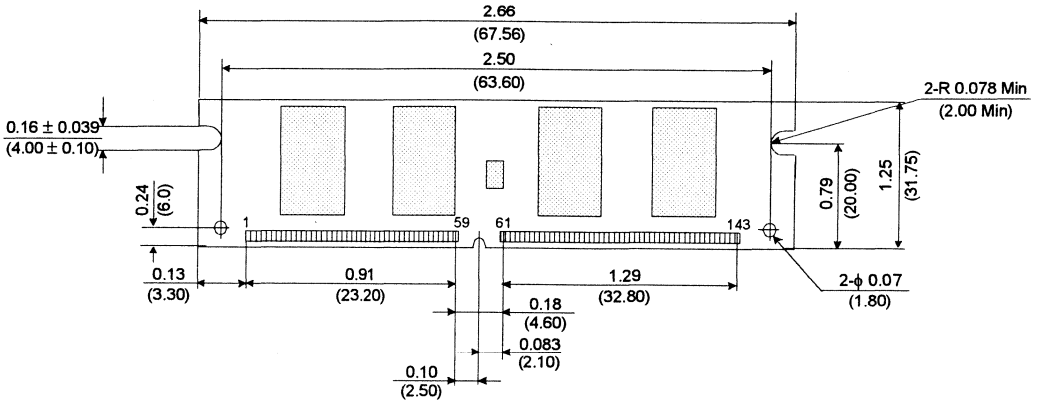
Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

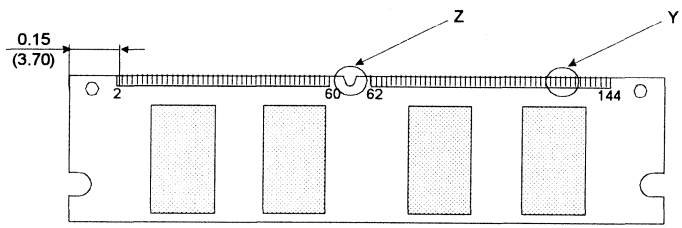
(V=Valid, X=Don't care, H=Logic high, L=Logic low)

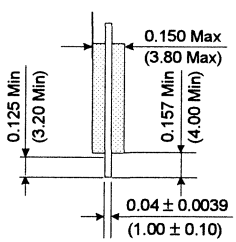
Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

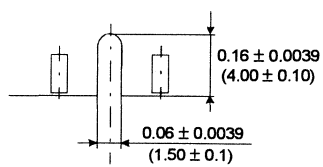
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

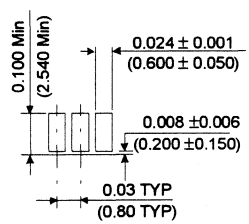








Detail Z



Detail Y

Tolerances : ±.006(.15) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : K4S641632C

M464S0824CT1-L1H/L1L

- Organization : 8MX64
- Composition : 4MX16 *8
- Used component part # : K4S641632C-TL1H/L1L
- # of banks in module : 2 rows
- # of banks in component : 4 banks
- Feature : 1,250 mil height & double sided component
- Refresh : 4K/64ms
- **Contents** :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	8		08h		1
5	# of module Rows on this assembly	2 Rows		02h		
6	Data width of this assembly	64 bits		40h		
7	..... Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	Non parity		00h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x16		10h		
14	Error checking SDRAM width	None		00h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing		00h		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	2 Rows of 32MB		08h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

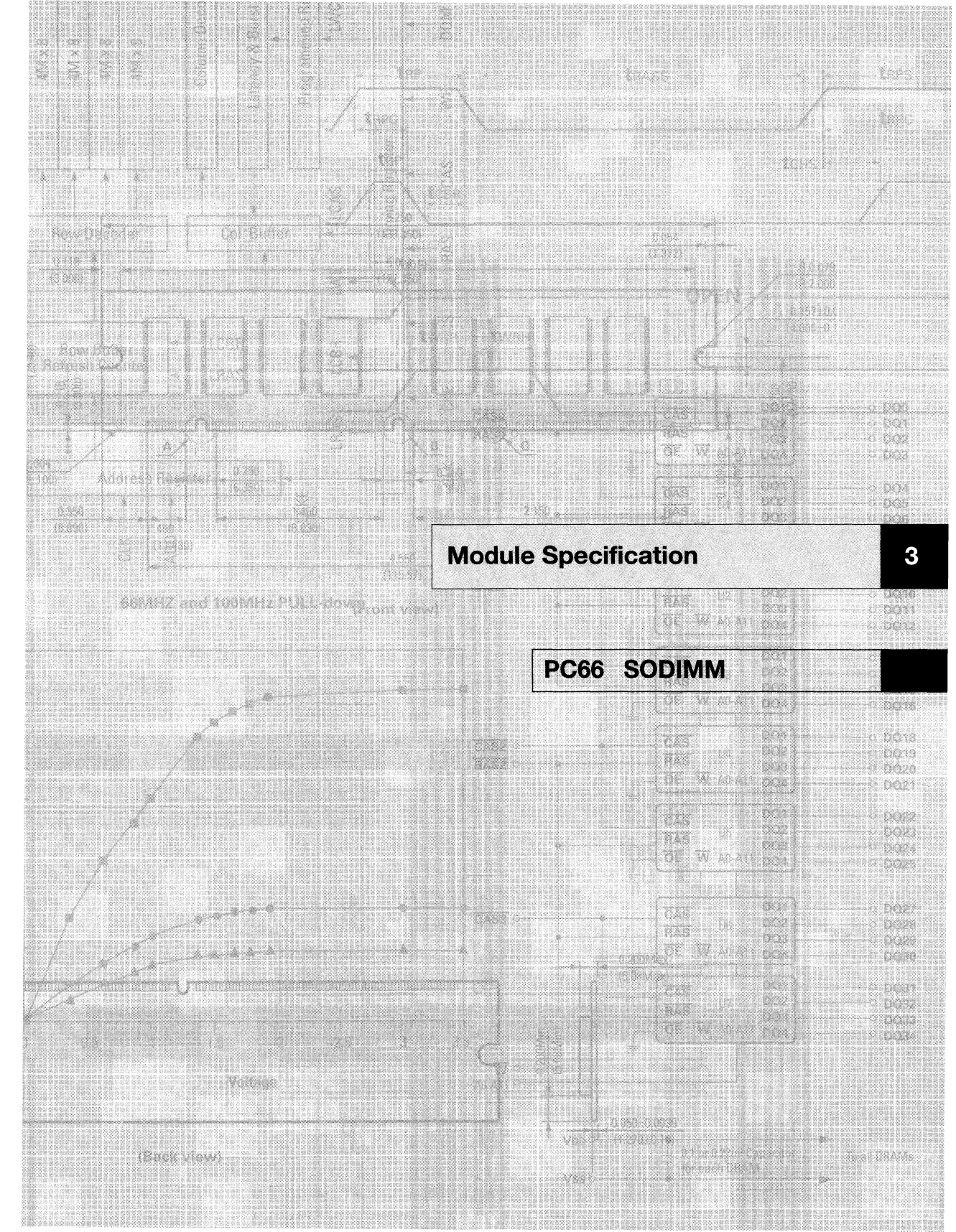
SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		05h	35h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	..... Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	4		34h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	..... Manufacturer part # (Data bits)	6		36h		
77	..... Manufacturer part # (Data bits)	4		34h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	0		30h		
80	..... Manufacturer part # (Module depth)	8		38h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	C		43h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	1		31h		
86	Manufacturer part # (Hyphen)	"-"		2Dh		
87	Manufacturer part # (Power)	L		4Ch		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	1		31h		
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)		43h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		CFh	CDh	
128+	Unused storage locations	Undefined		-		5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

Module Specification 3

PC66 SODIMM



M466S0424DT0 SDRAM SODIMM

4Mx64 SDRAM SODIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M466S0424DT0 is a 4M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M466S0424DT0 consists of four CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M466S0424DT0 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M466S0424DT0-L10/C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,000mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

1	VSS	2	VSS	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	VSS	56	VSS	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	VSS	108	VSS
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	VSS	22	VSS	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	*A12	119	VSS	120	VSS
27	VDD	28	VDD	71	*$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	*CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	VSS	76	VSS	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	VSS	36	VSS	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	VSS	140	VSS
47	DQ12	48	DQ44	91	VSS	92	VSS	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0	Clock input
CKE0	Clock enable input
$\overline{CS0}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

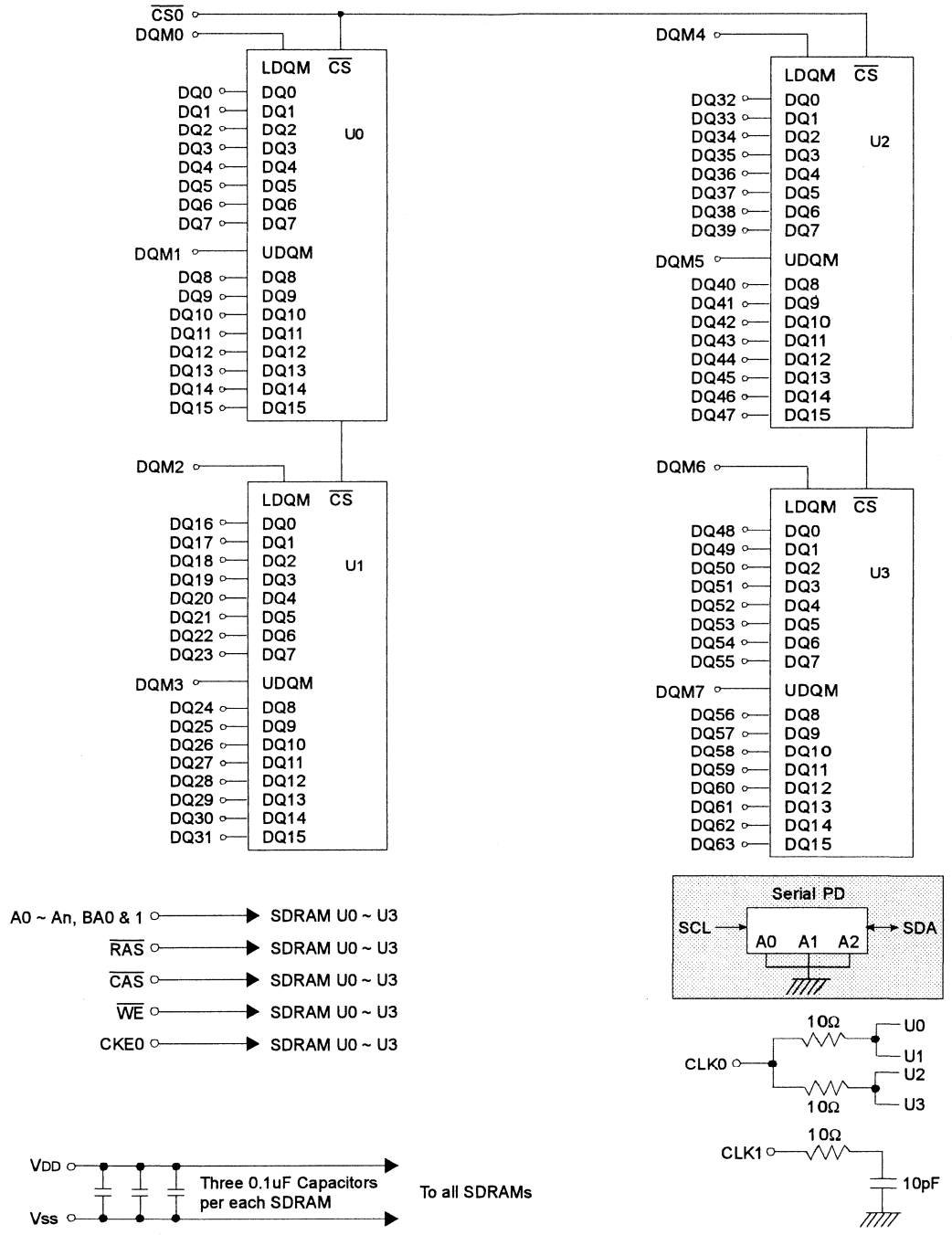
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA7
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	4	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC.The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	15	25	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	15	25	pF
Input capacitance (CKE0)	C_{IN3}	15	25	pF
Input capacitance (CLK0)	C_{IN4}	10	13	pF
Input capacitance ($\overline{CS0}$)	C_{IN5}	10	15	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	8	10	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	9	12	pF

DC CHARACTERISTICS

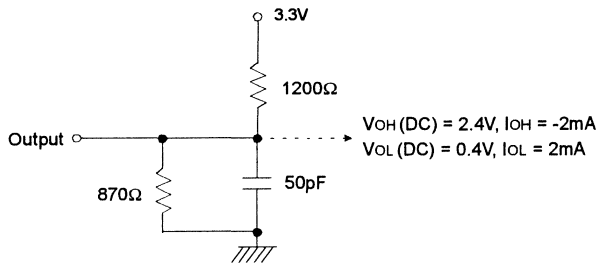
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition		Version -10	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA		400	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		4	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} =∞		4		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		60	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		24		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		12	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} =∞		12		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		100	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		60	mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs		440	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		500	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	C	4		
			L	1.6	mA	

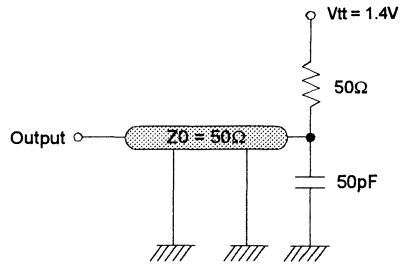
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
Row cycle time		tRAS(max)	100	us	
		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	2	CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20ns	-	5
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -10, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tSAC		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	tOH	3		ns	2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tSS	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A7)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A7)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

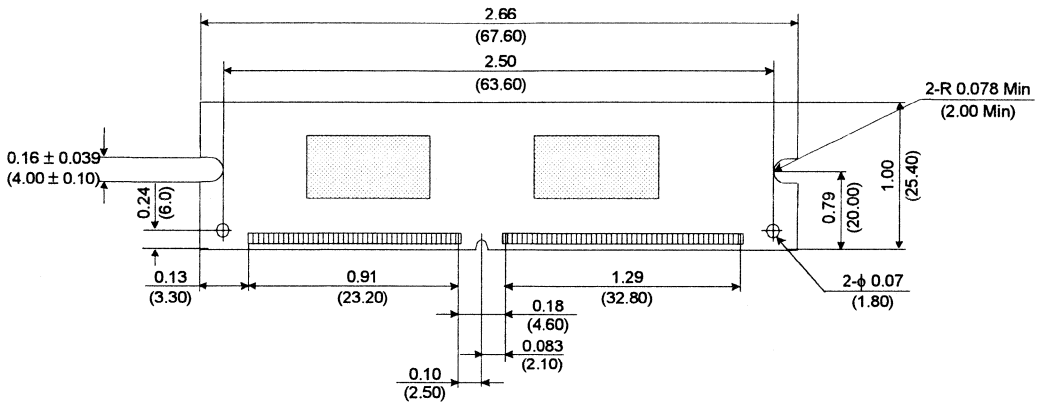
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

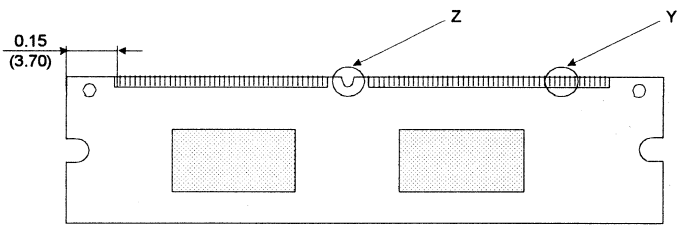
6. Burst stop command is valid at every burst length.

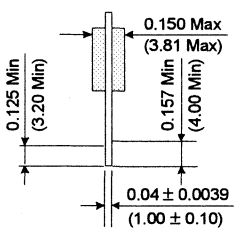
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

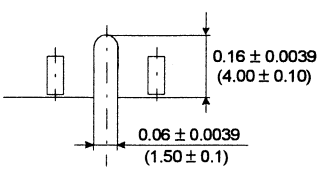
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

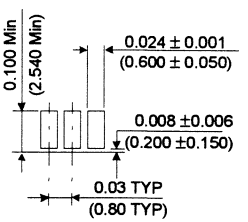








Detail Z



Detail Y

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : K4S641632D

M466S0424DT0-L10, C10

- Organization : 4Mx64
- Composition : 4Mx16 *4
- Used component part # : K4S641632D-TL10, C10
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	8	08h	1
5	# of module banks on this assembly	1 bank	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	1 bank of 32MB	08h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	EBh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	4	34h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	D	44h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	0	30h	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	L / C	4Ch / 43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	0	30h	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M466S0823DT2 SDRAM SODIMM

8Mx64 SDRAM SODIMM based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M466S0823DT2 is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M466S0823DT2 consists of eight CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M466S0823DT2 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M466S0823DT2-L10/C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,150mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

1	VSS	2	VSS	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	VSS	56	VSS	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	VSS	108	VSS
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	VSS	22	VSS	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	*A12	119	VSS	120	VSS
27	VDD	28	VDD	71	*$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	VSS	76	VSS	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	VSS	36	VSS	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	VSS	140	VSS
47	DQ12	48	DQ44	91	VSS	92	VSS	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0	Clock enable input
$\overline{CS0}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

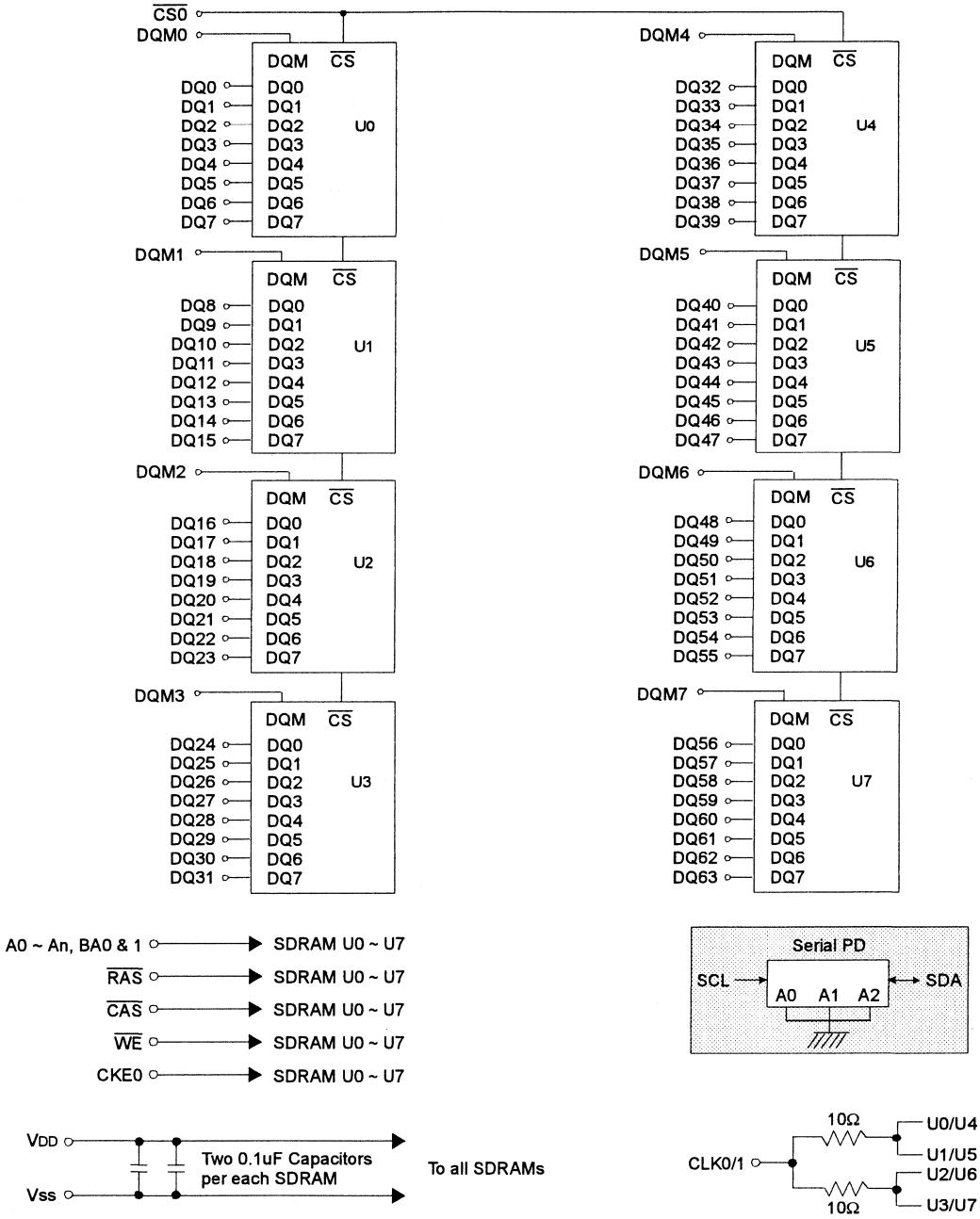
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SAMSUNG ELECTRONICS

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC.The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	23	40	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	23	40	pF
Input capacitance (CKE0)	C_{IN3}	23	40	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	15	21	pF
Input capacitance ($\overline{CS0}$)	C_{IN5}	25	45	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	8	10	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	9	12	pF

DC CHARACTERISTICS

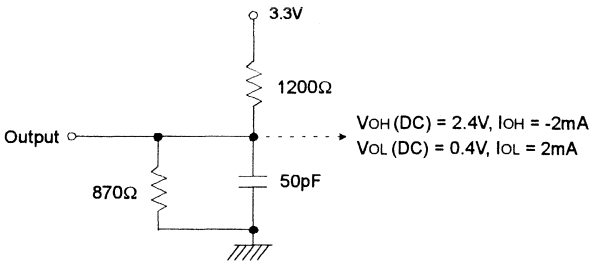
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition		Version -10	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA		560	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		8	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		8		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		120	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		48		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		24	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		24		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		200	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		120	mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs		760	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,000	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	C	8	mA	
			L	3.2	mA	

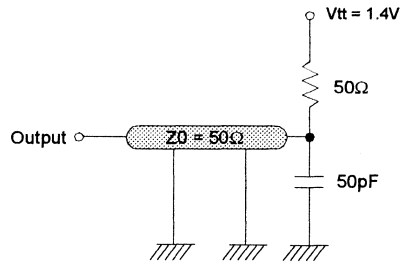
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
Row cycle time		tRAS(max)	100	us	
		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	2	CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20ns	-	5
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -10, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tSAC		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	tOH	3		ns	2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tSS	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

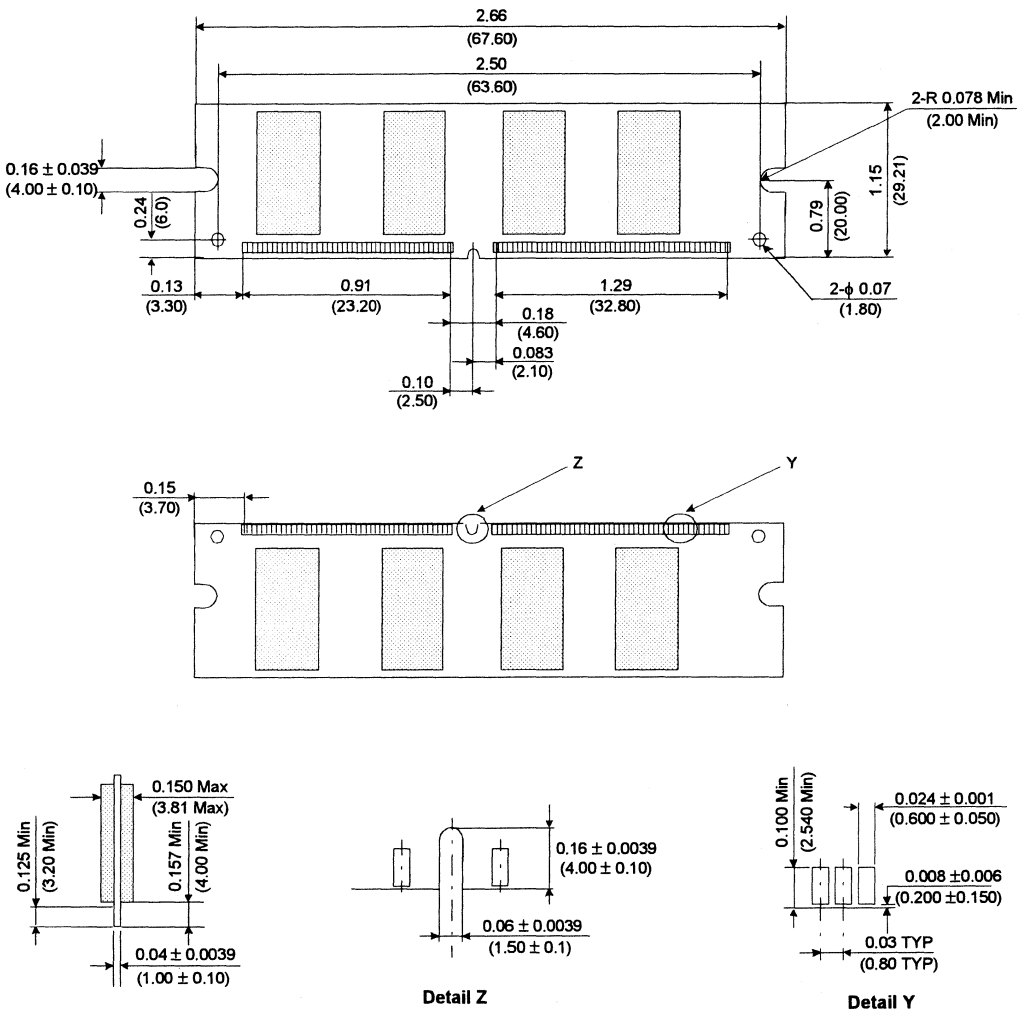
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832D

M466S0823DT2-L10, C10

- Organization : 8Mx64
- Composition : 8Mx8 *8
- Used component part # : K4S640832D-TL10, C10
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,150mil height & double sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module banks on this assembly	1 bank	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	Non.parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	1 bank of 64MB	10h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	ECh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	8	38h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	D	44h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	L / C	4Ch / 43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M466S0823DT3 SDRAM SODIMM

8Mx64 SDRAM SODIMM based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M466S0823DT3 is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M466S0823DT3 consists of eight CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M466S0823DT3 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M466S0823DT3-L10/C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,050mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

1	VSS	2	VSS	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	VSS	56	VSS	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD					105	A8	106	BA0
13	DQ4	14	DQ36		Voltage Key			107	VSS	108	VSS
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	VSS	22	VSS	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	*A12	119	VSS	120	VSS
27	VDD	28	VDD	71	*$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	VSS	76	VSS	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	VSS	36	VSS	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	VSS	140	VSS
47	DQ12	48	DQ44	91	VSS	92	VSS	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0	Clock enable input
$\overline{CS0}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

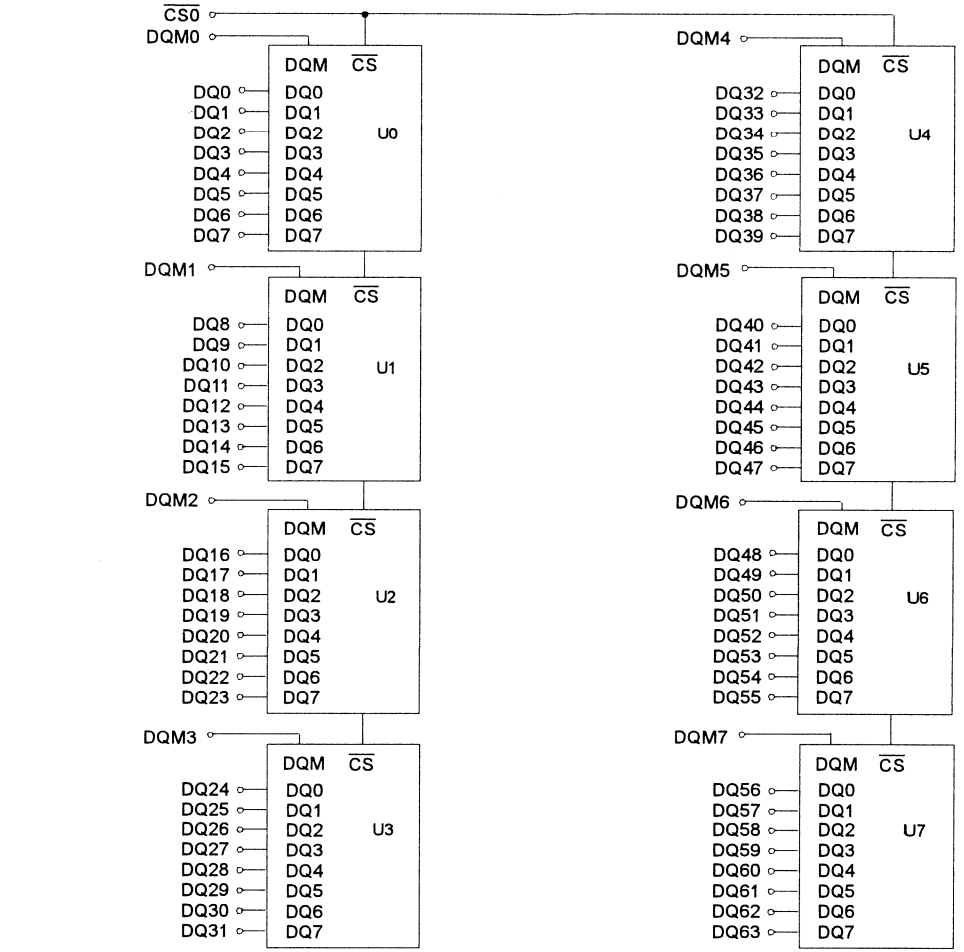
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

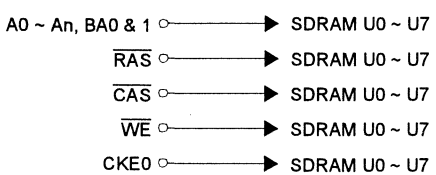
SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

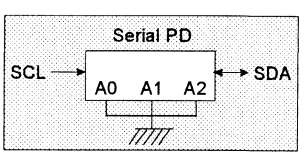
PIN CONFIGURATION DESCRIPTION

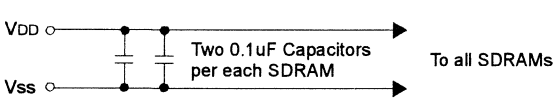
Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
$DQ_{0 \sim 63}$	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.

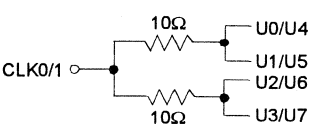
FUNCTIONAL BLOCK DIAGRAM











ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC.The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	23	40	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	23	40	pF
Input capacitance (CKE0)	C_{IN3}	23	40	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	15	21	pF
Input capacitance ($\overline{CS0}$)	C_{IN5}	25	45	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	8	10	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	9	12	pF

DC CHARACTERISTICS

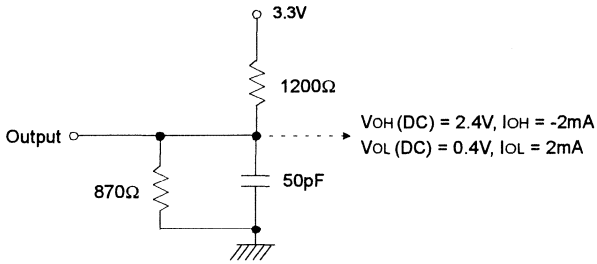
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition		Version -10	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA		560	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		8	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		8		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		120	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		48		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		24	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		24		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		200	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		120	mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs		760	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,000	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	C	8	mA	
			L	3.2	mA	

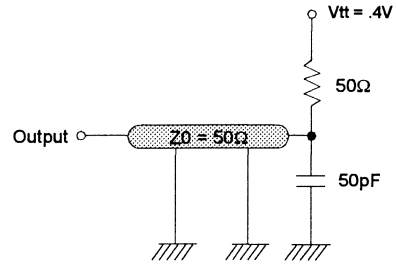
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
Row cycle time		tRAS(max)	100	us	
		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	2	CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20ns	-	5
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -10, tRDL=1CLK and tDAL=1CLK + 20ns is also supported .
SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tSAC		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	tOH	3		ns	2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tSS	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

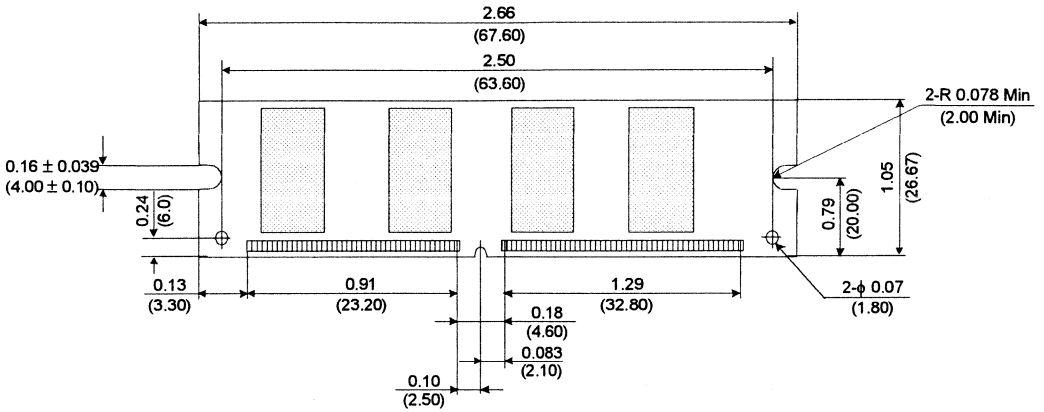
Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A8)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A8)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

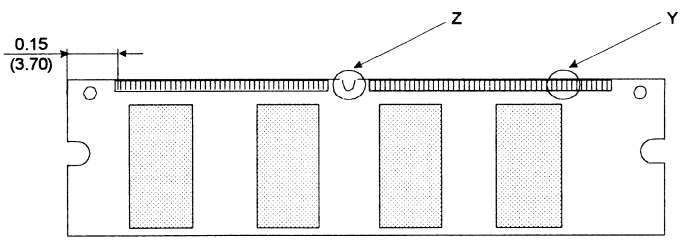
(V=Valid, X=Don't care, H=Logic high, L=Logic low)

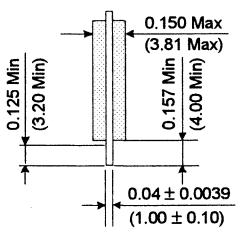
Notes : 1. OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

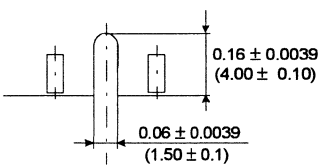
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

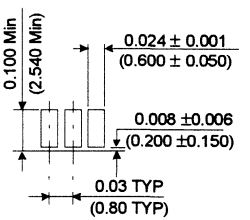








Detail Z



Detail Y

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832D

M466S0823DT3-L10, C10

- Organization : 8Mx64
- Composition : 8Mx8 *8
- Used component part # : K4S640832D-TL10, C10
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,050mil height & double sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module banks on this assembly	1 bank	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	1 bank of 64MB	10h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	ECh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	8	38h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	D	44h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	3	33h	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	L / C	4Ch / 43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	3	33h	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M466S0824DT2 SDRAM SODIMM

8Mx64 SDRAM SODIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M466S0824DT2 is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M466S0824DT2 consists of eight CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M466S0824DT2 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M466S0824DT2-L10 /C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,150mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VSS	2	VSS	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	VSS	56	VSS	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	VSS	108	VSS
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	VSS	22	VSS	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	*A12	119	VSS	120	VSS
27	VDD	28	VDD	71	$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	VSS	76	VSS	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	VSS	36	VSS	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	VSS	140	VSS
47	DQ12	48	DQ44	91	VSS	92	VSS	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0 ~ CKE1	Clock enable input
$\overline{CS0}$ ~ $\overline{CS1}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

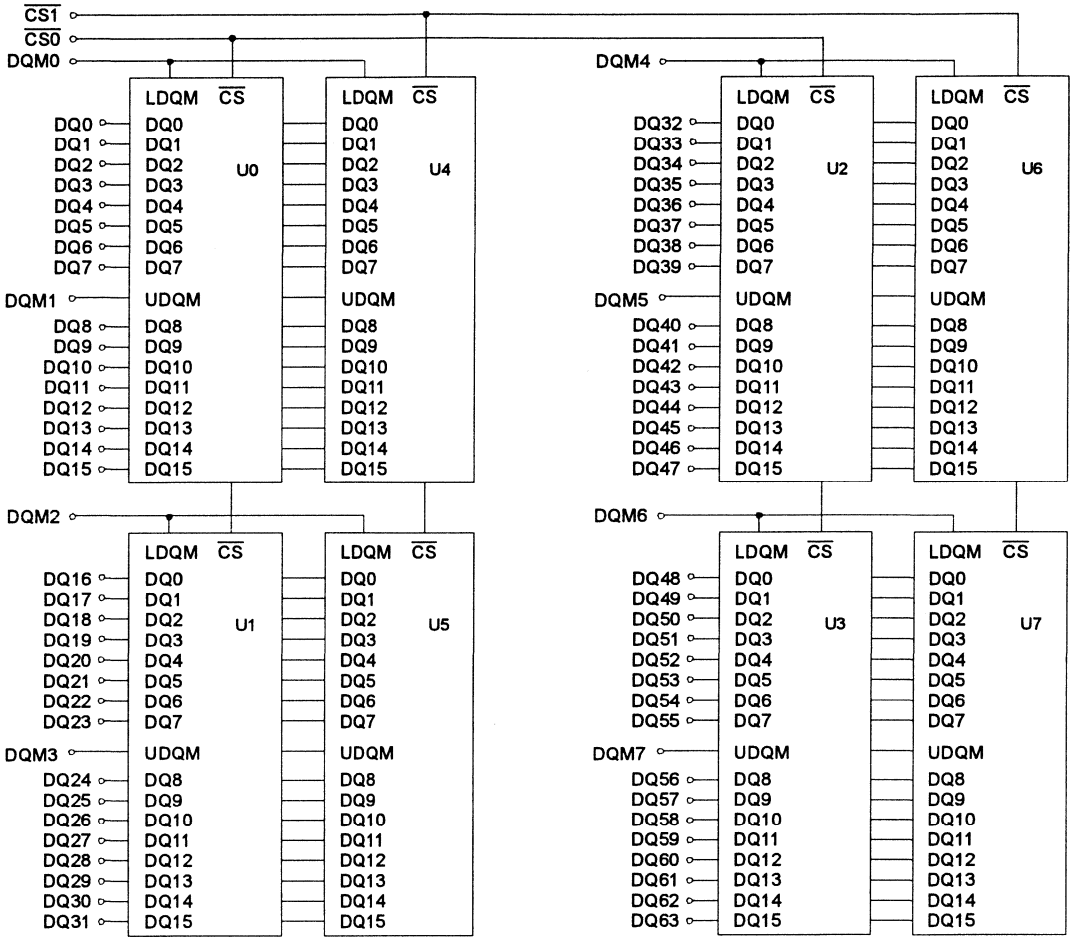
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

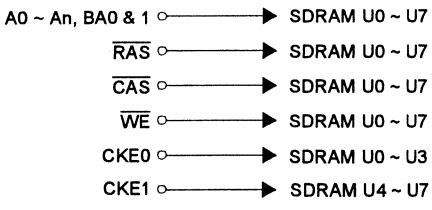
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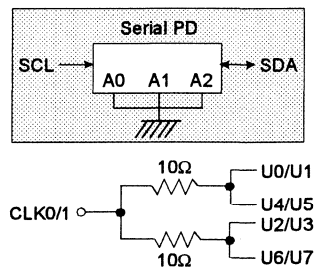
PIN CONFIGURATION DESCRIPTION

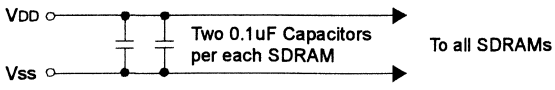
Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA7
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM









ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC.The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	25	45	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	25	45	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	15	25	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	15	21	pF
Input capacitance ($\overline{CS0}$ ~ $\overline{CS1}$)	C_{IN5}	15	25	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	10	12	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	10	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition		Version -10	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA		500	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		8	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} =∞		8		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		120	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		48		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		24	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} =∞		24		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		200	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		120	mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs		540	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		600	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	C	8	mA	
			L	3.2	mA	

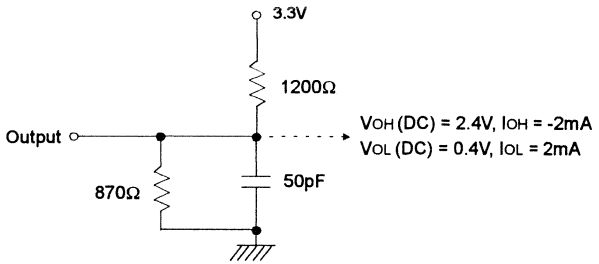
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

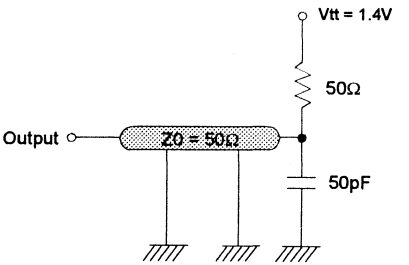
3. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	12	ns	2
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tSAC		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	tOH	3		ns	2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tSS	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

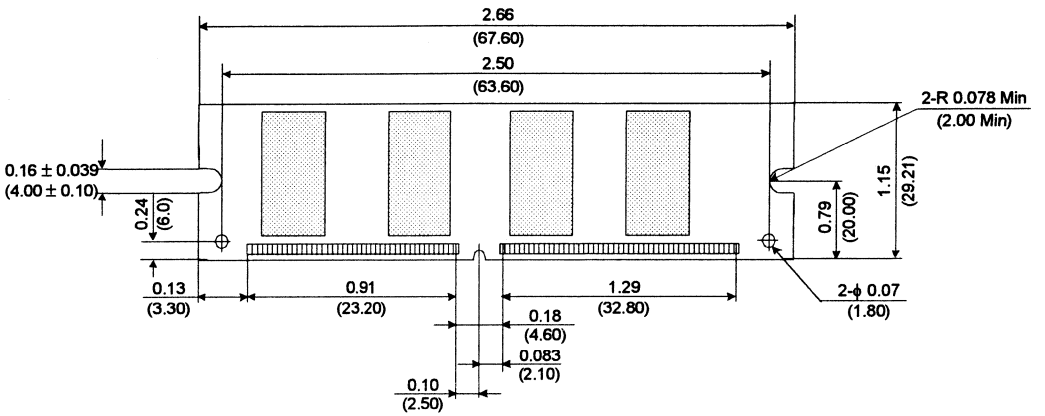
Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A7)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A7)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

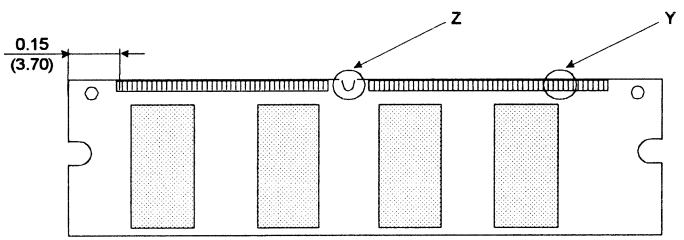
(V=Valid, X=Don't care, H=Logic high, L=Logic low)

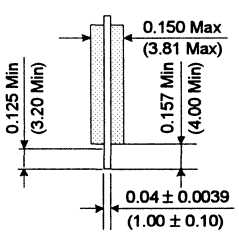
Notes : 1. OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

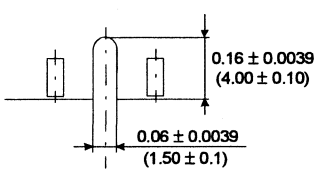
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

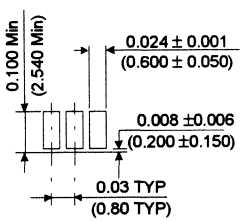








Detail Z



Detail Y

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : K4S641632D

M466S0824DT2-L10, C10

- Organization : 8Mx64
- Composition : 4Mx16 *8
- Used component part # : K4S641632D-TL10, C10
- # of banks in module : 2 banks
- # of banks in component : 4 banks
- Feature : 1,150mil height & double sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	8	08h	1
5	# of module banks on this assembly	2 banks	02h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	2 banks of 32MB	08h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	ECh	

Byte #	Function Described	Function Supported -0	Hex value -0	Note
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	8	38h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	D	44h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	L / C	4Ch / 43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M466S0424CT0 SDRAM SODIMM

4Mx64 SDRAM SODIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M466S0424CT0 is a 4M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M466S0424CT0 consists of four CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M466S0424CT0 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M466S0424CT0-L10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,000mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

1	VSS	2	VSS	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	VSS	56	VSS	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD					105	A8	106	BA0
13	DQ4	14	DQ36		**Voltage Key**			107	VSS	108	VSS
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	VSS	22	VSS	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	*A12	119	VSS	120	VSS
27	VDD	28	VDD	71	*$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	*CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	VSS	76	VSS	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	VSS	36	VSS	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	VSS	140	VSS
47	DQ12	48	DQ44	91	VSS	92	VSS	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0	Clock input
CKE0	Clock enable input
$\overline{CS0}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

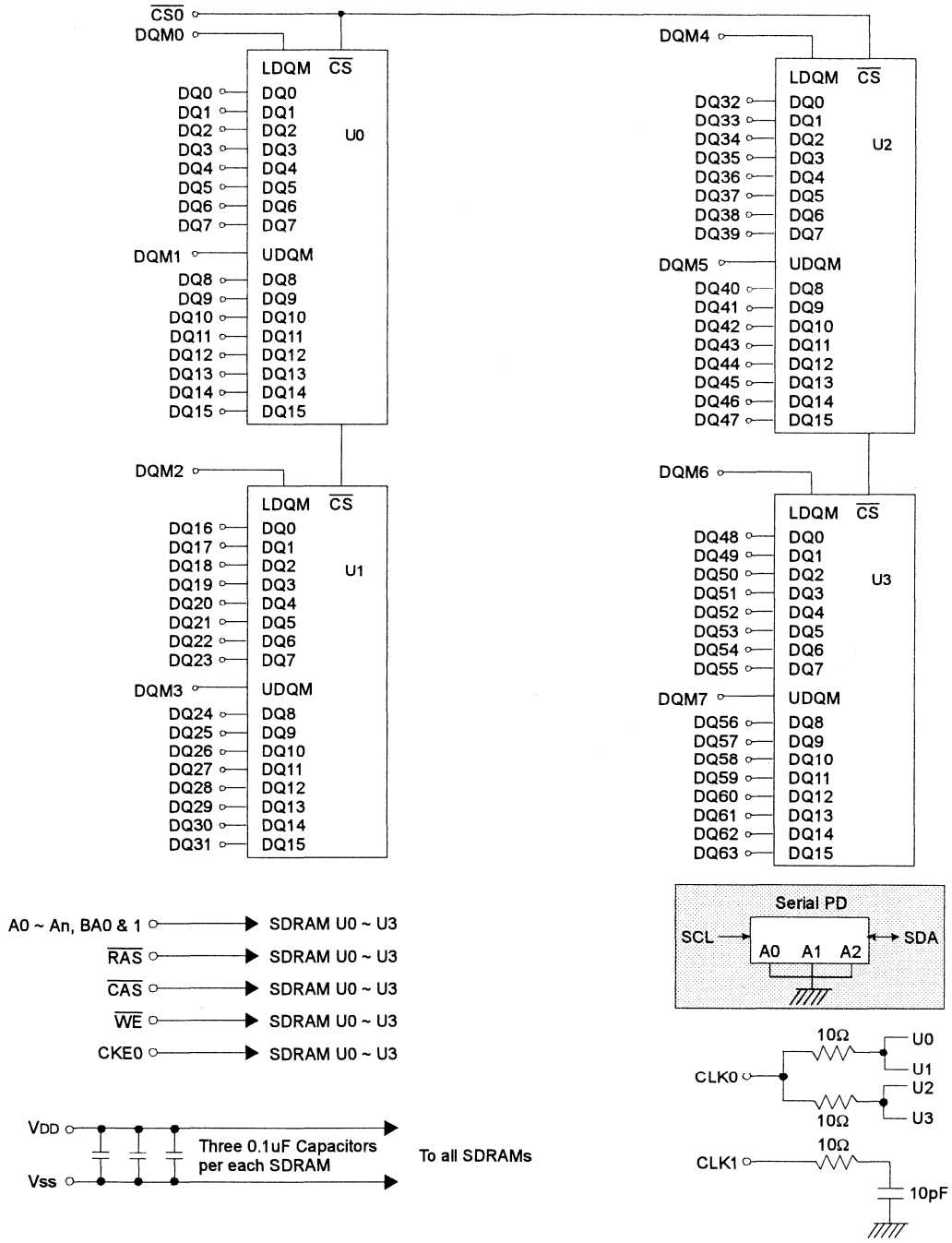
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA7
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
$DQ_{0 \sim 63}$	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	4	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-4	-	4	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC.The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	30	40	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	30	40	pF
Input capacitance (CKE0)	C_{IN3}	25	35	pF
Input capacitance (CLK0)	C_{IN4}	25	35	pF
Input capacitance ($\overline{CS0}$)	C_{IN5}	25	35	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	5	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	5	15	pF

DC CHARACTERISTICS

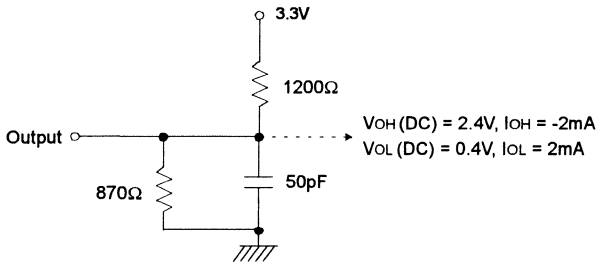
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -10	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		260	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		4	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} =∞		4		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		48	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		24		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		8	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} =∞		8		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		80	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		40	mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	300	mA	1
			2	280		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		440	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		1.8	mA	

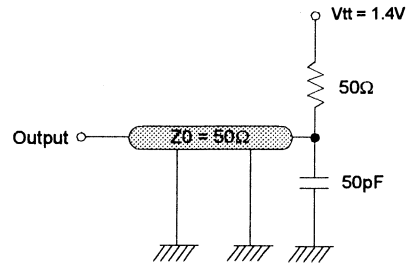
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	12	ns	2
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tSAC		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	tOH	3		ns	2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tSS	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

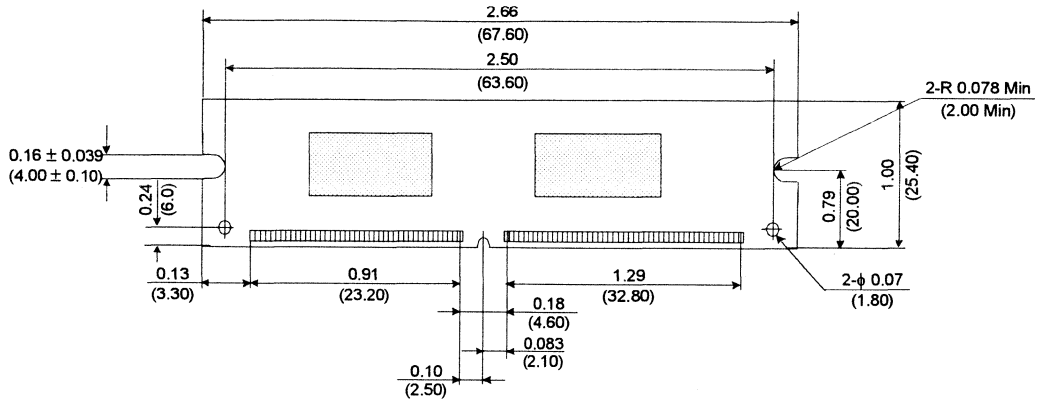
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

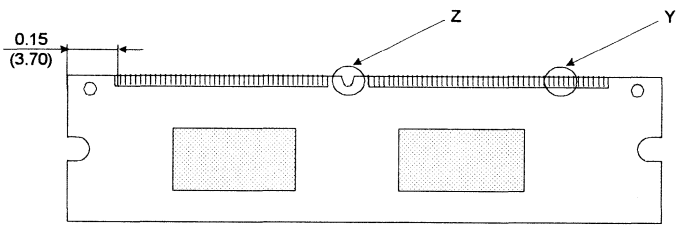
6. Burst stop command is valid at every burst length.

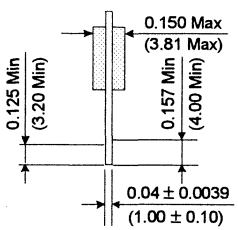
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

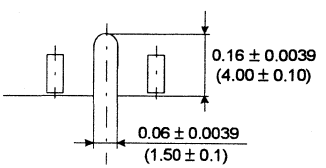
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

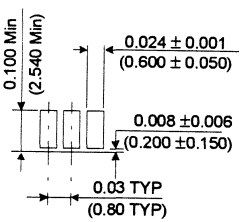








Detail Z



Detail Y

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : K4S641632C

M466S0424CT0-L10

- Organization : 4Mx64
- Composition : 4Mx16 *4
- Used component part # : K4S641632C-TL10
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	8	08h	1
5	# of module banks on this assembly	1 bank	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	1 bank of 32MB	08h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	EBh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	4	34h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	C	43h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	0	30h	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	L	4Ch	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	0	30h	
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)	43h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M466S0823CT2 SDRAM SODIMM

8Mx64 SDRAM SODIMM based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M466S0823CT2 is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M466S0823CT2 consists of eight CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M466S0823CT2 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M466S0823CT2-L10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,150mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

1	VSS	2	VSS	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	VSS	56	VSS	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	VSS	108	VSS
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	VSS	22	VSS	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	*A12	119	VSS	120	VSS
27	VDD	28	VDD	71	*$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	VSS	76	VSS	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	VSS	36	VSS	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	VSS	140	VSS
47	DQ12	48	DQ44	91	VSS	92	VSS	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0	Clock enable input
$\overline{CS0}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

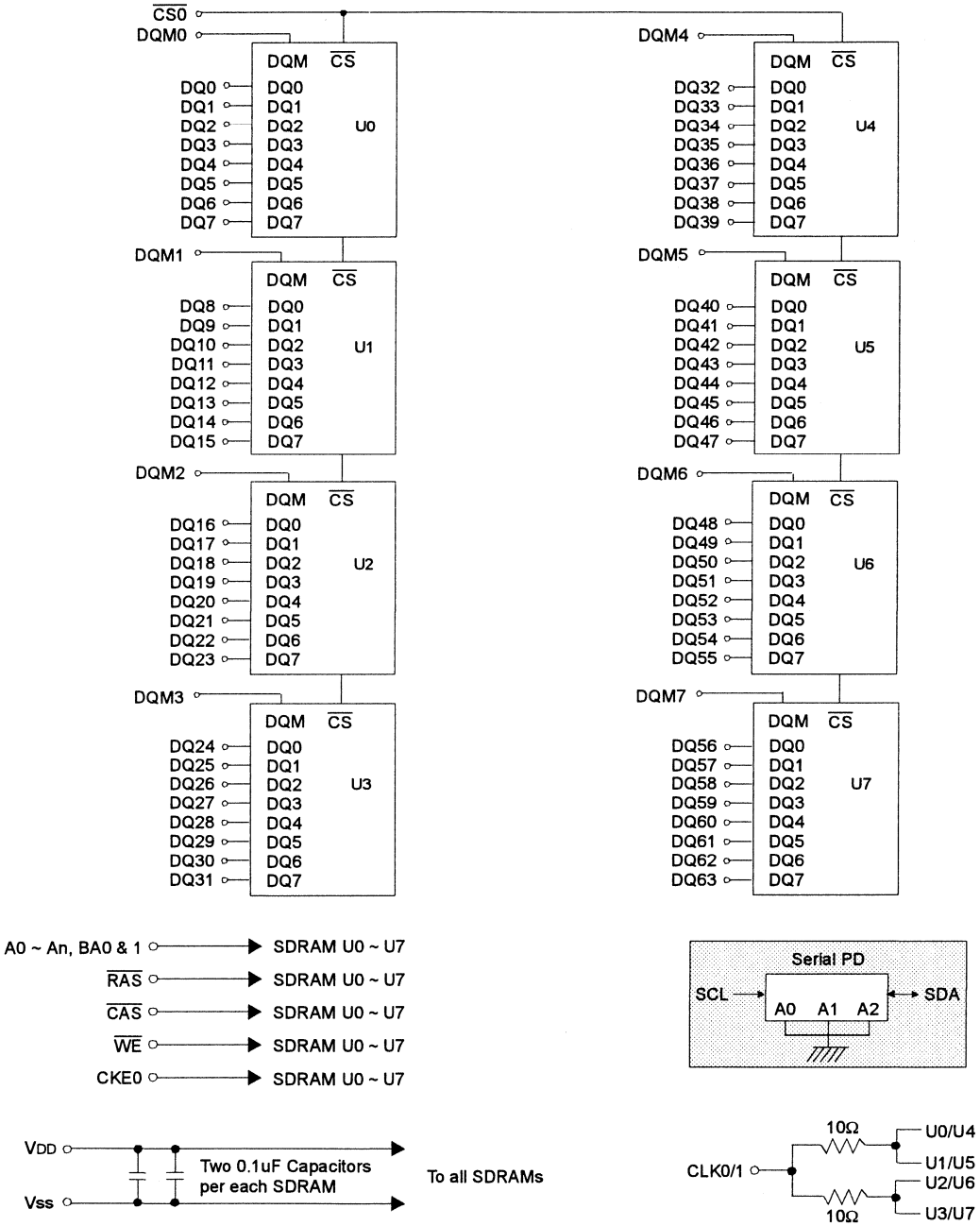
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-8	-	8	uA	3
Input leakage current (I/O pins)	• I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC.The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	40	60	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	40	60	pF
Input capacitance (CKE0)	C_{IN3}	35	55	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	25	35	pF
Input capacitance ($\overline{CS0}$)	C_{IN5}	35	55	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	5	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	5	15	pF

DC CHARACTERISTICS

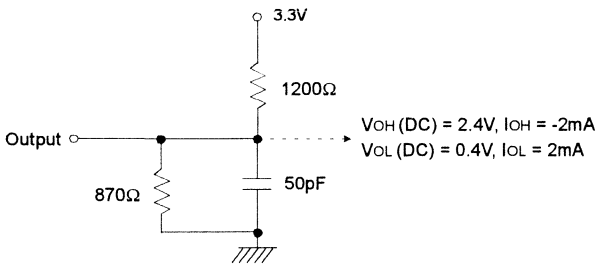
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -10	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		520	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		8	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} =∞		8		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		96	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		48		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		16	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} =∞		16		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		160	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		80	mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	600	mA	1
			2	560		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		880	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		3.6	mA	

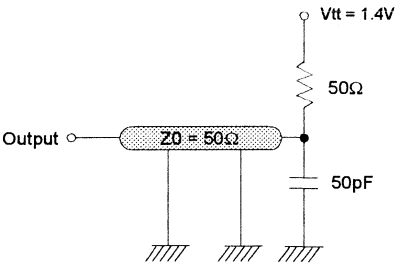
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	12	ns	2
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tSAC		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	tOH	3		ns	2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tSS	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

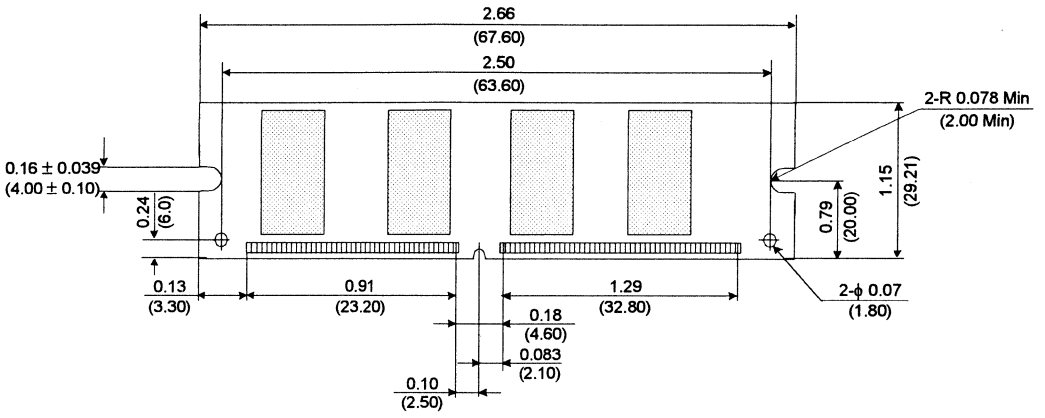
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

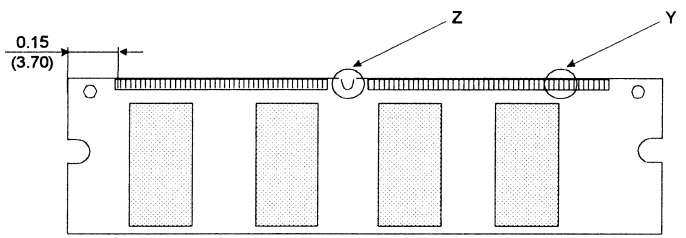
6. Burst stop command is valid at every burst length.

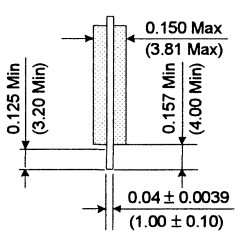
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

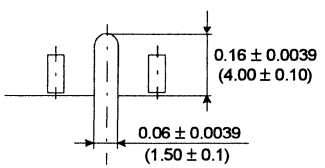
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

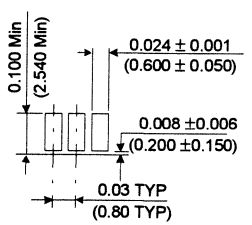








Detail Z



Detail Y

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832C

M466S0823CT2-L10

- Organization : 8Mx64
- Composition : 8Mx8 *8
- Used component part # : K4S640832C-TL10
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,150mil height & double sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module banks on this assembly	1 bank	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	1 bank of 64MB	10h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	ECh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	8	38h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	C	43h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	L	4Ch	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)	43h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M466S0823CT3 SDRAM SODIMM

8Mx64 SDRAM SODIMM based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M466S0823CT3 is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M466S0823CT3 consists of eight CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M466S0823CT3 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M466S0823CT3-L10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,050mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

1	VSS	2	VSS	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	VSS	56	VSS	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD					105	A8	106	BA0
13	DQ4	14	DQ36		Voltage Key			107	VSS	108	VSS
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	VSS	22	VSS	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	*A12	119	VSS	120	VSS
27	VDD	28	VDD	71	*$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	VSS	76	VSS	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	VSS	36	VSS	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	VSS	140	VSS
47	DQ12	48	DQ44	91	VSS	92	VSS	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0	Clock enable input
$\overline{CS0}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

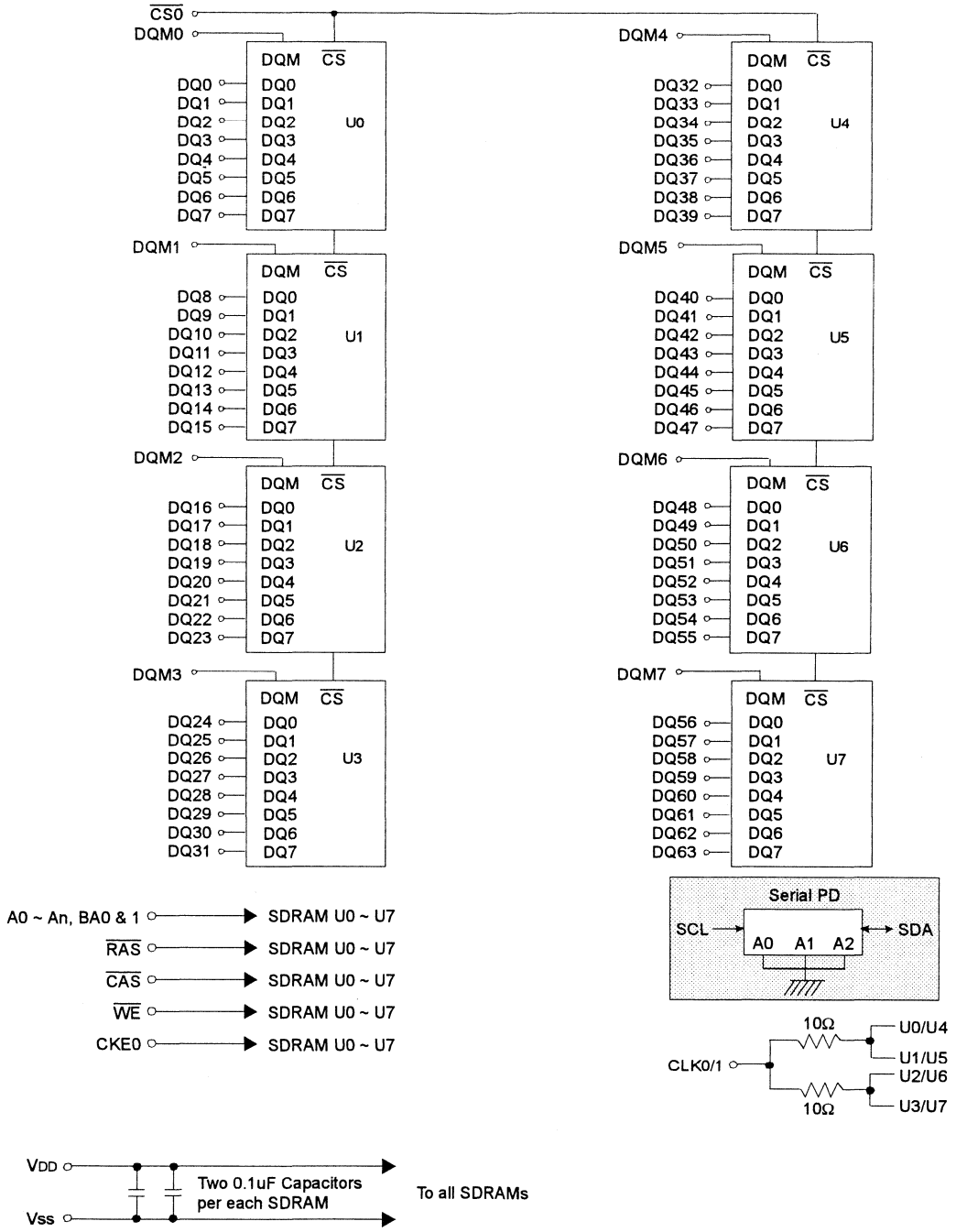
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+t_{SS} prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
$DQ_{0 \sim 63}$	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-8	-	8	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC.The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	40	60	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	40	60	pF
Input capacitance (CKE0)	C_{IN3}	35	55	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	25	35	pF
Input capacitance ($\overline{CS0}$)	C_{IN5}	35	55	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	5	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	5	15	pF

DC CHARACTERISTICS

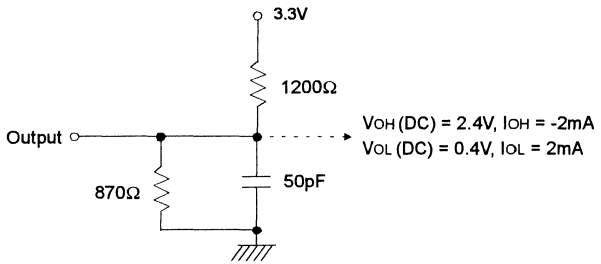
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -10	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		520	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		8	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} =∞		8		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		96	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		48		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		16	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} =∞		16		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		160	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		80	mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	600	mA	1
			2	560		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		880	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		3.6	mA	

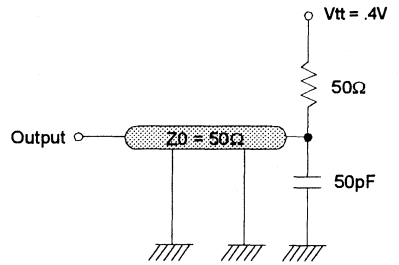
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	12	ns	2
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	t_{SAC}		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	t_{OH}	3		ns	2
	CAS latency=2		3			
CLK high pulse width		t_{CH}	3.5		ns	3
CLK low pulse width		t_{CL}	3.5		ns	3
Input setup time		t_{SS}	2.5		ns	3
Input hold time		t_{SH}	1.5		ns	3
CLK to output in Low-Z		t_{SLZ}	1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		7	ns	
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

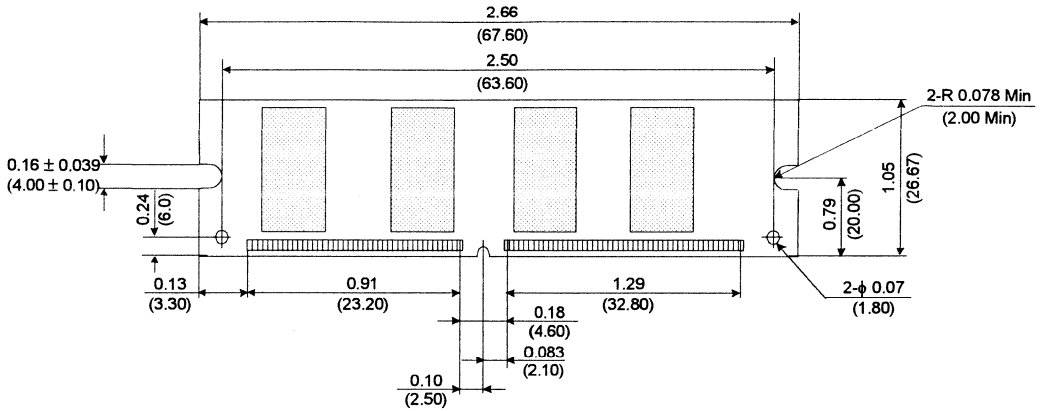
Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A8)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A8)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

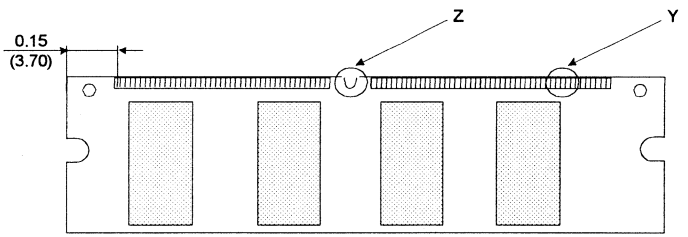
(V=Valid, X=Don't care, H=Logic high, L=Logic low)

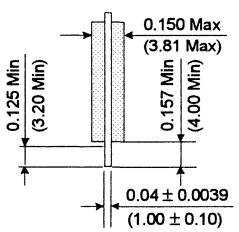
Notes : 1. OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

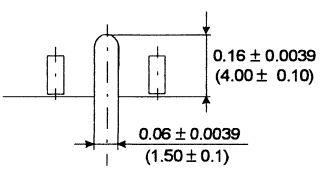
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

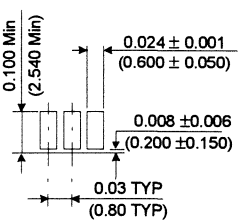








Detail Z



Detail Y

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832C

M466S0823CT3-L10

- Organization : 8Mx64
- Composition : 8Mx8 *8
- Used component part # : K4S640832C-TL10
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,050mil height & double sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module banks on this assembly	1 bank	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	1 bank of 64MB	10h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	ECh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	8	38h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	C	43h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	3	33h	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	L	4Ch	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	3	33h	
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)	43h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M466S0824CT2 SDRAM SODIMM

8Mx64 SDRAM SODIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M466S0824CT2 is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M466S0824CT2 consists of eight CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M466S0824CT2 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M466S0824CT2-L10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,150mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VSS	2	VSS	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	VSS	56	VSS	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	VSS	108	VSS
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	VSS	22	VSS	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	*A12	119	VSS	120	VSS
27	VDD	28	VDD	71	$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	VSS	76	VSS	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	VSS	36	VSS	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	VSS	140	VSS
47	DQ12	48	DQ44	91	VSS	92	VSS	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0 ~ CKE1	Clock enable input
$\overline{CS0}$ ~ $\overline{CS1}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

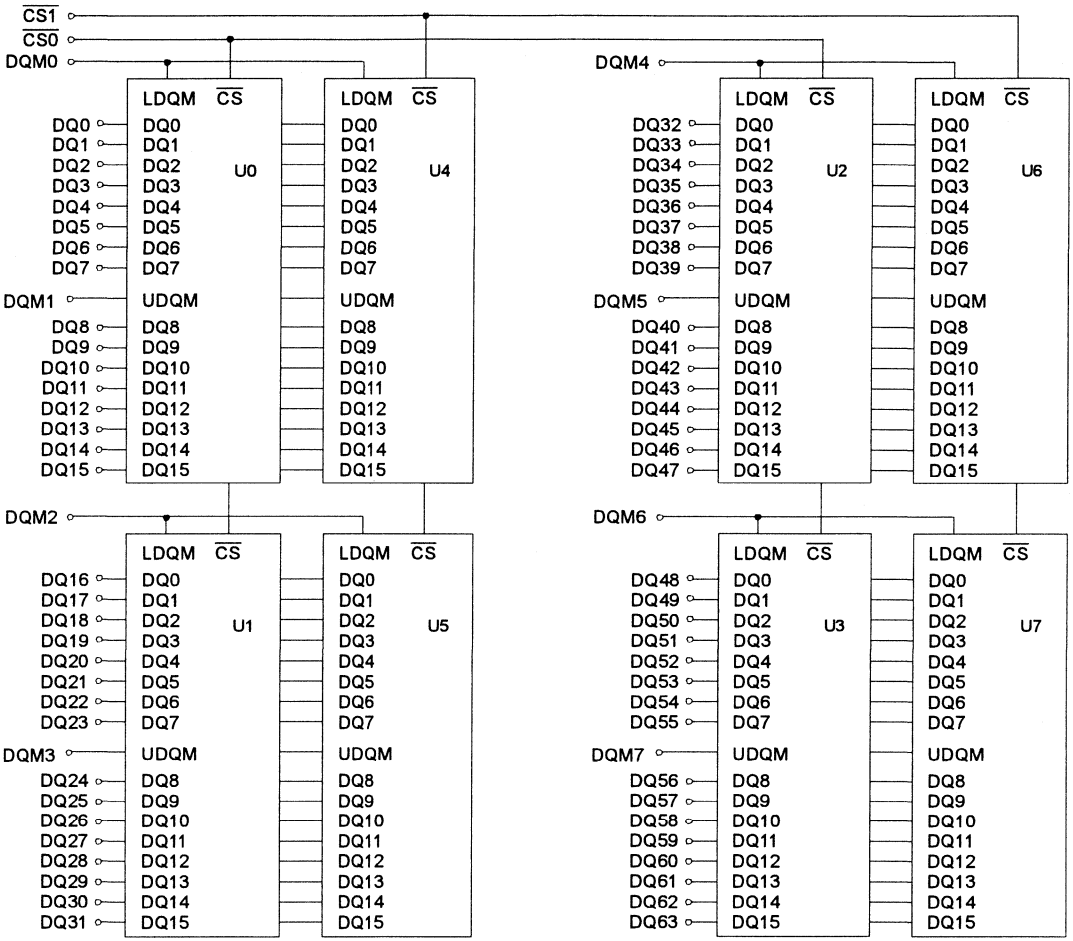
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

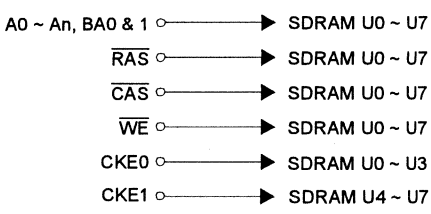
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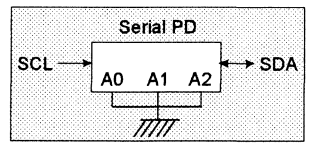
PIN CONFIGURATION DESCRIPTION

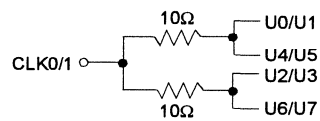
Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+t_{SS} prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA7
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
$DQ_{0 \sim 63}$	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.

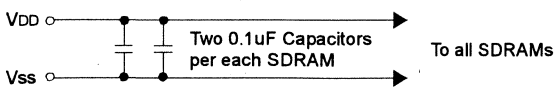
FUNCTIONAL BLOCK DIAGRAM











SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-8	-	8	uA	3
Input leakage current (I/O pins)	I_{IL}	-3	-	3	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC.The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	40	60	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	40	60	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	25	35	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	25	35	pF
Input capacitance ($\overline{CS0}$ ~ $\overline{CS1}$)	C_{IN5}	25	35	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	15	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	5	15	pF

DC CHARACTERISTICS

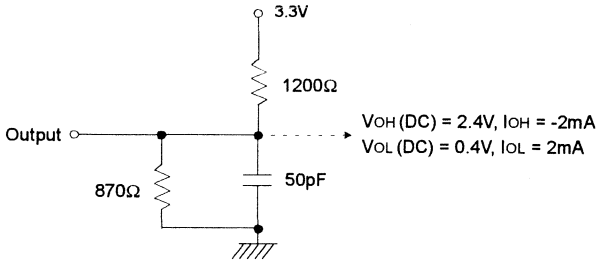
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -10	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		340	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		8	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} =∞		8		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		96	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		48		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		16	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} =∞		16		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		160	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		80	mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	380	mA	1
			2	360		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		880	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		3.6	mA	

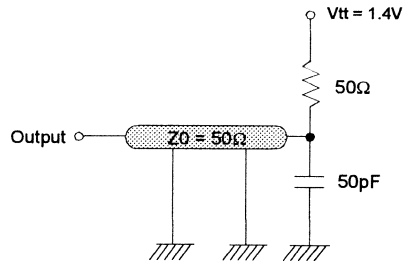
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	12	ns	2
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tSAC		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	tOH	3		ns	2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tSS	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

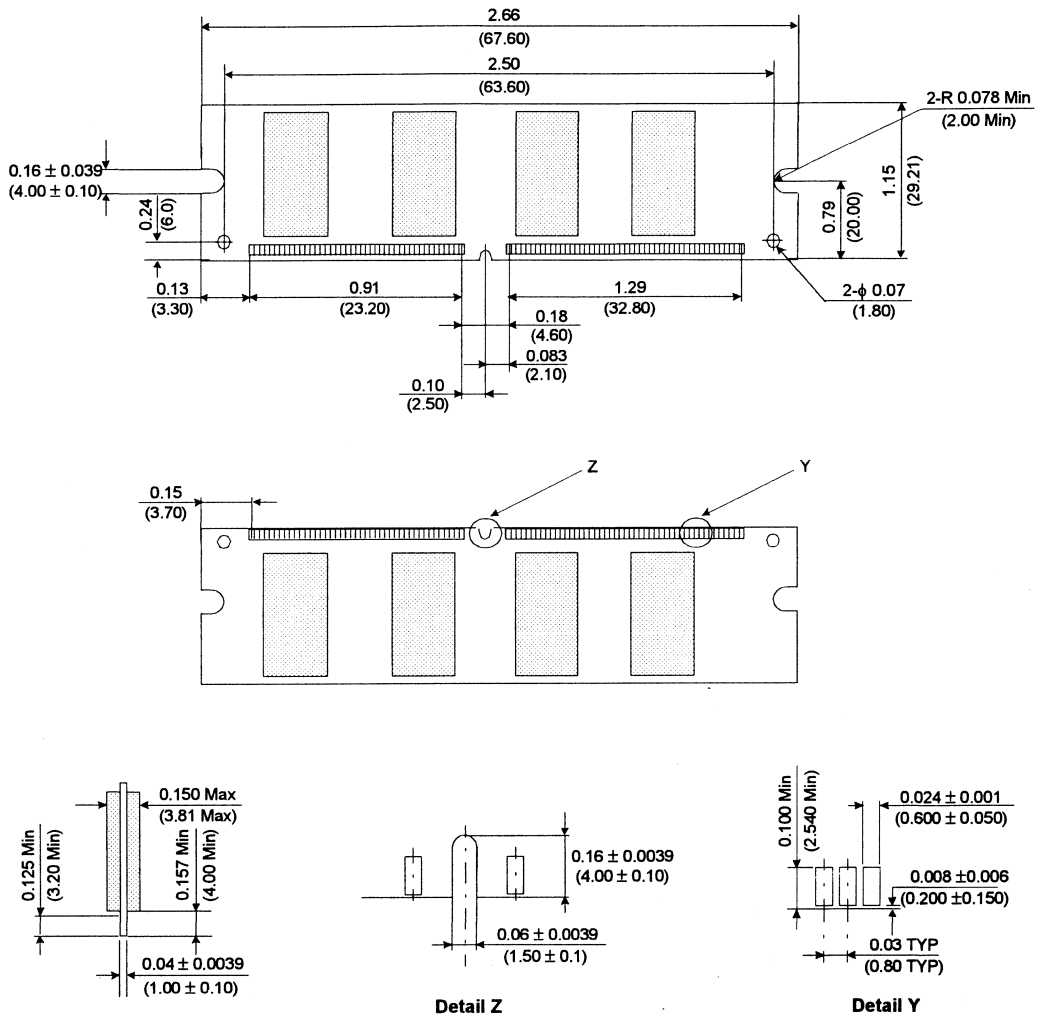
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : K4S641632C

M466S0824CT2-L10

- Organization : 8Mx64
- Composition : 4Mx16 *8
- Used component part # : K4S641632C-TL10
- # of banks in module : 2 banks
- # of banks in component : 4 banks
- Feature : 1,150mil height & double sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	8	08h	1
5	# of module banks on this assembly	2 banks	02h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	2 banks of 32MB	08h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	ECh	

Byte #	Function Described	Function Supported -0	Hex value -0	Note
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	8	38h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	C	43h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	L	4Ch	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)	43h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

Module Specification

3

PC100 Registered DIMM

M377S0823DT3 SDRAM DIMM (Intel 1.2 ver. Base)

8Mx72 SDRAM DIMM with PLL & Register based on 8Mx8, 4Banks 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S0823DT3 is a 8M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S0823DT3 consists of nine CMOS 8Mx8 bit Synchronous DRAMs in TSOP-II 400mil packages, two 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S0823DT3 is a Dual In-line Memory Module and is intented for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high band-width, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S0823DT3-C1H	100MHz (10ns @ CL=2)
M377S0823DT3-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,500mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	*CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Colume address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

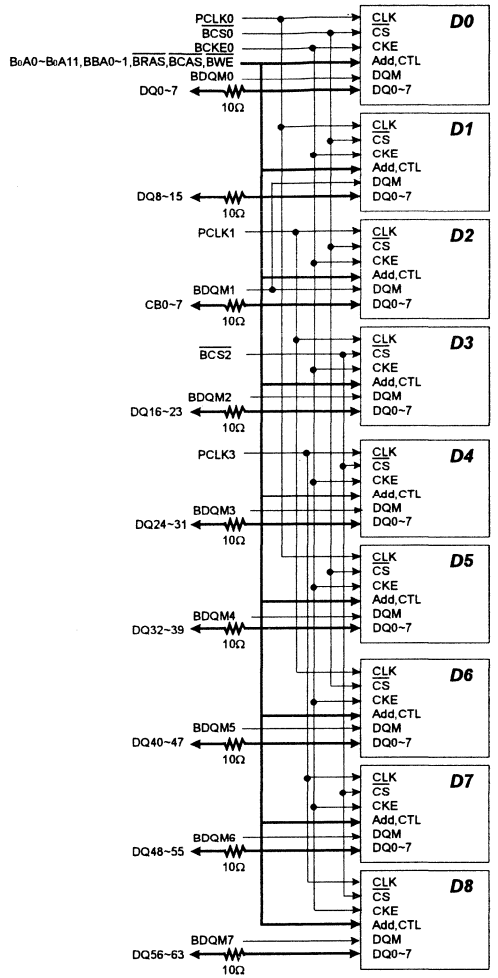
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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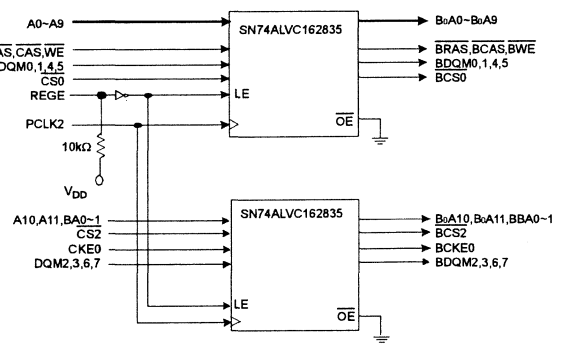
PIN CONFIGURATION DESCRIPTION

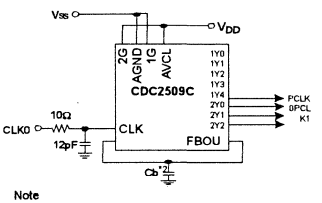
Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	*Register enable*	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to V_{DD} through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
WP	*Write protection*	WP pin is connected to V_{SS} through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM

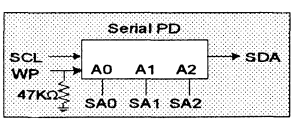


Notes : Address/Control Signals are connected to D2 through 100 ohms resistor.

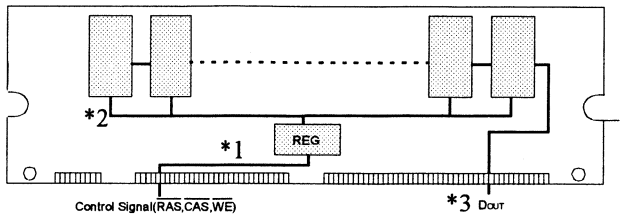


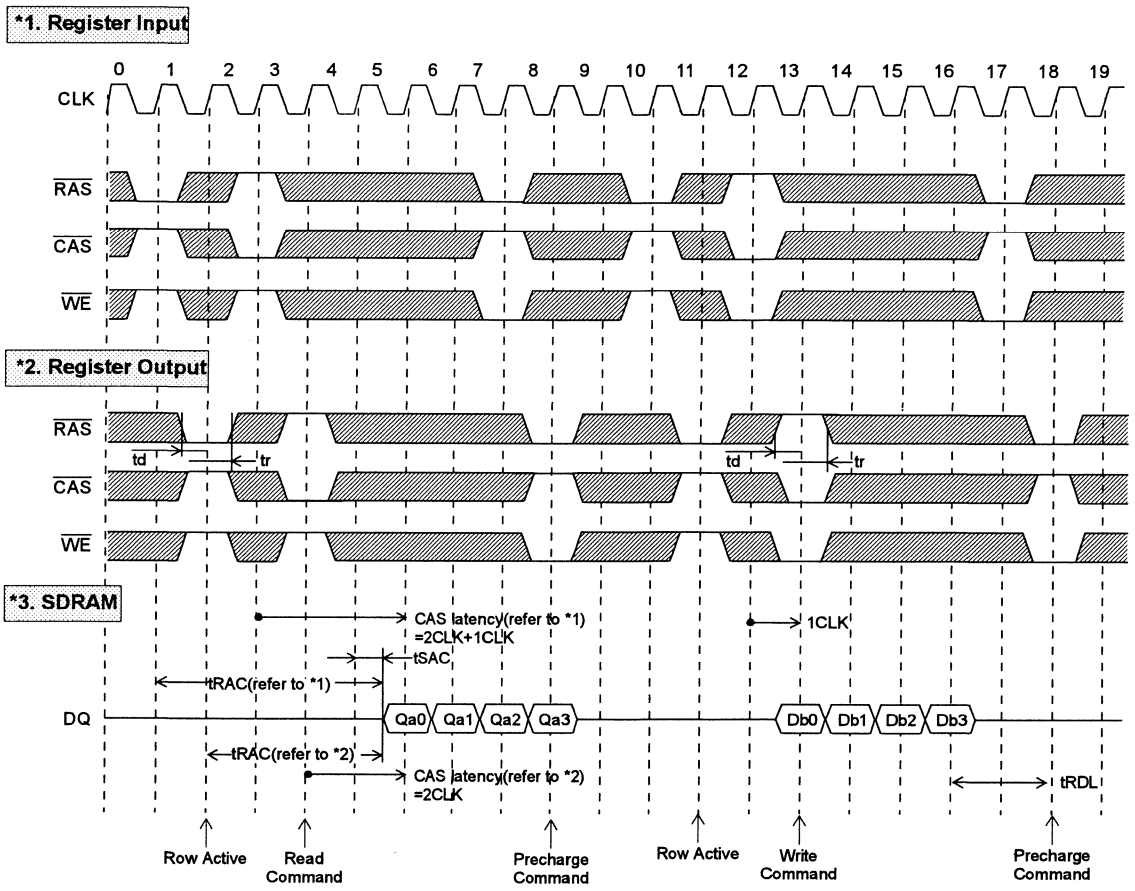


Note
1. Unused clock termination : 10Ω and 12pF
2. The actual values of Cb will depend upon the PLL chosen.



STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)





td, tr = Delay of register (74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

: Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	9	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended Operating Conditions (Voltage Referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11})	C_{IN1}	-	12	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	12	pF
Input capacitance (CKE0)	C_{IN3}	-	12	pF
Input capacitance (CLK0)	C_{IN4}	-	12	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	12	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	12	pF
Input capacitance (BA0 ~ BA1)	C_{IN7}	-	12	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	12	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT1}	-	12	pF

DC CHARACTERISTICS

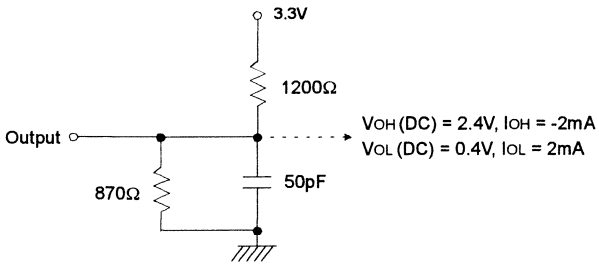
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version		Unit	Note
			-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	1,130		mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	359		mA	3
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	11			
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	485		mA	3
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	56			
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	377		mA	3
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	29			
Active standby current in non power-down mode	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	575		mA	3
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	137		mA	3
Operating current (Burst mode)	I_{CC4}	I_O = 0mA Page burst 4Banks activated t_{CCD}=2CLK	1,355		mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	1,625		mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	359		mA	3

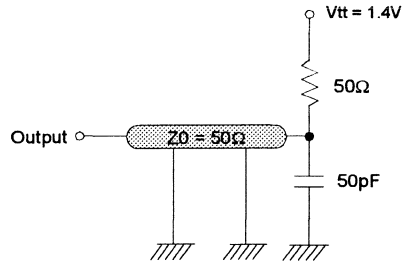
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Measured with 1 PLL & 2 Drive ICs.
4. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to row precharge		tRDL(min)	2		CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns		-	5
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

Notes :
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For 1H/1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported . SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	1,2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	1
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

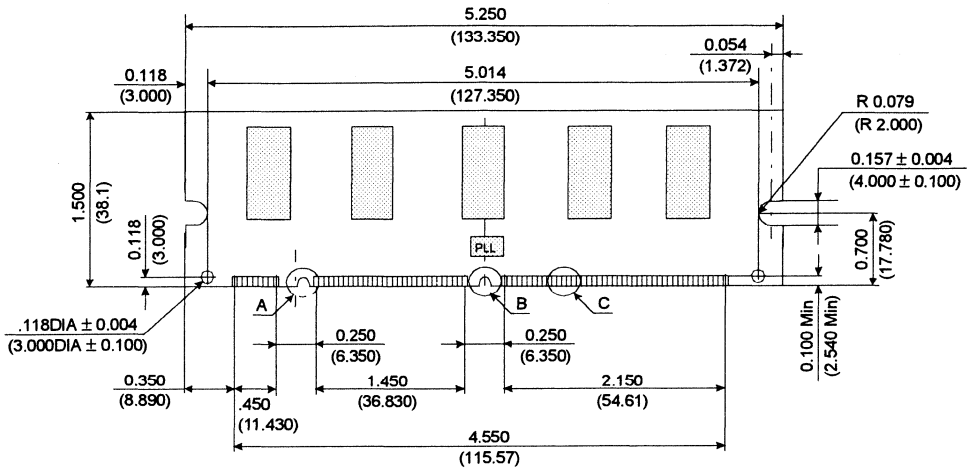
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

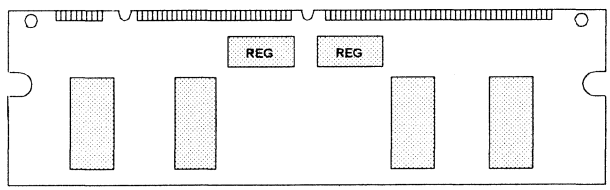
6. Burst stop command is valid at every burst length.

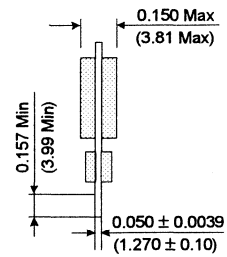
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

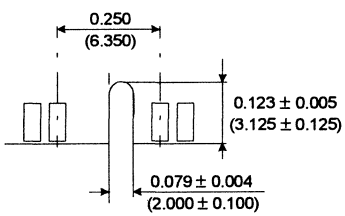
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

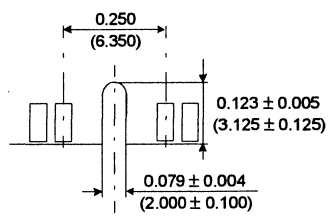




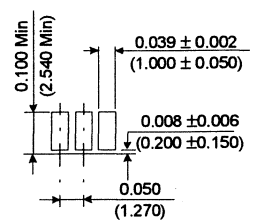




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832D

M377S0823DT3-C1H/C1L(1.2ver)

- Organization : 8MX72
- Composition : 8MX8 *9
- Used component part # : K4S640832D-TC1H/C1L
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,500 mil height & double sided component
- Refresh : 4K/64ms
- **Contents** :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	9		09h		1
5	# of module Rows on this assembly	1 Row		01h		
6	Data width of this assembly	72 bits		48h		
7	..... Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x8		08h		
14	Error checking SDRAM width	x8		08h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	1 Row of 64MB		10h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		36h	66h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	..... Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	..... Manufacturer part # (Data bits)	7		37h		
77	..... Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	0		30h		
80	..... Manufacturer part # (Module depth)	8		38h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	3		33h		
83	Manufacturer part # (Component revision)	D		44h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	3		33h		
86	Manufacturer part # (Hyphen)	"-"		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	3		33h		
92	..... Manufacturer revision code (For component)	D (5th Gen.)		44h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M377S1620DT3 SDRAM DIMM (Intel 1.2 ver. Base)

16Mx72 SDRAM DIMM with PLL & Register based on 16Mx4, 4Banks, 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S1620DT3 is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S1620DT3 consists of eighteen CMOS 16Mx4 bit Synchronous DRAMs in TSOP-II 400mil packages, three 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S1620DT3 is a Dual In-line Memory Module and is intented for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S1620DT3-C1H	100MHz (10ns @ CL=2)
M377S1620DT3-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,700mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	*CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Colume address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

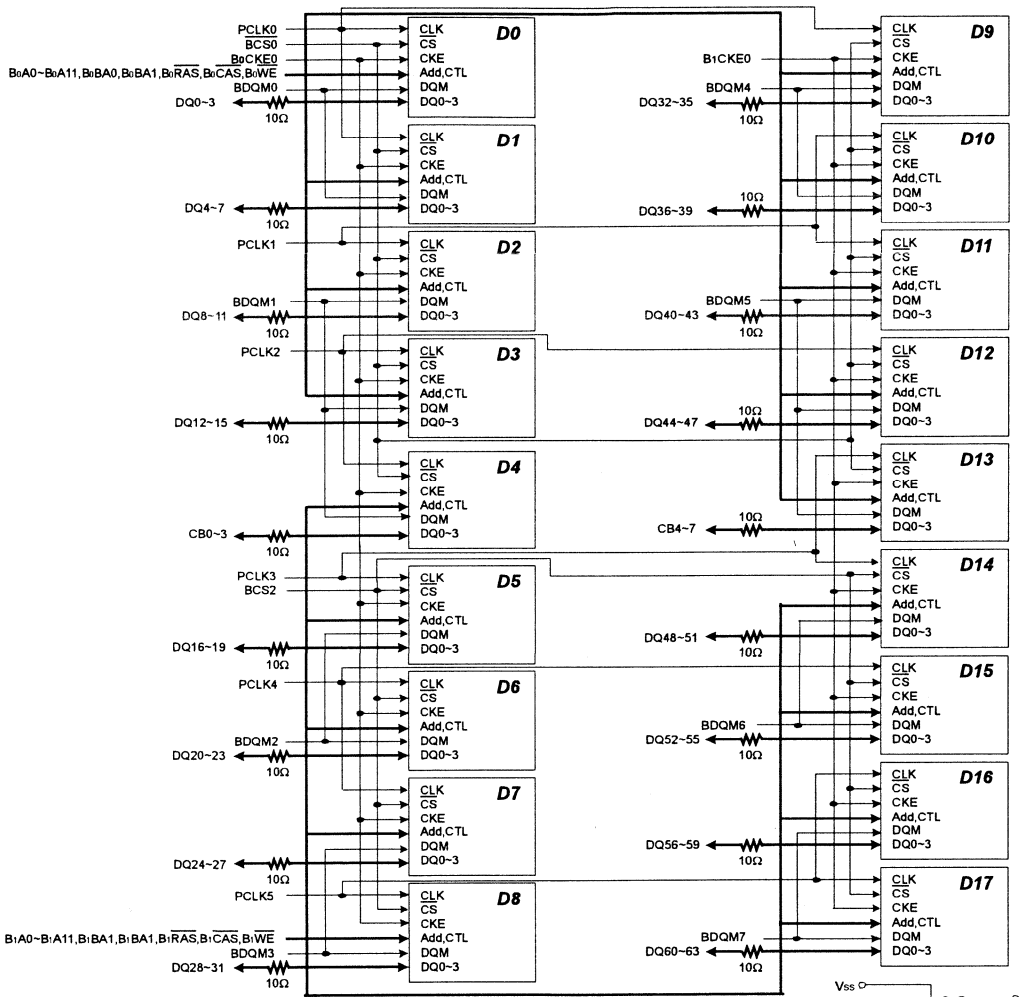
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

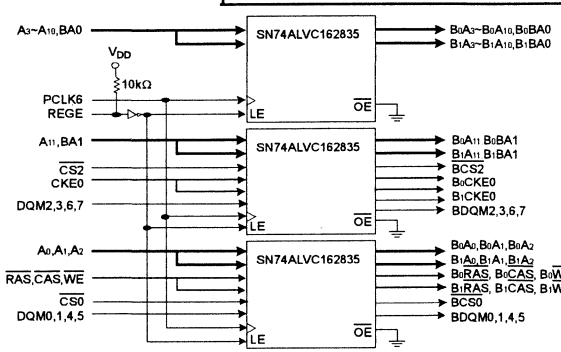
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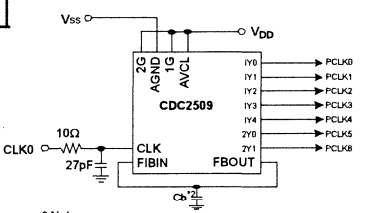
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	*Register enable*	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to V_{DD} through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
WP	*Write protection*	WP pin is connected to Vss through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.

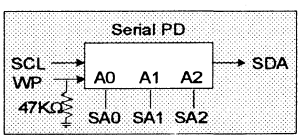
FUNCTIONAL BLOCK DIAGRAM





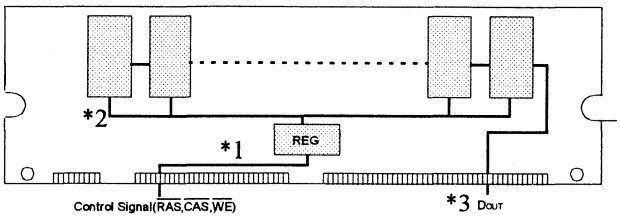


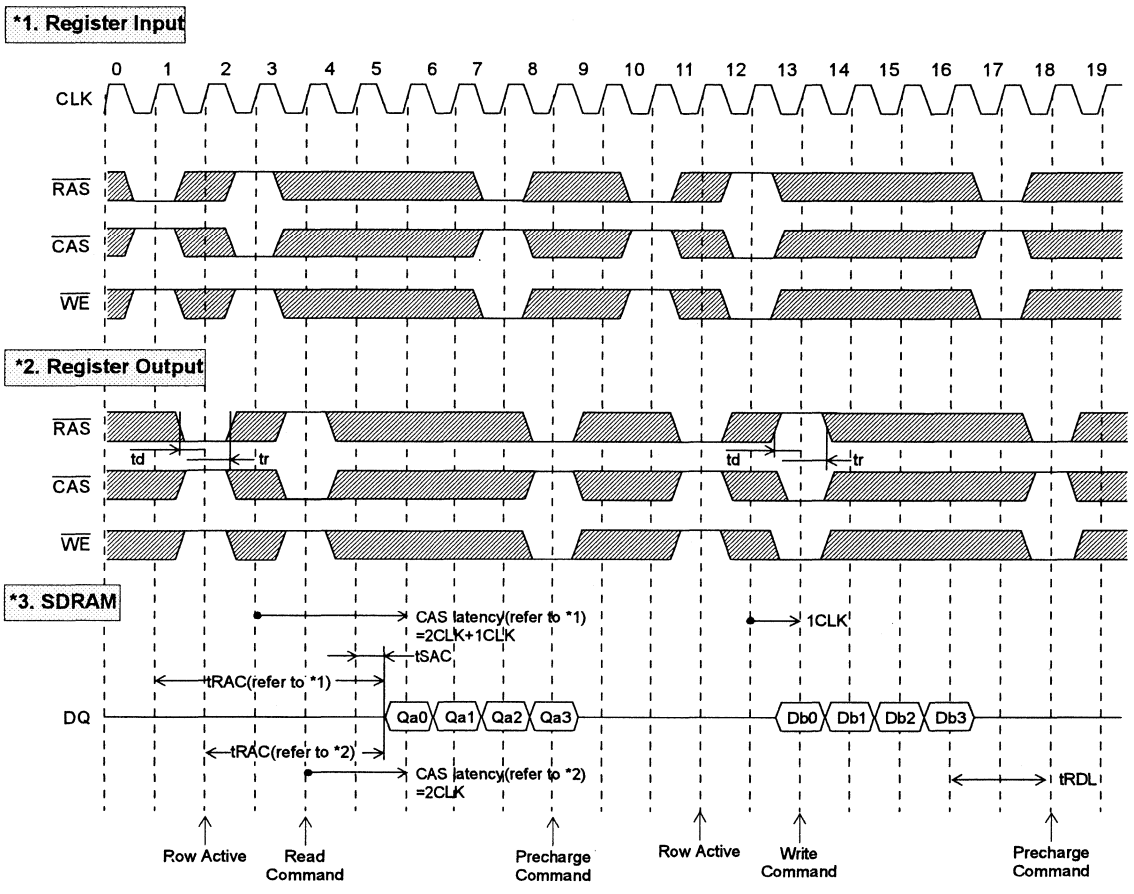
* Note
1. Unused clock termination : 10Ω and 12pF
2. The actual values of Cb will depend upon the PLL chosen.



SAMSUNG ELECTRONICS

STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)





td, tr = Delay of register (74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

: Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	18	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11})	C_{IN1}	-	19	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	19	pF
Input capacitance (CKE0)	C_{IN3}	-	19	pF
Input capacitance (CLK0)	C_{IN4}	-	12	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	12	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	12	pF
Input capacitance (BA0 ~ BA1)	C_{IN7}	-	19	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	12	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT1}	-	12	pF

DC CHARACTERISTICS

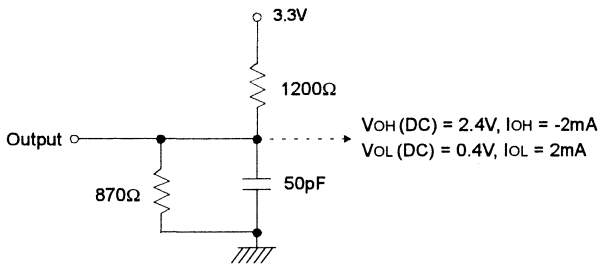
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version		Unit	Note
			-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	1,670		mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	368		mA	3
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	20		mA	
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	620		mA	3
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable	110			
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	404		mA	3
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	56			
Active Standby current in non power-down mode	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	800		mA	3
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	272		mA	3
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0mA Page burst 4 Banks activated t_{CCD}=2CLK	1,940		mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	2,750		mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	368		mA	3

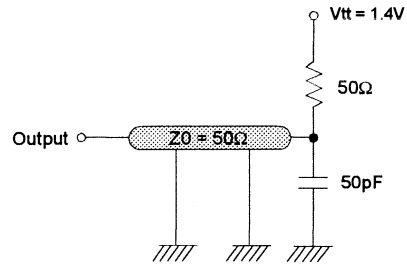
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Measured with 1 PLL & 3 Drive ICs.
4. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to row precharge		tRDL(min)	2		CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns		-	5
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

Notes :
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For 1H/1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported . SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	1,2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	1
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

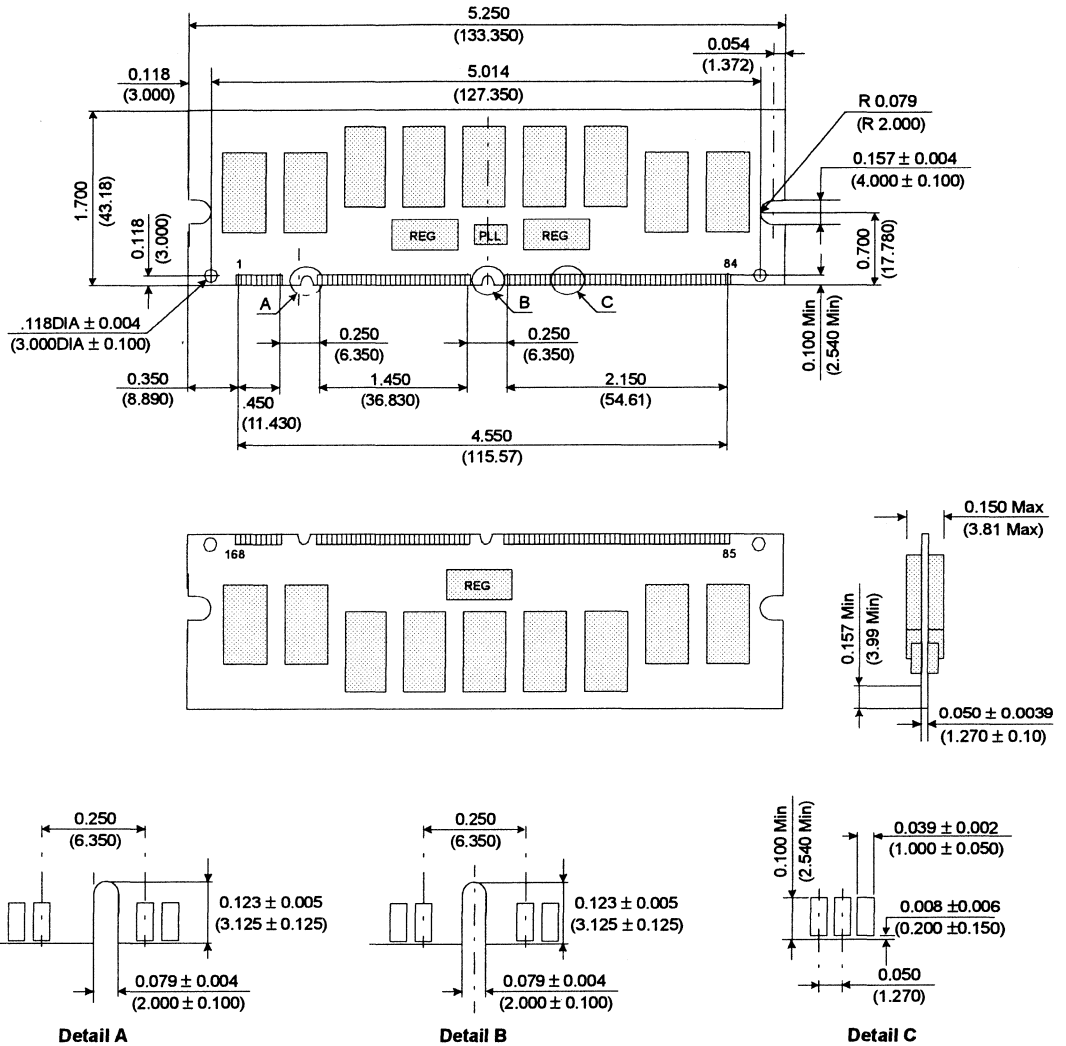
Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_9$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_9$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 16Mx4 SDRAM, TSOP
SDRAM Part No. : K4S640432D

M377S1620DT3-C1H/C1L(1.2ver)

- Organization : 16MX72
- Composition : 16MX4 *18
- Used component part # : K4S640432D-TC1H/C1L
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 4K/64ms
- **Contents** :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	10		0Ah		1
5	# of module Rows on this assembly	1 Row		01h		
6	Data width of this assembly	72 bits		48h		
7	..... Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x4		04h		
14	Error checking SDRAM width	x4		04h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	1 Row of 128MB		20h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		3Fh	6Fh	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	..... Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	..... Manufacturer part # (Data bits)	7		37h		
77	..... Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	1		31h		
80	..... Manufacturer part # (Module depth)	6		36h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	0		30h		
83	Manufacturer part # (Component revision)	D		44h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	3		33h		
86	Manufacturer part # (Hyphen)	"-"		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	3		33h		
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)		44h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M350S0823CT1 SDRAM DIMM (Intel 1.0 ver. Base)

8Mx72 SDRAM DIMM with Register based on 8Mx8, 4Banks 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M350S0823CT1 is a 8M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M350S0823CT1 consists of nine CMOS 8Mx8 bit Synchronous DRAMs in TSOP-II 400mil packages, two 18-bits Drive ICs for input control signal and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168pin glass-epoxy substrate. One 0.22uF and two 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M350S0823CT1 is a Dual In-line Memory Module and is intented for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M350S0823CT1-C80	125MHz (8ns @ CL=3)
M350S0823CT1-C1H	100MHz (10ns @ CL=2)
M350S0823CT1-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,500mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0 ~ 3	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address storbe
$\overline{CAS}$	Colume address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

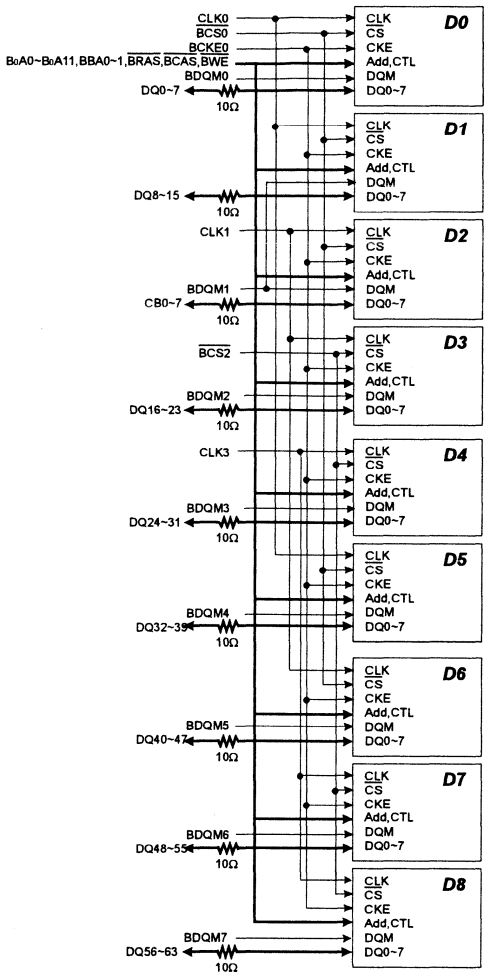
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

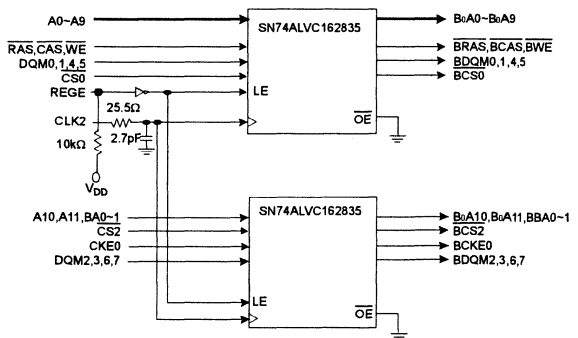
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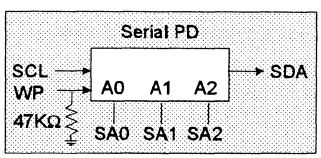
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	*Register enable*	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to V_{DD} through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
WP	*Write protection*	WP pin is connected to V_{SS} through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM

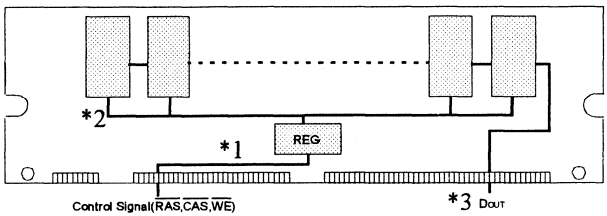


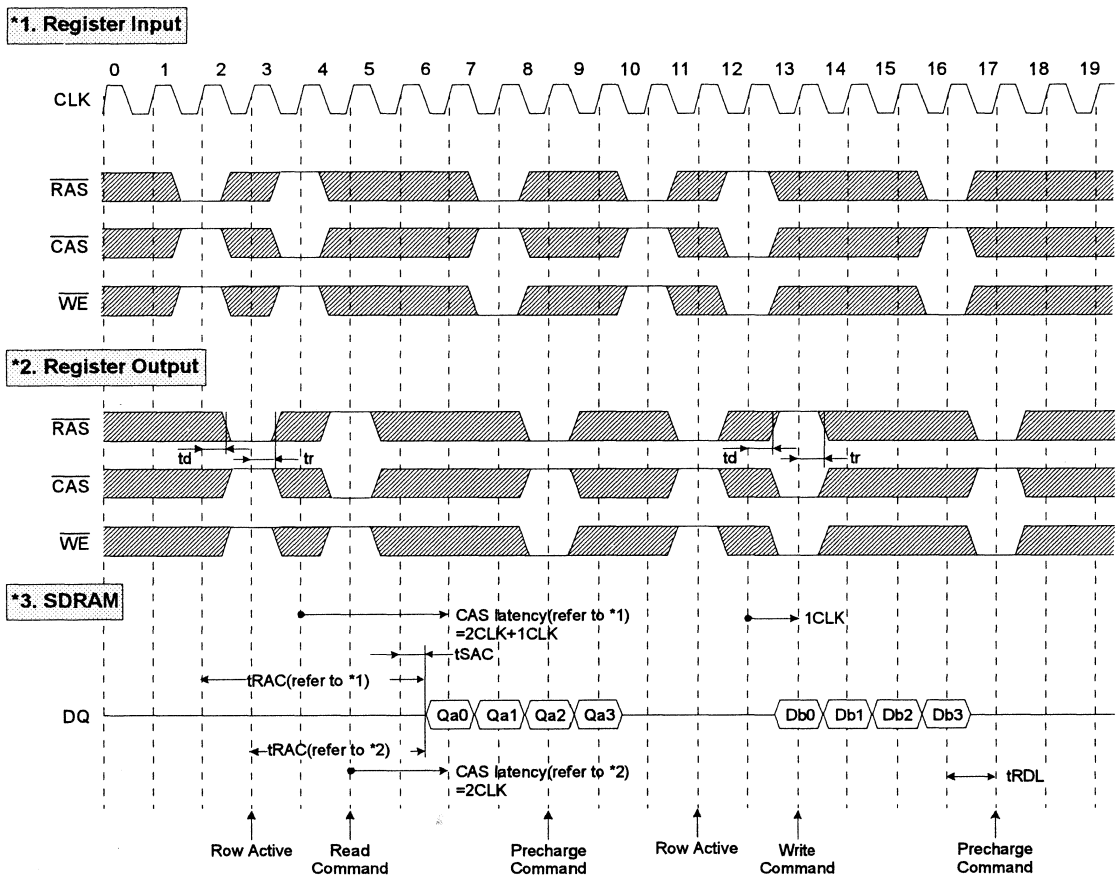




SAMSUNG ELECTRONICS

STANDARD TIMING DIAGRAM WITH REGISTER (CL=2, BL=4)





td, tr = Delay of register (SN74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (SN74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

: Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	9	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-2	-	2	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11})	C_{IN1}	-	16	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	16	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	-	16	pF
Input capacitance (CLK2)	C_{IN4}	-	18	pF
Input capacitance (CLK0,CLK1,CLK3)	C_{IN5}	-	22	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN6}	-	16	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN7}	-	16	pF
Input capacitance (BA0 ~ BA1)	C_{IN8}	-	16	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	17	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT1}	-	17	pF

DC CHARACTERISTICS

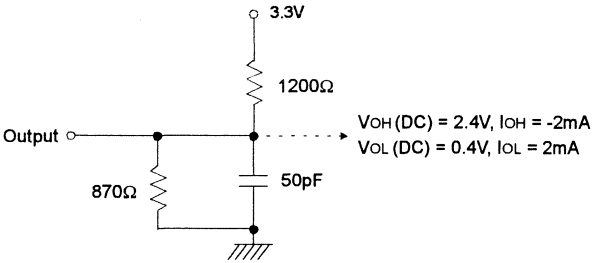
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-80	-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		775	730	730	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		10			mA	3
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		10				
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		109			mA	3
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		55				
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		19			mA	3
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		19				
Active standby current in non power-down mode	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		181			mA	3
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		91			mA	3
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0mA Page burst 2Banks activated t_{CCD}=2CLK	3	955	775	775	mA	1
			2	775	775	730		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,126			mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		10			mA	3

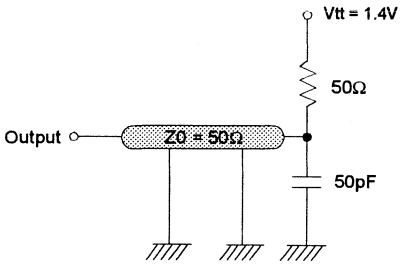
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Measured with 2 Drive ICs.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write in Reg. DIMM (1 CLK earlier than Unbuff. DIMM)
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		12		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6	ns	1,2
	CAS latency=2			6		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	1,2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	1
	CAS latency=2			6		6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes: 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

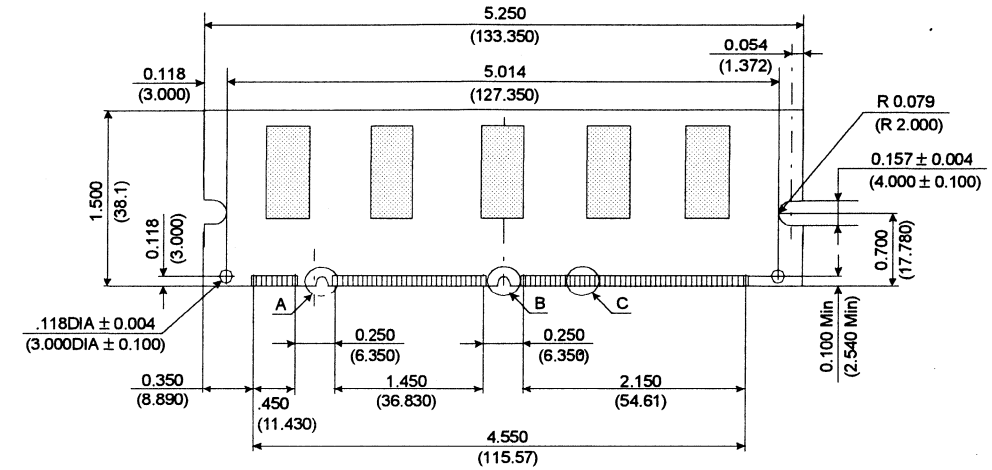
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

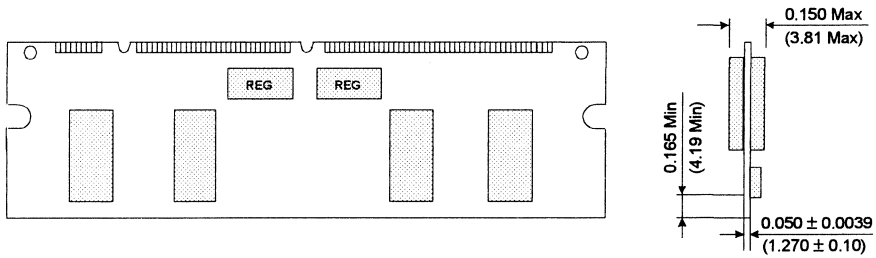
6. Burst stop command is valid at every burst length.

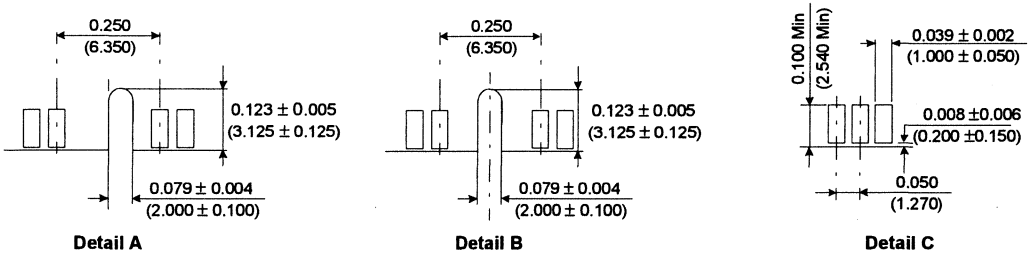
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)







Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832C

M350S0823CT1-C80/C1H/C1L(1.0ver)

- Organization : 8MX72
- Composition : 8MX8 *9
- Used component part # : K4S640832C-TC80/C1H/C1L
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,500 mil height & double sided component
- Refresh : 4K/64ms
- **Contents** :

Byte #	Function described	Function Supported			Hex value			Note
		-80	1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module Rows on this assembly	1 Row			01h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs			1Bh			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	1 Row of 64MB			10h			
32	Command and Address signal input setup time	2ns			20h			
33	Command and Address signal input hold time	1ns			10h			
34	Data signal input setup time	2ns			20h			

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns			10h			
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	Current release Intel spd 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			0Ch	32h	62h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	..... Manufacturer part # (Data bits)	5			35h			
77	..... Manufacturer part # (Data bits)	0			30h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	0			30h			
80	..... Manufacturer part # (Module depth)	8			38h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	C			43h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	1			31h			
86	Manufacturer part # (Hyphen)	"-"			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	1			31h			
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)			43h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	Intel Specification details	Detailed 100MHz Information			FDh	FFh	FDh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M377S0823CT1 SDRAM DIMM (Intel 1.0 ver. Base)

8Mx72 SDRAM DIMM with PLL & Register based on 8Mx8, 4Banks 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S0823CT1 is a 8M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung KMM377S823CT1 consists of nine CMOS 8Mx8 bit Synchronous DRAMs in TSOP-II 400mil packages, two 18-bits Drive ICs for input control signal and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168pin glass-epoxy substrate. One 0.22uF and two 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The KMM377S823CT1 is a Dual In-line Memory Module and is intented for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S0823CT1-C80	125MHz (8ns @ CL=3)
M377S0823CT1-G1H	100MHz (10ns @ CL=2)
M377S0823CT1-G1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,500mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	*CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Colume address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

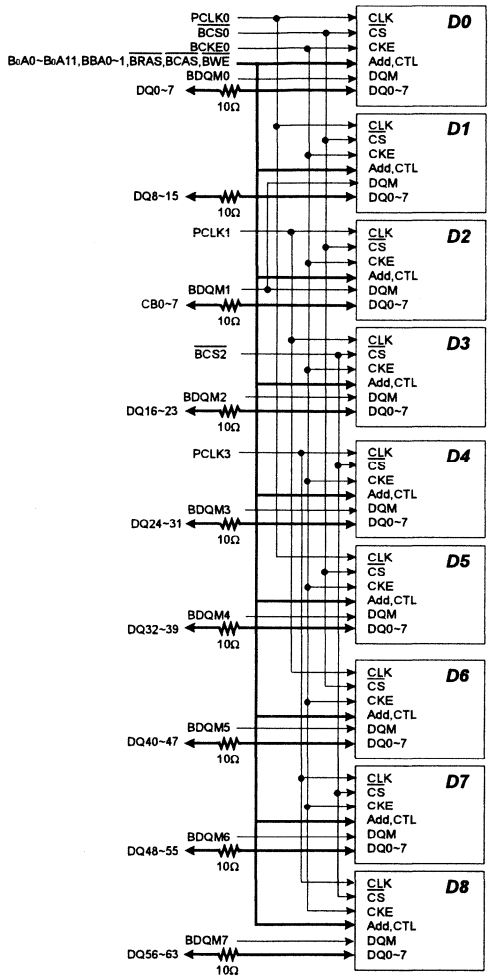
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

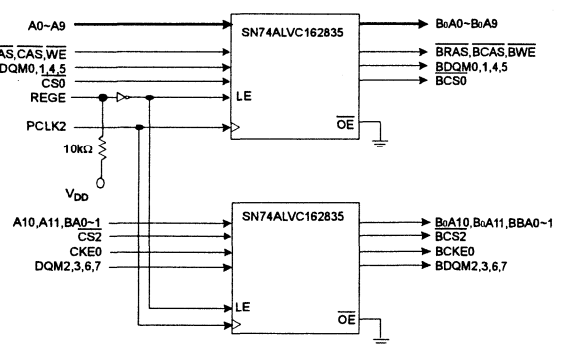
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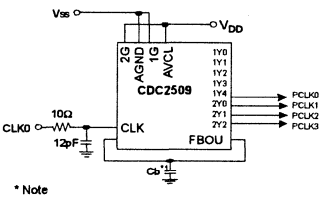
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	*Register enable*	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to V_{DD} through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
WP	*Write protection*	WP pin is connected to V_{SS} through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.

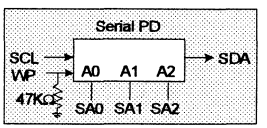
FUNCTIONAL BLOCK DIAGRAM



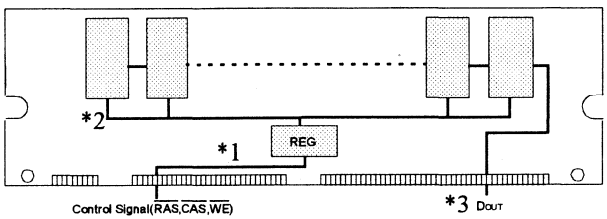


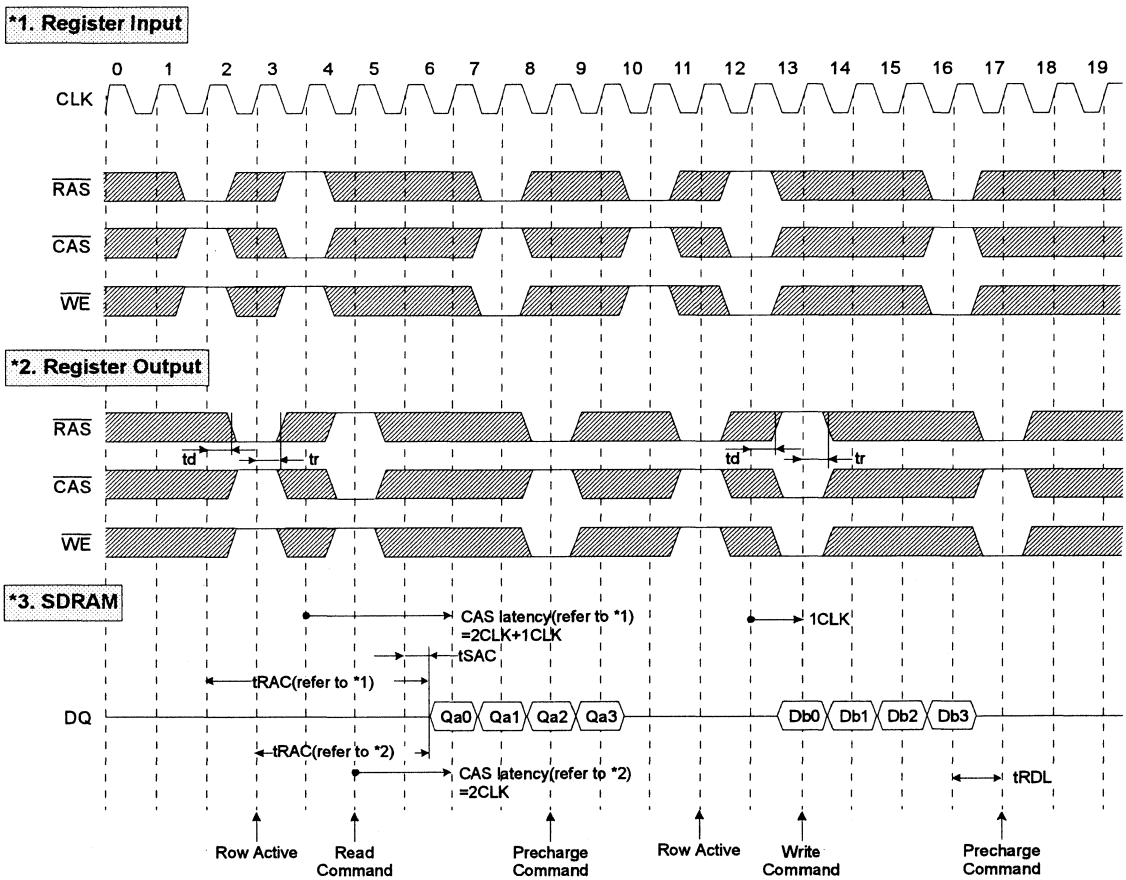


* Note
1. The actual values of Cb will depend upon the PLL chosen.



STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)





td, tr = Delay of register (SN74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (SN74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

: Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	9	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended Operating Conditions (Voltage Referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-2	-	2	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11})	C_{IN1}	-	16	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	16	pF
Input capacitance (CKE0)	C_{IN3}	-	16	pF
Input capacitance (CLK0)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	16	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	16	pF
Input capacitance (BA0 ~ BA1)	C_{IN7}	-	16	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	17	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT1}	-	17	pF

DC CHARACTERISTICS

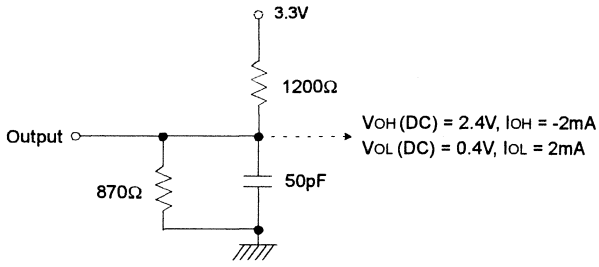
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-80	-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		825	780	780	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		11			mA	3
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		11				
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		110			mA	3
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		56				
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		20			mA	3
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		20				
Active standby current in non power-down mode	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		182			mA	3
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		92			mA	3
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0mA Page burst 2Banks activated t_{CCD}=2CLK	3	1,005	825	825	mA	1
			2	825	825	780		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,127			mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		11			mA	3

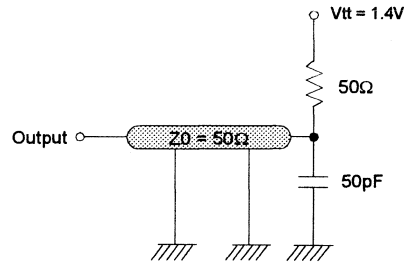
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Measured with 1 PLL & 2 Drive ICs.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter	Symbol	Version			Unit	Note
		-80	-1H	-1L		
Row active to row active delay	t_{RRD}(min)	16	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay	t_{RCD}(min)	20	20	20	ns	1
Row precharge time	t_{RP}(min)	20	20	20	ns	1
Row active time	t_{RAS}(min)	48	50	50	ns	1
	t_{RAS}(max)	100			us	
Row cycle time	t_{RC}(min)	68	70	70	ns	1
Last data in to new col. address delay	t_{CDL}(min)	1			CLK	2
Last data in to row precharge	t_{RDL}(min)	1			CLK	2
Last data in to burst stop	t_{BDL}(min)	1			CLK	2
Col. address to col. address delay	t_{CCD}(min)	1			CLK	3
Number of valid output data	CAS latency=3	2			ea	4
	CAS latency=2	1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write in Reg. DIMM (1 CLK earlier than Unbuff. DIMM)
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		10		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6	ns	1,2
	CAS latency=2			6		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	1,2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	1
	CAS latency=2			6		6		7		

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A8)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A8)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

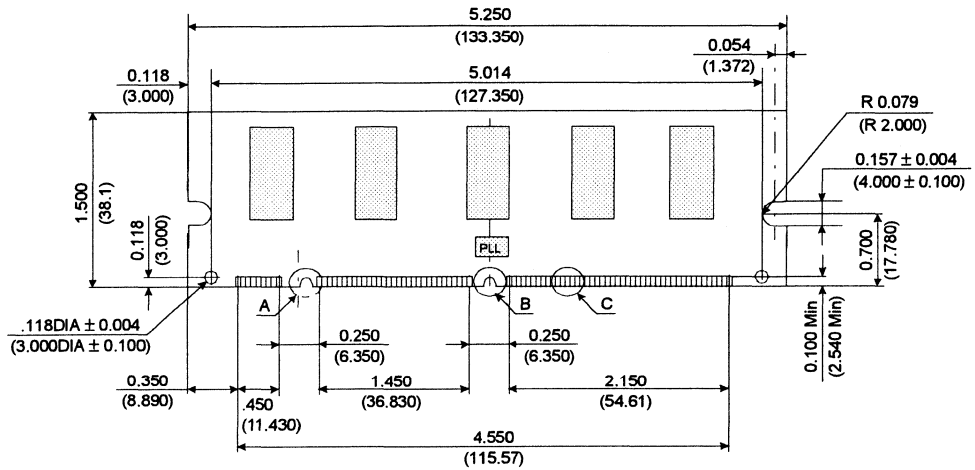
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

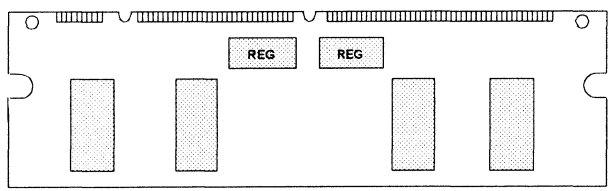
6. Burst stop command is valid at every burst length.

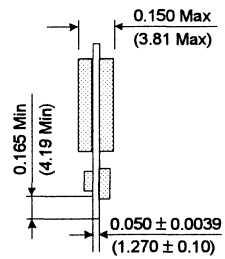
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

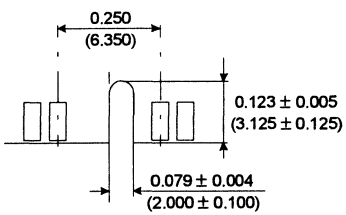
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

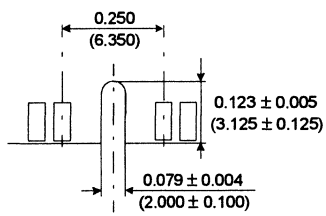




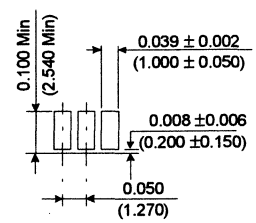




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832C

M377S0823CT1-C80/C1H/C1L(1.0ver)

- Organization : 8MX72
- Composition : 8MX8 *9
- Used component part # : K4S640832C-TC80/C1H/C1L
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,500 mil height & double sided component
- Refresh : 4K/64ms
- **Contents** :

Byte #	Function described	Function Supported			Hex value			Note
		-80	1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module Rows on this assembly	1 Row			01h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL			1Fh			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	1 Row of 64MB			10h			
32	Command and Address signal input setup time	2ns			20h			
33	Command and Address signal input hold time	1ns			10h			
34	Data signal input setup time	2ns			20h			

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns			10h			
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	Current release Intel spd 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			10h	36h	66h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	..... Manufacturer part # (Data bits)	7			37h			
77	..... Manufacturer part # (Data bits)	7			37h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	0			30h			
80	..... Manufacturer part # (Module depth)	8			38h			
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	C			43h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	1			31h			
86	Manufacturer part # (Hyphen)	"-"			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	1			31h			
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)			43h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	Intel Specification details	Detailed 100MHz Information			8Dh	8Fh	8Dh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M377S1620CT1 SDRAM DIMM (Intel 1.0 ver. Base)

16Mx72 SDRAM DIMM with PLL & Register based on 16Mx4, 4Banks 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S1620CT1 is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S1620CT1 consists of eighteen CMOS 16Mx4 bit Synchronous DRAMs in TSOP-II 400mil packages, three 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. One 0.22uF and two 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S1620CT1 is a Dual In-line Memory Module and is intented for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

•Performance range

Part No.	Max Freq. (Speed)
M377S1620CT1-C80	125MHz (8ns @ CL=3)
M377S1620CT1-C1H	100MHz (10ns @ CL=2)
M377S1620CT1-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,700mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	*CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Colume address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

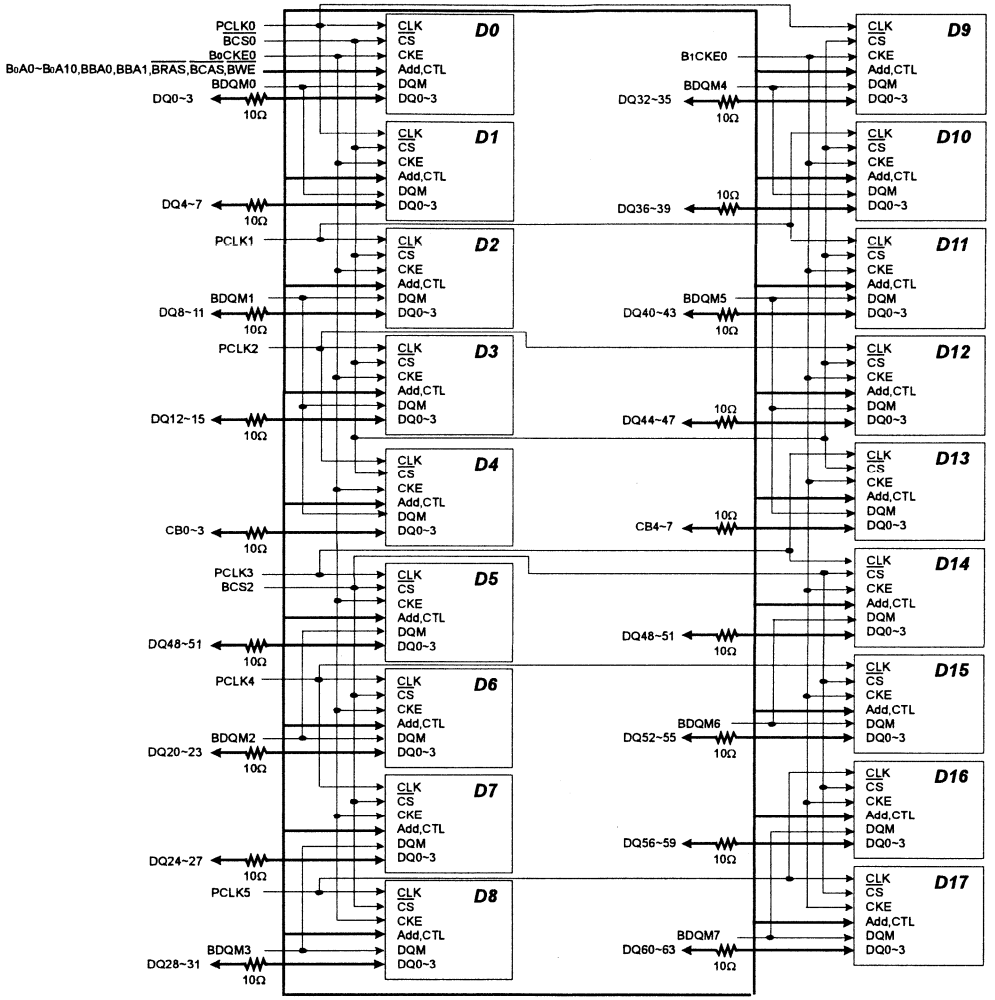
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

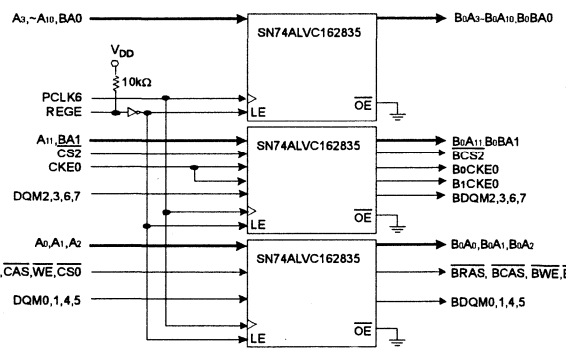
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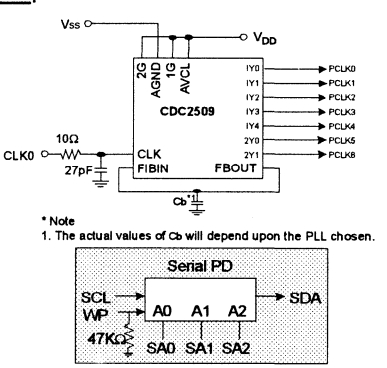
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	*Register enable*	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to V_{DD} through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
WP	*Write protection*	WP pin is connected to V_{SS} through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM

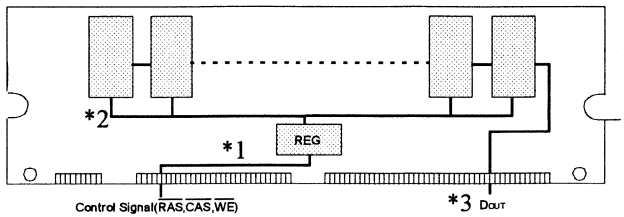


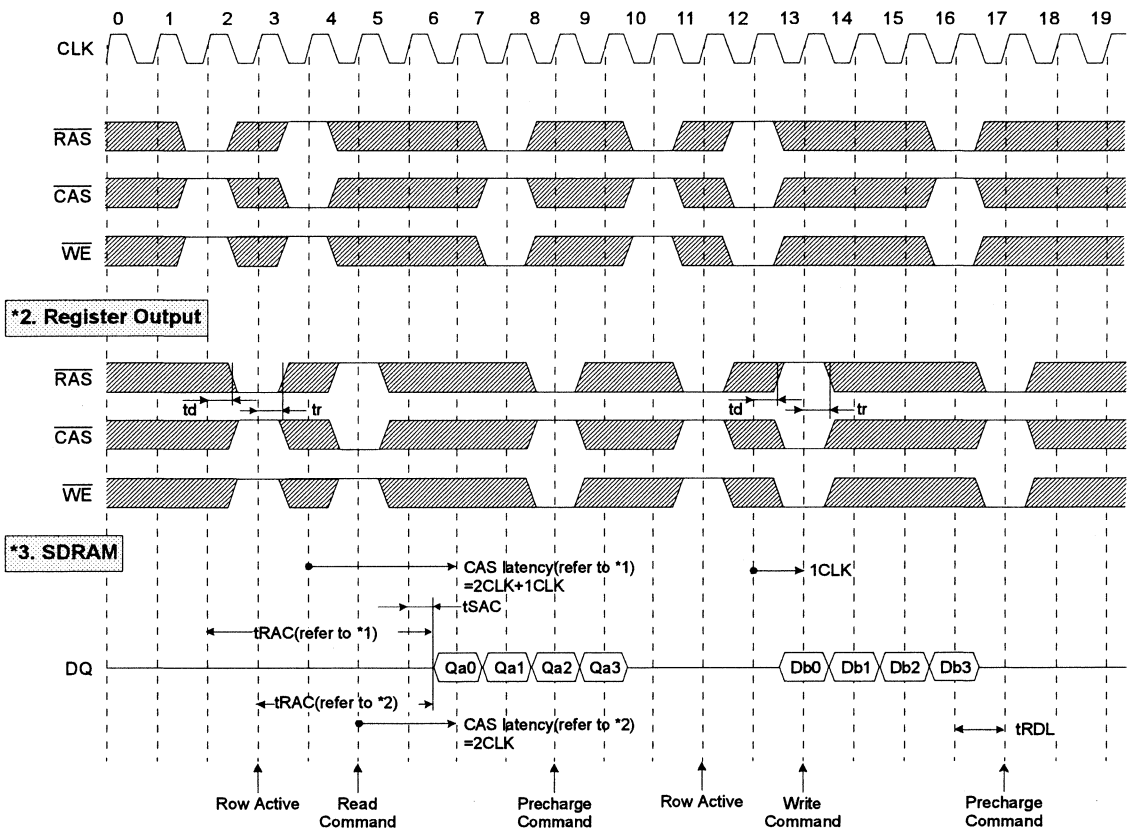




SAMSUNG ELECTRONICS

STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)





td, tr = Delay of register (SN74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (SN74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

: Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	18	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-3	-	3	uA	3
Input leakage current (I/O Pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11})	C_{IN1}	-	16	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	16	pF
Input capacitance (CKE0)	C_{IN3}	-	22	pF
Input capacitance (CLK0)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	16	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	16	pF
Input capacitance (BA0 ~ BA1)	C_{IN7}	-	16	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	17	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT1}	-	17	pF

DC CHARACTERISTICS

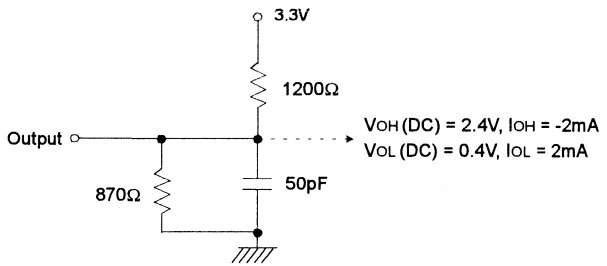
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-80	-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1,550	1,460	1,460	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		20			mA	3
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		20				
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		218			mA	3
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		110				
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		38			mA	3
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		38				
Active Standby current in non power-down mode	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		362			mA	3
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		182			mA	3
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0mA Page burst 2 Banks activated t_{CCD}=2CLK	3	1,910	1,550	1,550	mA	1
			2	1,550	1,550	1,460		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		2,250			mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		20			mA	3

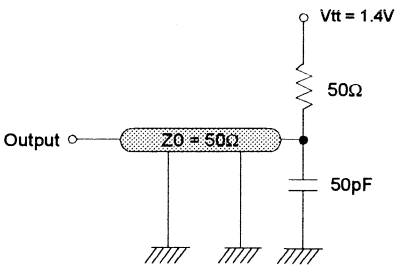
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Measured with 1 PLL & 3 Drive ICs.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write in Reg. DIMM (1 CLK earlier than Unbuff. DIMM)
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		10		10		12			
CLK to valid output delay	CAS latency=3	t_{SAC}		6		6		6	ns	1,2
	CAS latency=2			6		6		7		
Output data hold time	CAS latency=3	t_{OH}	3		3		3		ns	1,2
	CAS latency=2		3		3		3			
CLK high pulse width		t_{CH}	3		3		3		ns	3
CLK low pulse width		t_{CL}	3		3		3		ns	3
Input setup time		t_{SS}	2		2		2		ns	3
Input hold time		t_{SH}	1		1		1		ns	3
CLK to output in Low-Z		t_{SLZ}	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		6		6		6	ns	1
	CAS latency=2			6		6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, A_9 ~ A_0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A_0 ~ A_9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A_0 ~ A_9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Notes : 1. OP Code : Operand code
A_0 ~ A_{11} & BA_0 ~ BA_1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA_0 ~ BA_1 : Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

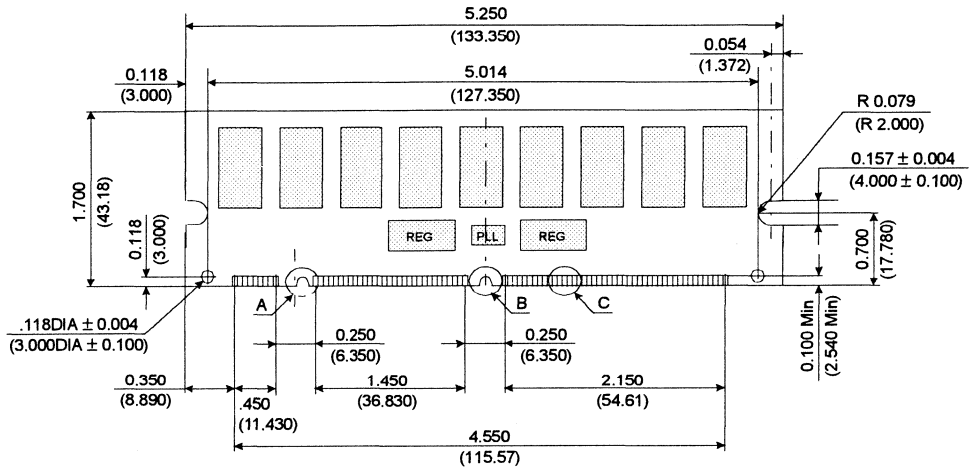
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

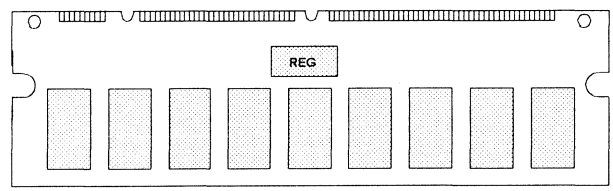
6. Burst stop command is valid at every burst length.

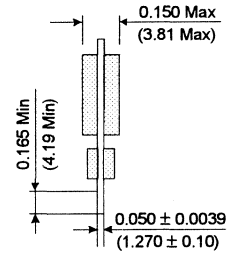
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

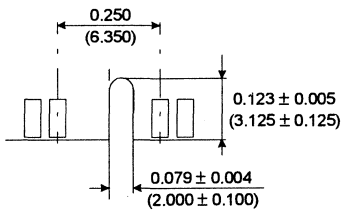
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

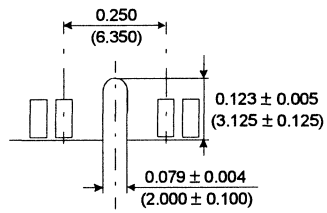




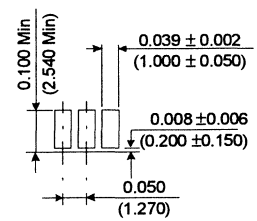




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 16Mx4 SDRAM, TSOP
SDRAM Part No. : K4S640432C

M377S1620CT1-C80/C1H/C1L(1.0ver)

- Organization : 16MX72
- Composition : 16MX4 *18
- Used component part # : K4S640432C-TC80/C1H/C1L
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 4K/64ms
- **Contents** :

Byte #	Function described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	1 Row			01h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x4			04h			
14	Error checking SDRAM width	x4			04h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL			1Fh			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	1 Row of 128MB			20h			
32	Command and Address signal input setup time	2ns			20h			
33	Command and Address signal input hold time	1ns			10h			
34	Data signal input setup time	2ns			20h			

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns			10h			
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	Current release Intel spd 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			19h	3Fh	6Fh	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	..... Manufacturer part # (Data bits)	7			37h			
77	..... Manufacturer part # (Data bits)	7			37h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	1			31h			
80	..... Manufacturer part # (Module depth)	6			36h			
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2			32h			
82	Manufacturer part # (Composition component)	0			30h			
83	Manufacturer part # (Component revision)	C			43h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	1			31h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	1			31h			
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)			43h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	Intel Specification details	Detailed 100MHz Information			8Dh	8Fh	8Dh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M377S0823CT2 SDRAM DIMM (Intel 1.1 ver. Base)

8Mx72 SDRAM DIMM with PLL & Register based on 8Mx8, 4Banks 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S0823CT2 is a 8M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S0823CT2 consists of nine CMOS 8Mx8 bit Synchronous DRAMs in TSOP-II 400mil packages, two 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S0823CT2 is a Dual In-line Memory Module and is intented for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high band-width, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S0823CT2-C1H	100MHz (10ns @ CL=2)
M377S0823CT2-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,500mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	*CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Colume address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

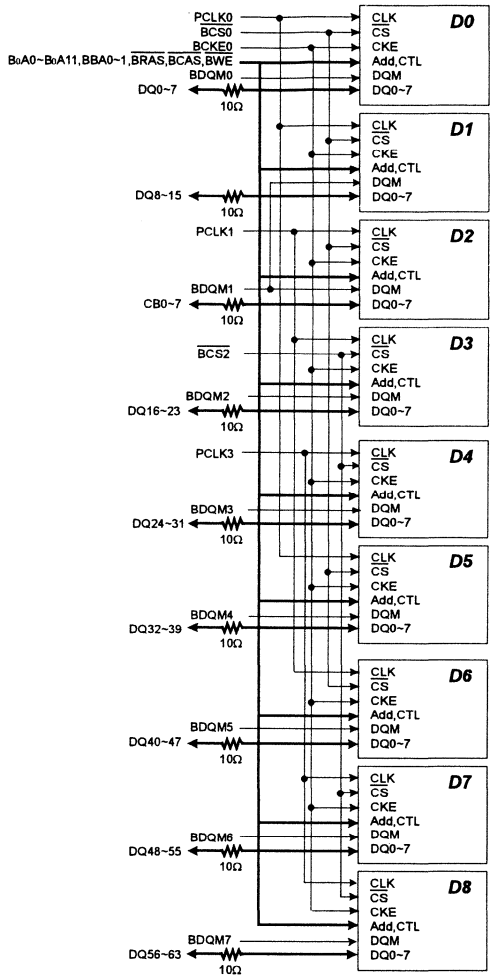
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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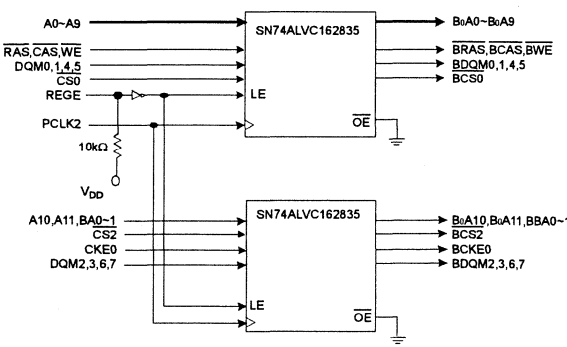
PIN CONFIGURATION DESCRIPTION

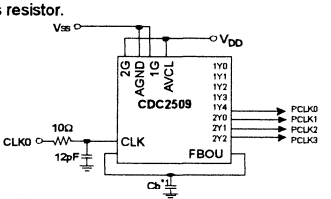
Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	*Register enable*	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to V_{DD} through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
WP	*Write protection*	WP pin is connected to V_{SS} through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM

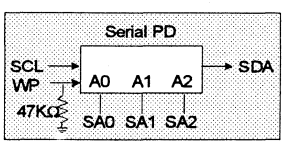


Notes : Address/Control Signals are connected to D2 through 100 ohms resistor.



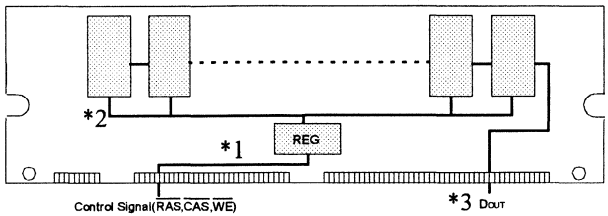


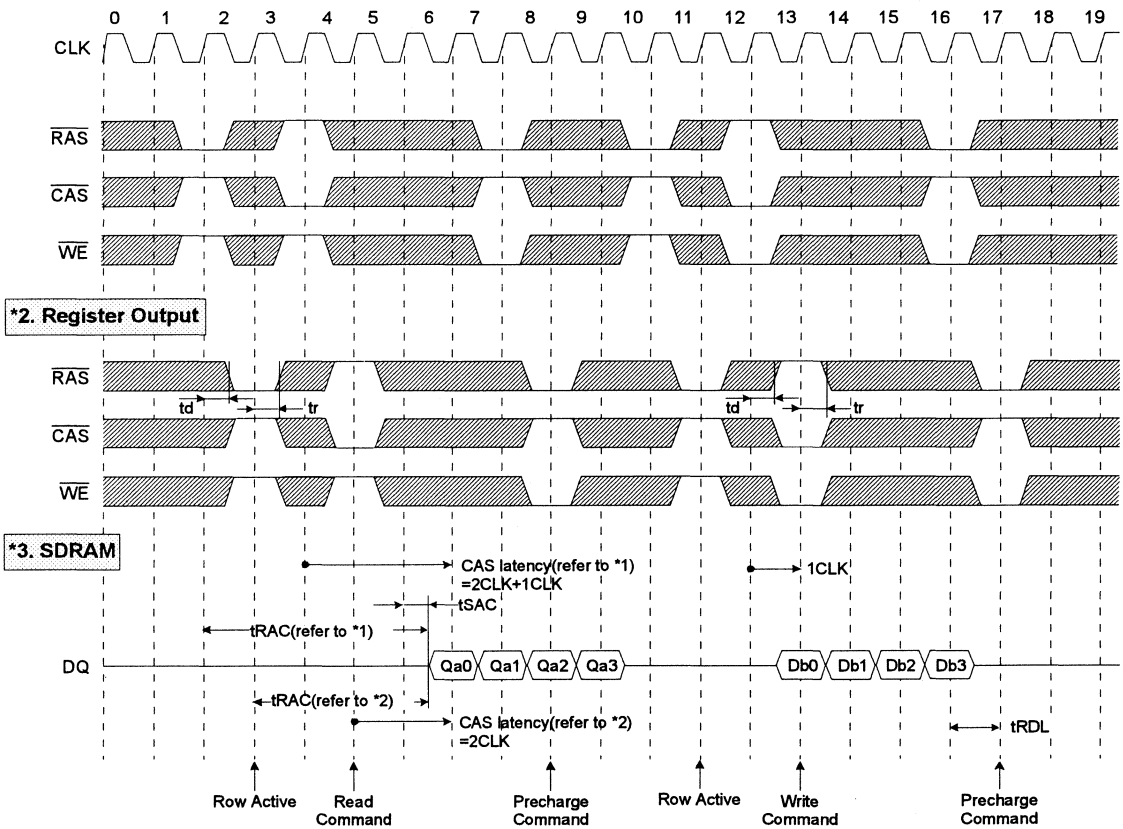
* Note
1. The actual values of Cb will depend upon the PLL chosen.



SAMSUNG ELECTRONICS

STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)





td, tr = Delay of register (SN74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (SN74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

: Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	9	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended Operating Conditions (Voltage Referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-2	-	2	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11})	C_{IN1}	-	15	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	15	pF
Input capacitance (CKE0)	C_{IN3}	-	15	pF
Input capacitance (CLK0)	C_{IN4}	-	26	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	15	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	15	pF
Input capacitance (BA0 ~ BA1)	C_{IN7}	-	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	17	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT1}	-	17	pF

DC CHARACTERISTICS

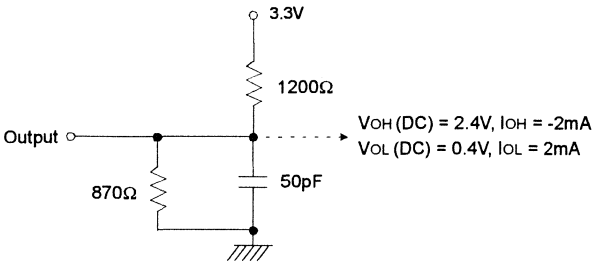
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -1H	Version -1L	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		780	780	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		11		mA	3
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		11			
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		110		mA	3
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		56			
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		20		mA	3
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		20			
Active standby current in non power-down mode	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		182		mA	3
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		92		mA	3
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0mA Page burst 2Banks activated t_{CCD}=2CLK	3	825	825	mA	1
			2	825	780		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,126		mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		11		mA	3

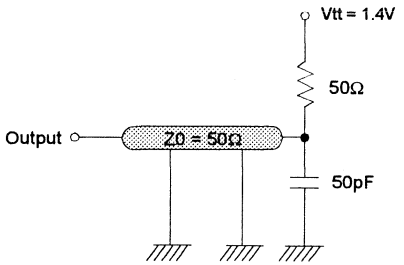
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Measured with 1 PLL & 2 Drive ICs.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		t_{RRD}(min)	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		t_{RCD}(min)	20	20	ns	1
Row precharge time		t_{RP}(min)	20	20	ns	1
Row active time		t_{RAS}(min)	50	50	ns	1
		t_{RAS}(max)	100		us	
Row cycle time		t_{RC}(min)	70	70	ns	1
Last data in to new col. address delay		t_{CDL}(min)	1		CLK	2
Last data in to row precharge		t_{RDL}(min)	1		CLK	2
Last data in to burst stop		t_{BDL}(min)	1		CLK	2
Col. address to col. address delay		t_{CCD}(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write in Reg. DIMM (1 CLK earlier than Unbuff. DIMM)
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	t_{SAC}		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	t_{OH}	3		3		ns	1,2
	CAS latency=2		3		3			
CLK high pulse width		t_{CH}	3		3		ns	3
CLK low pulse width		t_{CL}	3		3		ns	3
Input setup time		t_{SS}	2		2		ns	3
Input hold time		t_{SH}	1		1		ns	3
CLK to output in Low-Z		t_{SLZ}	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		6		6	ns	1
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A8)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A8)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

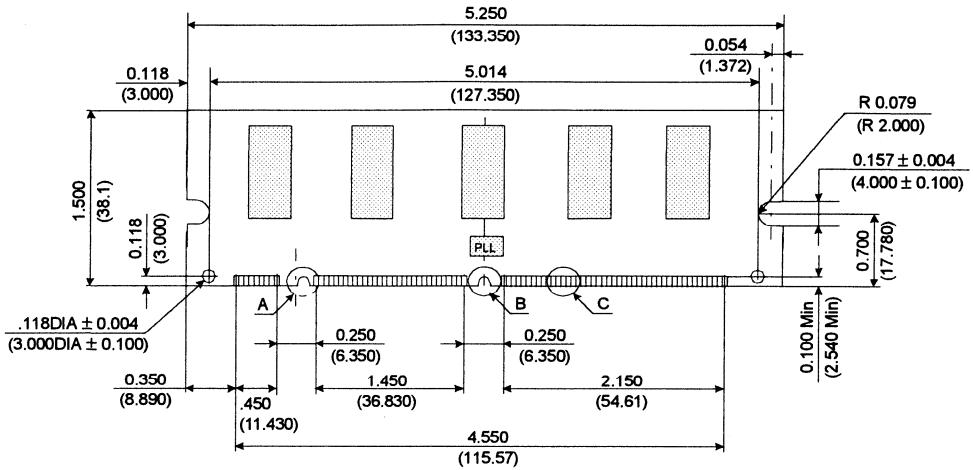
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

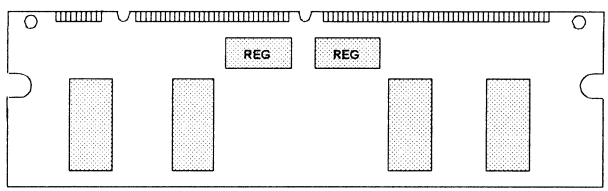
6. Burst stop command is valid at every burst length.

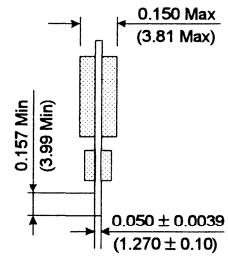
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

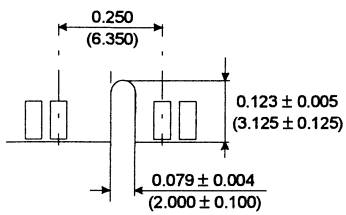
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

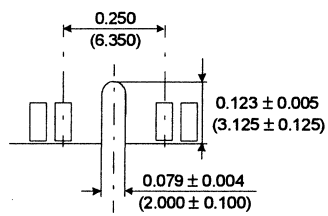




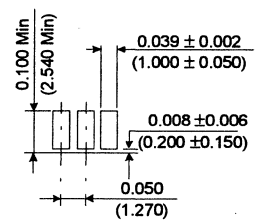




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832C

M377S0823CT2-C1H/C1L(1.1ver)

- Organization : 8MX72
- Composition : 8MX8 *9
- Used component part # : K4S640832C-TC1H/C1L
- # of banks in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,500 mil height & double sided component
- Refresh : 4K/64ms
- **Contents** :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	9		09h		1
5	# of module Rows on this assembly	1 Row		01h		
6	Data width of this assembly	72 bits		48h		
7	..... Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x8		08h		
14	Error checking SDRAM width	x8		08h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	1 Row of 64MB		10h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		36h	66h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	..... Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	..... Manufacturer part # (Data bits)	7		37h		
77	..... Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	0		30h		
80	..... Manufacturer part # (Module depth)	8		38h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	3		33h		
83	Manufacturer part # (Component revision)	C		43h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	2		32h		
86	Manufacturer part # (Hyphen)	"-"		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	2		32h		
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)		43h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M377S1620CT2 SDRAM DIMM (Intel 1.1 ver. Base)

16Mx72 SDRAM DIMM with PLL & Register based on 16Mx4, 4Banks, 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S1620CT2 is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S1620CT2 consists of eighteen CMOS 16Mx4 bit Synchronous DRAMs in TSOP-II 400mil packages, three 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S1620CT2 is a Dual In-line Memory Module and is intented for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S1620CT2-C1H	100MHz (10ns @ CL=2)
M377S1620CT2-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,700mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	*CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

.PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Colume address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

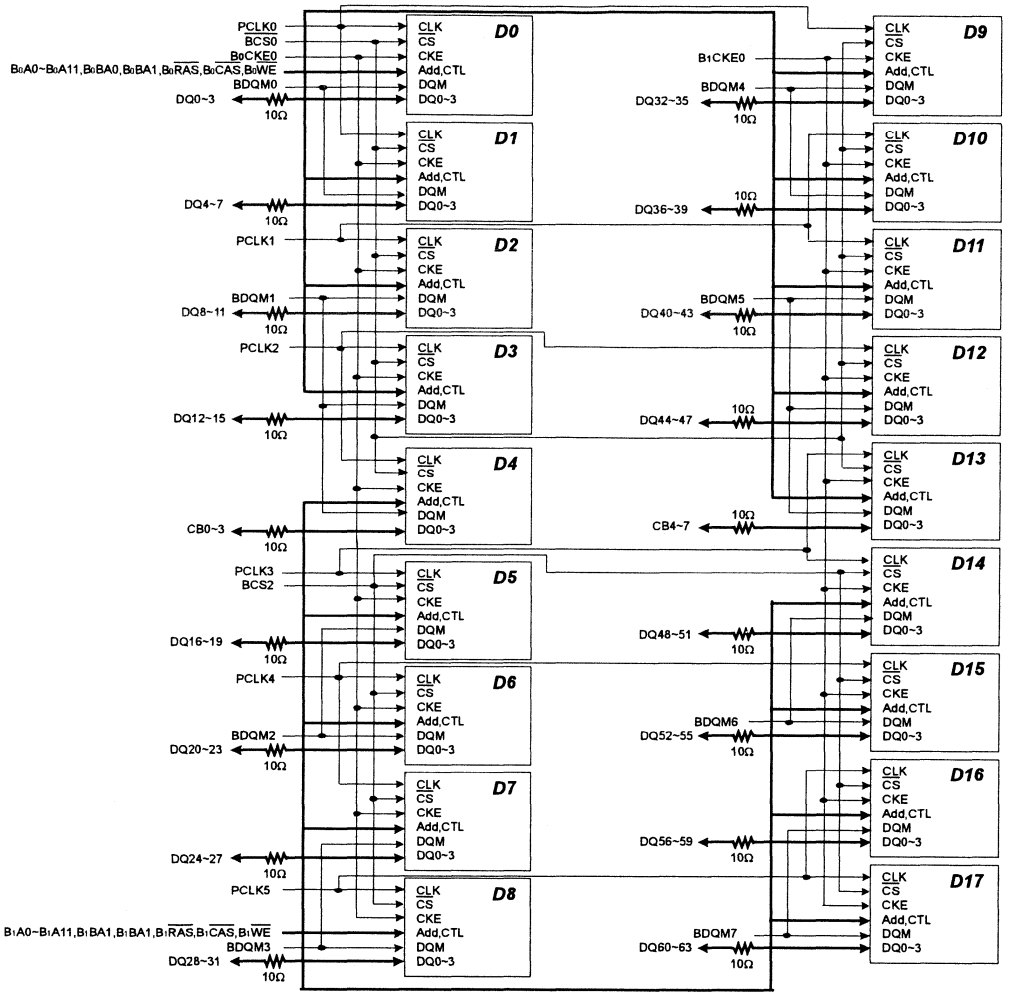
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

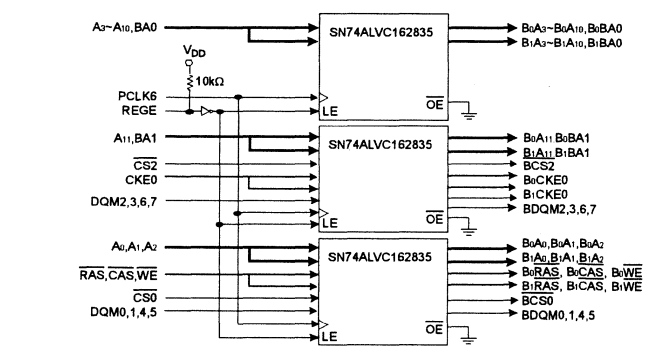
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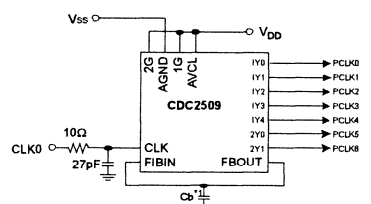
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	*Register enable*	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to V_{DD} through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
WP	*Write protection*	WP pin is connected to V_{SS} through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.

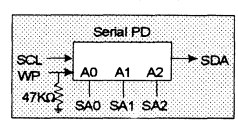
FUNCTIONAL BLOCK DIAGRAM



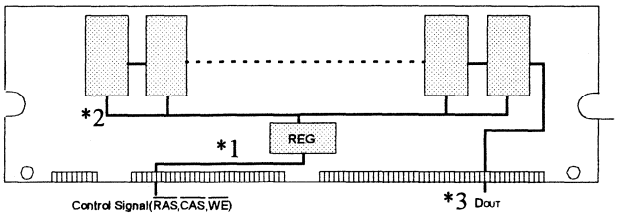


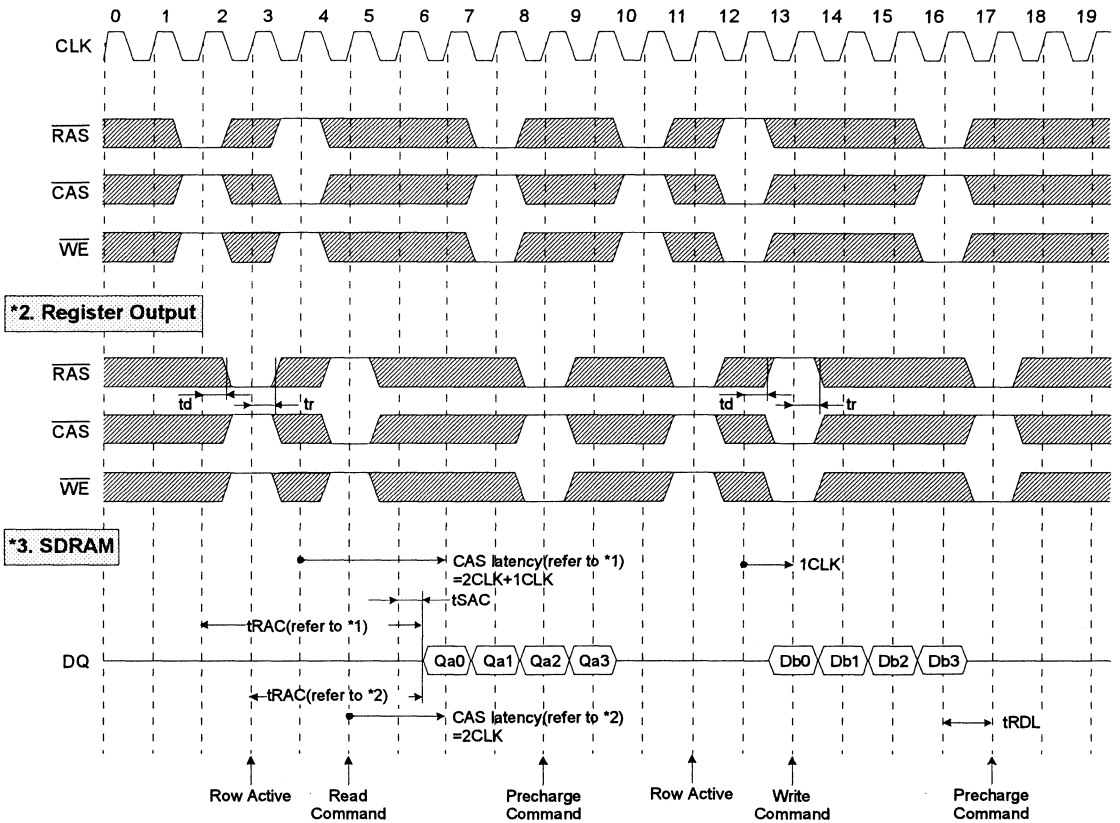


* Note
1. The actual values of Cb will depend upon the PLL chosen.



STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)





td, tr = Delay of register (SN74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (SN74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

: Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	18	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-3	-	3	uA	3
Input leakage current (I/O Pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11})	C_{IN1}	-	20	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	20	pF
Input capacitance (CKE0)	C_{IN3}	-	20	pF
Input capacitance (CLK0)	C_{IN4}	-	26	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	15	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	15	pF
Input capacitance (BA0 ~ BA1)	C_{IN7}	-	20	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	17	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT1}	-	17	pF

DC CHARACTERISTICS

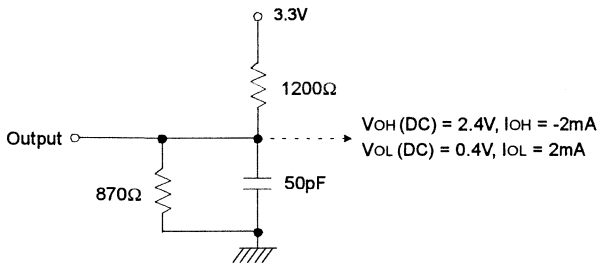
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version		Unit	Note
				-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1,370	1,370	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		20		mA	3
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		20		mA	
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		218		mA	3
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		110			
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		38		mA	3
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		38			
Active Standby current in non power-down mode	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		362		mA	3
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		182		mA	3
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0mA Page burst 2 Banks activated t_{CCD}=2CLK	3	1,370	1,370	mA	1
			2	1,370	1,280		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		2,450		mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		20		mA	3

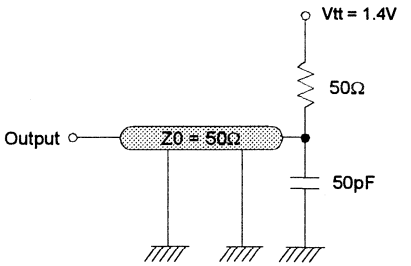
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Measured with 1 PLL & 3 Drive ICs.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to row precharge		tRDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write in Reg. DIMM (1 CLK earlier than Unbuff. DIMM)
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	1,2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	1
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_9$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_9$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

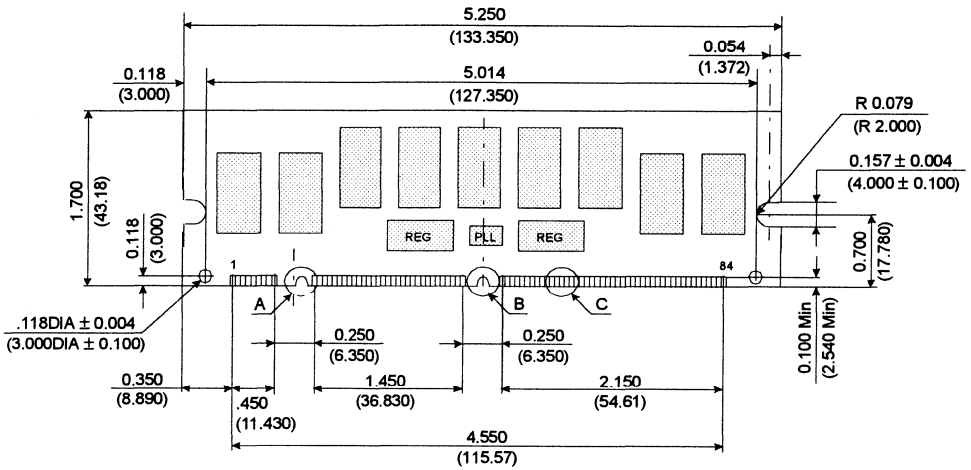
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

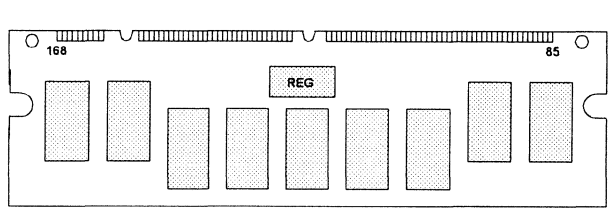
6. Burst stop command is valid at every burst length.

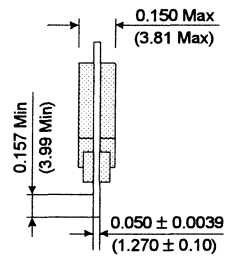
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

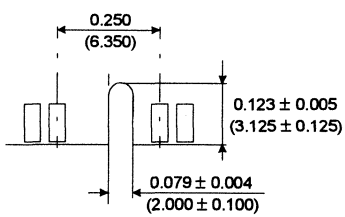
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

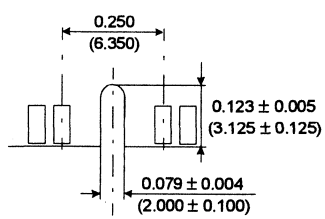




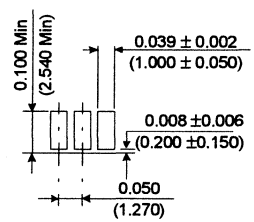




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 16Mx4 SDRAM, TSOP
SDRAM Part No. : K4S640432C

M377S1620CT2-C1H/C1L(1.1ver)

- Organization : 16MX72
- Composition : 16MX4 *18
- Used component part # : K4S640432C-TC1H/C1L
- # of banks in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 4K/64ms
- **Contents** :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	10		0Ah		1
5	# of module Rows on this assembly	1 Row		01h		
6	Data width of this assembly	72 bits		48h		
7	..... Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x4		04h		
14	Error checking SDRAM width	x4		04h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	1 Row of 128MB		20h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		3Fh	6Fh	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	..... Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	..... Manufacturer part # (Data bits)	7		37h		
77	..... Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	1		31h		
80	..... Manufacturer part # (Module depth)	6		36h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	0		30h		
83	Manufacturer part # (Component revision)	C		43h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	2		32h		
86	Manufacturer part # (Hyphen)	"-"		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	2		32h		
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)		43h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M377S0823CT3 SDRAM DIMM (Intel 1.2 ver. Base)

8Mx72 SDRAM DIMM with PLL & Register based on 8Mx8, 4Banks 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S0823CT3 is a 8M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S0823CT3 consists of nine CMOS 8Mx8 bit Synchronous DRAMs in TSOP-II 400mil packages, two 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S0823CT3 is a Dual In-line Memory Module and is intented for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high band-width, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S0823CT3-C1H	100MHz (10ns @ CL=2)
M377S0823CT3-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,500mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	*CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Colume address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

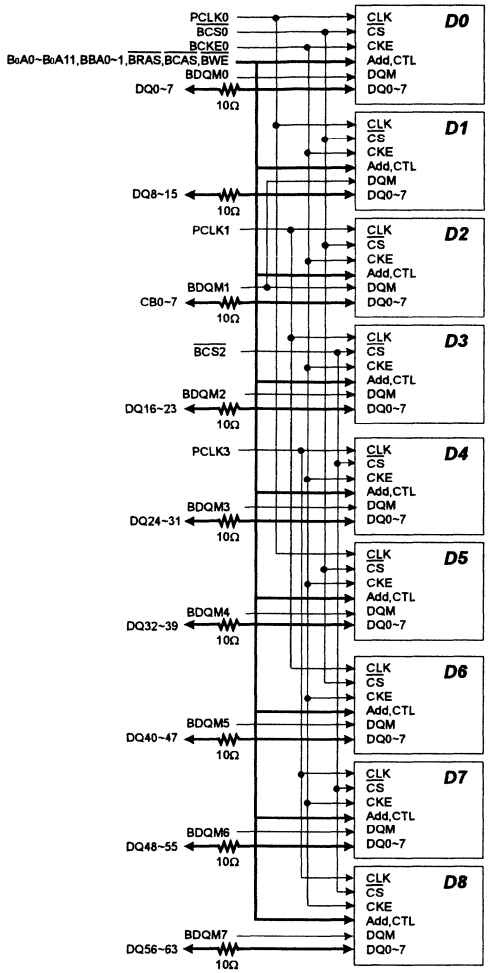
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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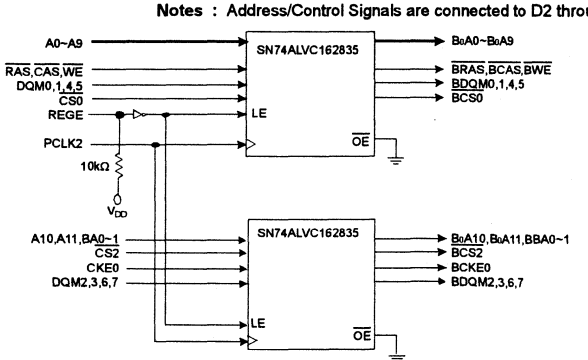
PIN CONFIGURATION DESCRIPTION

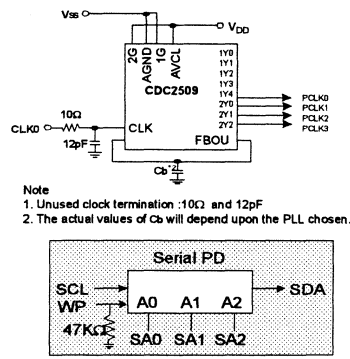
Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	*Register enable*	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to V_{DD} through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
WP	*Write protection*	WP pin is connected to V_{SS} through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



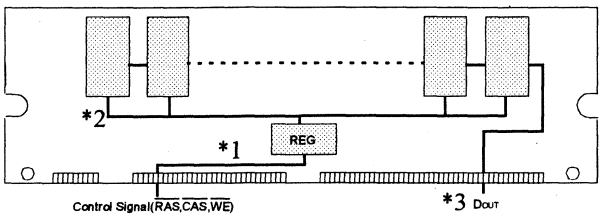
Notes : Address/Control Signals are connected to D2 through 100 ohms resistor.

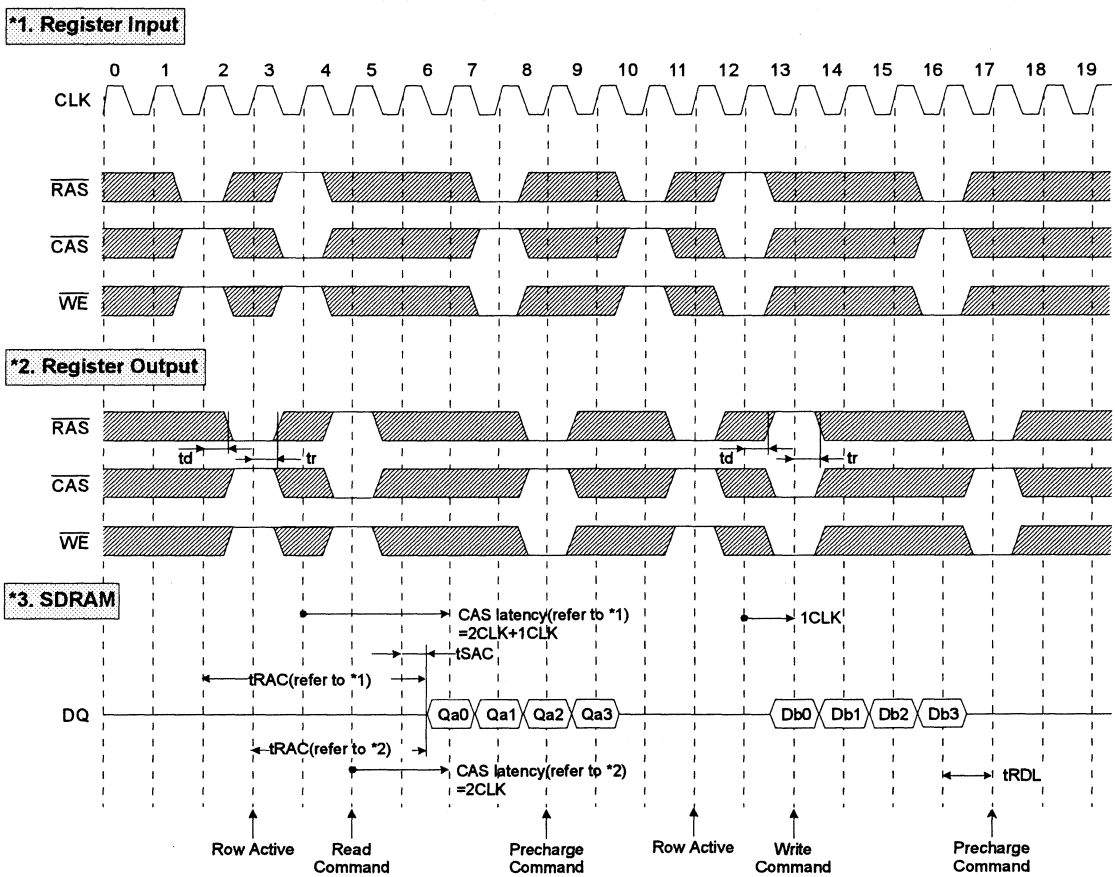




Note
1. Unused clock termination :10Ω and 12pF
2. The actual values of Cb will depend upon the PLL chosen.

STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)





td, tr = Delay of register (SN74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (SN74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

: Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	9	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended Operating Conditions (Voltage Referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-2	-	2	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11})	C_{IN1}	-	15	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	15	pF
Input capacitance (CKE0)	C_{IN3}	-	15	pF
Input capacitance (CLK0)	C_{IN4}	-	26	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	15	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	15	pF
Input capacitance (BA0 ~ BA1)	C_{IN7}	-	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	17	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT1}	-	17	pF

DC CHARACTERISTICS

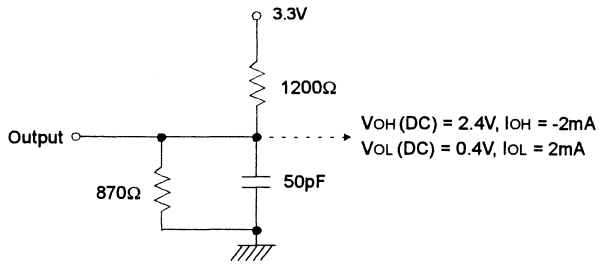
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version		Unit	Note
				-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		780	780	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		11		mA	3
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		11			
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		110		mA	3
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		56			
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		20		mA	3
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		20			
Active standby current in non power-down mode	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		182		mA	3
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		92		mA	3
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0mA Page burst 2Banks activated t_{CCD}=2CLK	3	825	825	mA	1
			2	825	780		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,126		mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		11		mA	3

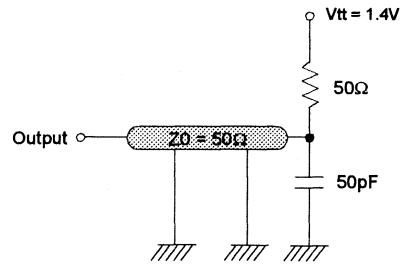
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Measured with 1 PLL & 2 Drive ICs.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to row precharge		tRDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write in Reg. DIMM (1 CLK earlier than Unbuff. DIMM)
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	t_{SAC}		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	t_{OH}	3		3		ns	1,2
	CAS latency=2		3		3			
CLK high pulse width		t_{CH}	3		3		ns	3
CLK low pulse width		t_{CL}	3		3		ns	3
Input setup time		t_{SS}	2		2		ns	3
Input hold time		t_{SH}	1		1		ns	3
CLK to output in Low-Z		t_{SLZ}	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		6		6	ns	1
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

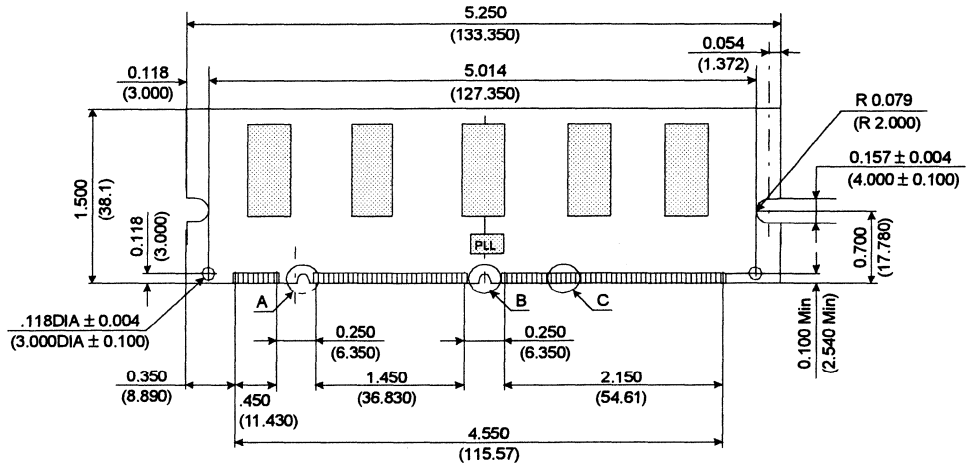
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

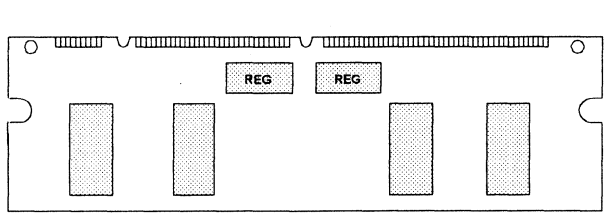
6. Burst stop command is valid at every burst length.

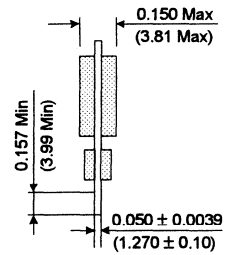
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

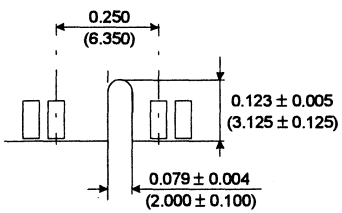
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

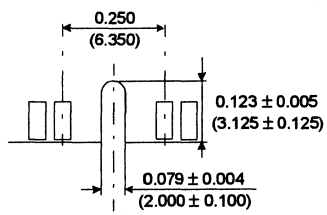




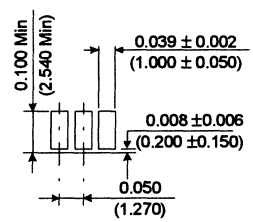




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832C

M377S0823CT3-C1H/C1L(1.2ver)

- Organization : 8MX72
- Composition : 8MX8 *9
- Used component part # : K4S640832C-TC1H/C1L
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,500 mil height & double sided component
- Refresh : 4K/64ms
- **Contents** :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	9		09h		1
5	# of module Rows on this assembly	1 Row		01h		
6	Data width of this assembly	72 bits		48h		
7	..... Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x8		08h		
14	Error checking SDRAM width	x8		08h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	1 Row of 64MB		10h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		36h	66h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	..... Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	..... Manufacturer part # (Data bits)	7		37h		
77	..... Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	0		30h		
80	..... Manufacturer part # (Module depth)	8		38h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	3		33h		
83	Manufacturer part # (Component revision)	C		43h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	3		33h		
86	Manufacturer part # (Hyphen)	"-"		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	3		33h		
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)		43h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M377S1620CT3 SDRAM DIMM (Intel 1.2 ver. Base)

16Mx72 SDRAM DIMM with PLL & Register based on 16Mx4, 4Banks, 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S1620CT3 is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S1620CT3 consists of eighteen CMOS 16Mx4 bit Synchronous DRAMs in TSOP-II 400mil packages, three 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S1620CT3 is a Dual In-line Memory Module and is intented for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S1620CT3-C1H	100MHz (10ns @ CL=2)
M377S1620CT3-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,700mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	*CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

.PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Colume address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

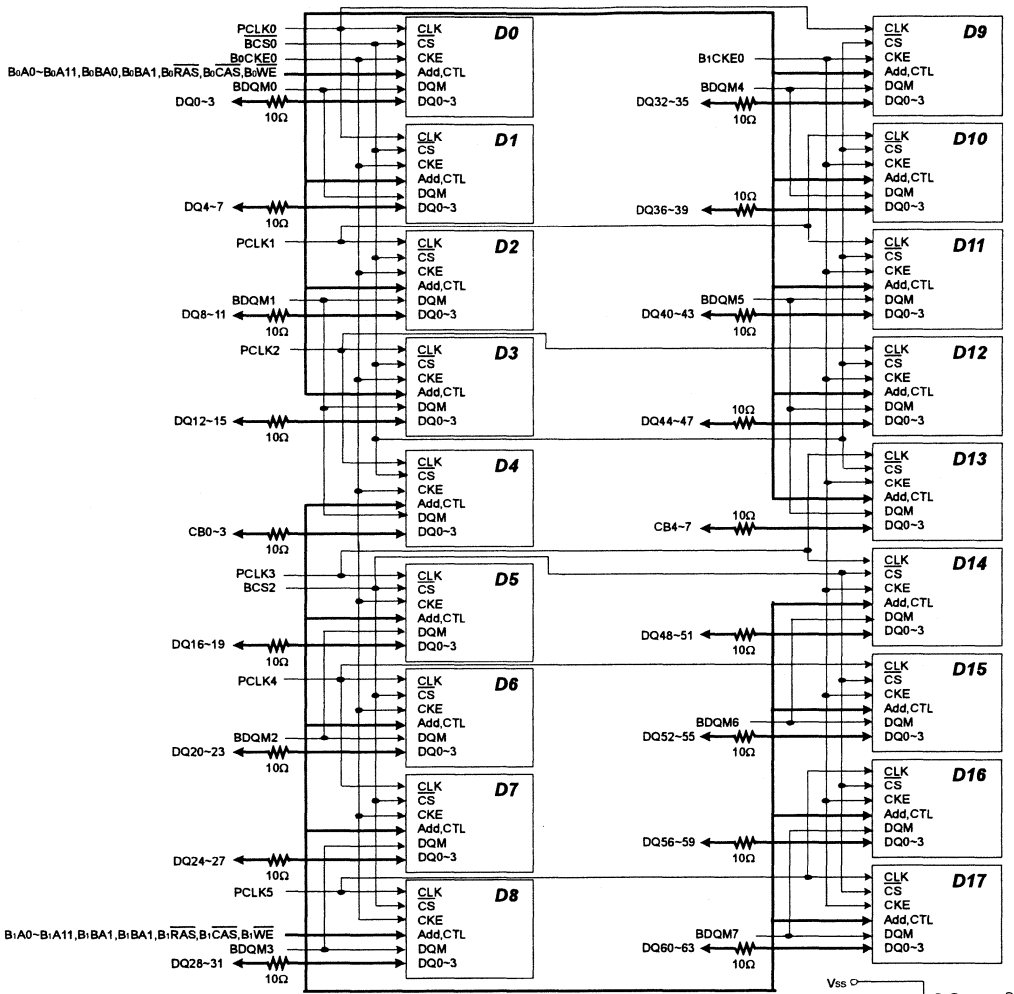
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

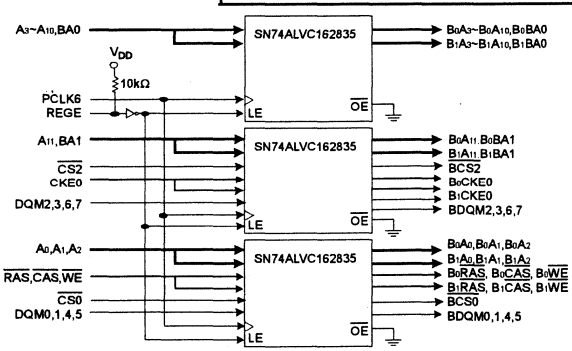
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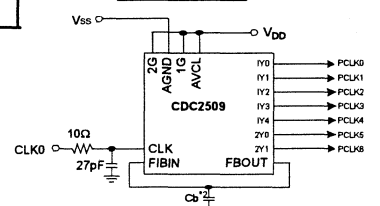
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	*Register enable*	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to V_{DD} through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
WP	*Write protection*	WP pin is connected to V_{SS} through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.

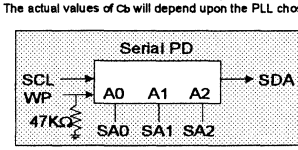
FUNCTIONAL BLOCK DIAGRAM





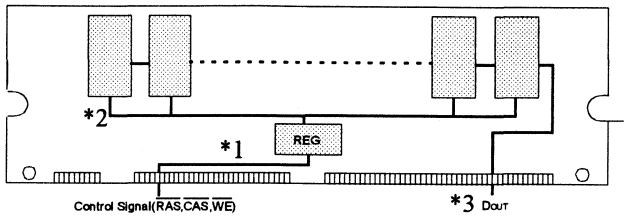


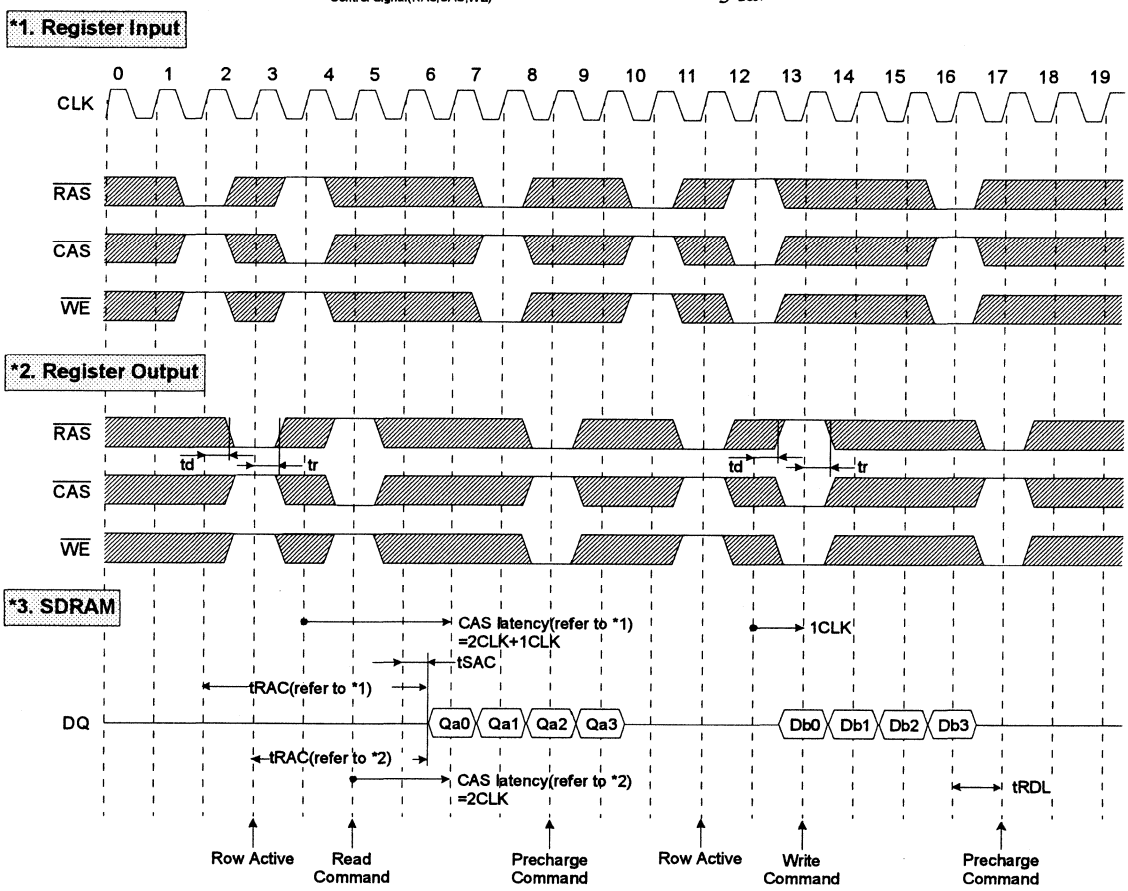
* Note
1. Unused clock termination : 10Ω and 12pF
2. The actual values of Cb will depend upon the PLL chosen.



SAMSUNG ELECTRONICS

STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)





td, tr = Delay of register (SN74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (SN74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

: Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	18	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-3	-	3	uA	3
Input leakage current (I/O Pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11})	C_{IN1}	-	20	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	20	pF
Input capacitance (CKE0)	C_{IN3}	-	20	pF
Input capacitance (CLK0)	C_{IN4}	-	26	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	15	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	15	pF
Input capacitance (BA0 ~ BA1)	C_{IN7}	-	20	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	17	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT1}	-	17	pF

DC CHARACTERISTICS

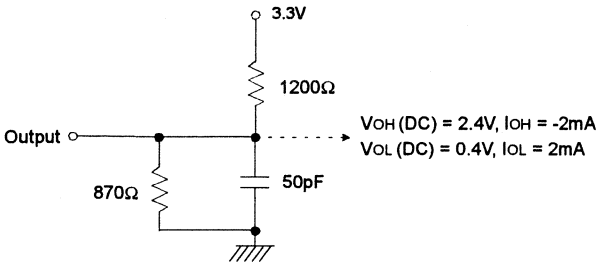
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version		Unit	Note
				-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1,370	1,370	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		20		mA	3
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		20		mA	
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		218		mA	3
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable		110			
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		38		mA	3
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		38			
Active Standby current in non power-down mode	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		362		mA	3
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		182		mA	3
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0mA Page burst 2 Banks activated t_{CCD}=2CLK	3	1,370	1,370	mA	1
			2	1,370	1,280		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		2,450		mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		20		mA	3

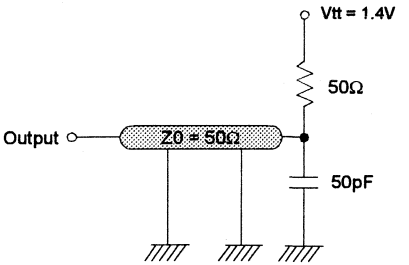
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Measured with 1 PLL & 3 Drive ICs.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to row precharge		tRDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write in Reg. DIMM (1 CLK earlier than Unbuff. DIMM)
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	1,2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	1
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_9$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_9$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

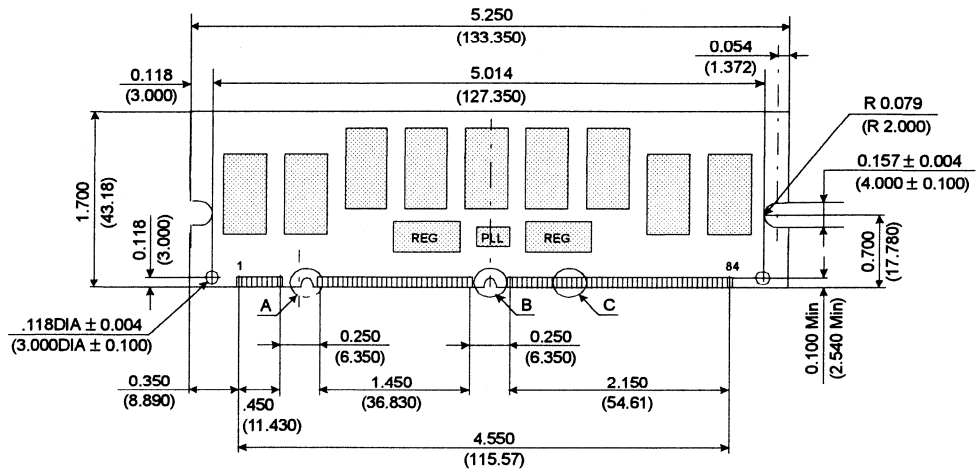
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

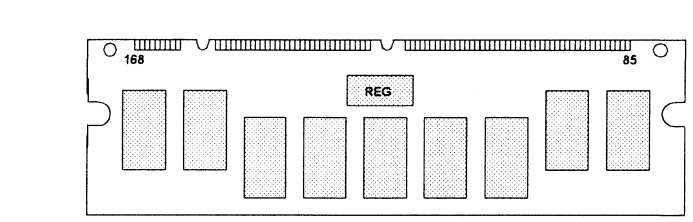
6. Burst stop command is valid at every burst length.

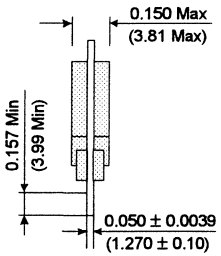
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

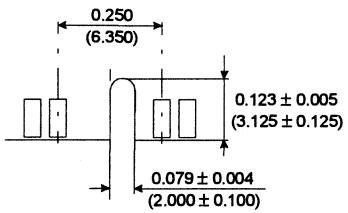
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

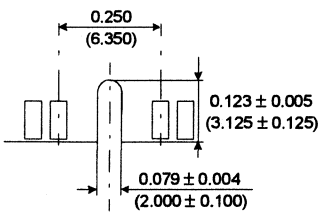




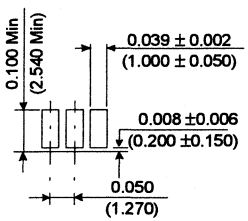




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 16Mx4 SDRAM, TSOP
SDRAM Part No. : K4S640432C

M377S1620CT3-C1H/C1L(1.2ver)

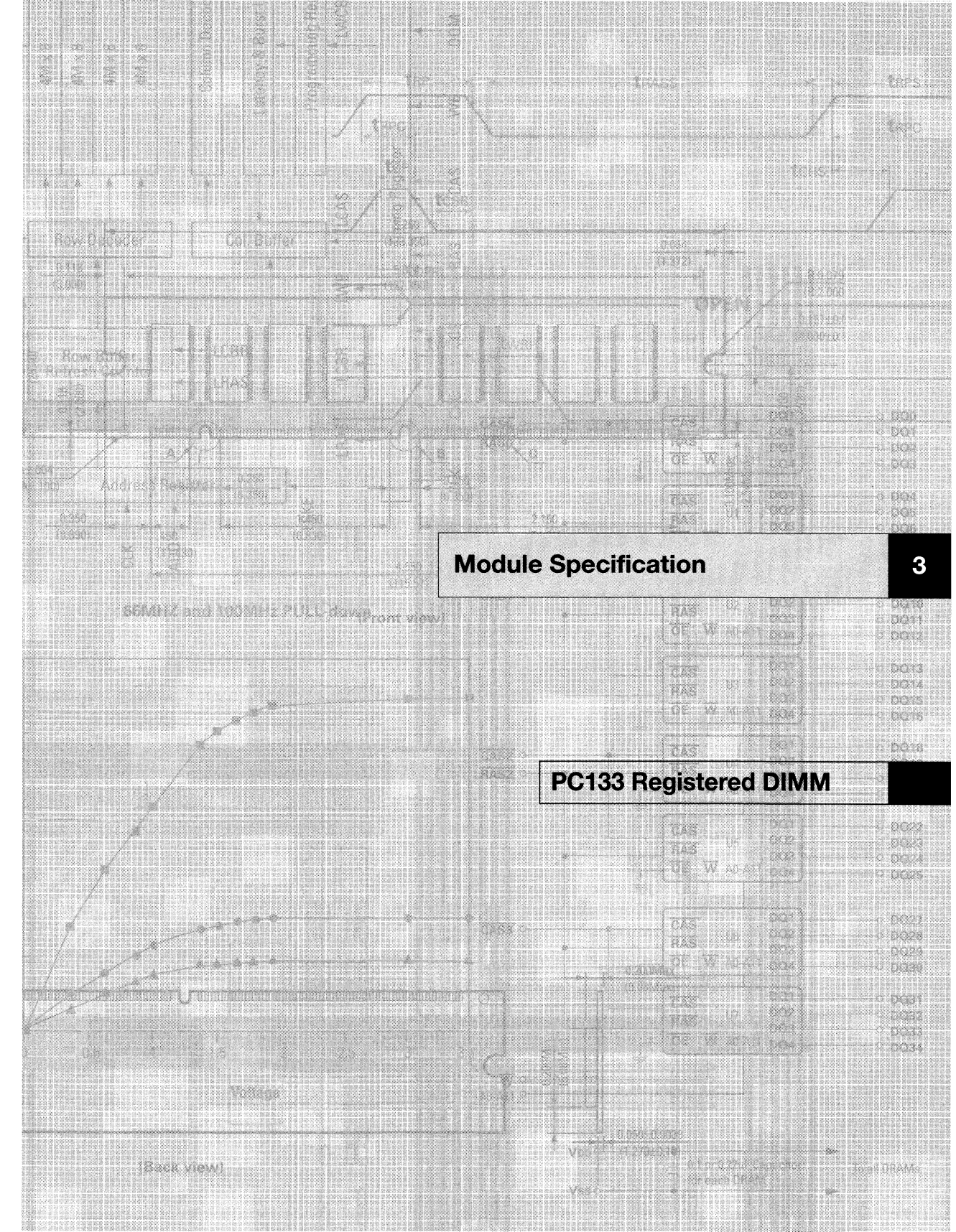
- Organization : 16MX72
- Composition : 16MX4 *18
- Used component part # : K4S640432C-TC1H/C1L
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 4K/64ms
- **Contents** :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	10		0Ah		1
5	# of module Rows on this assembly	1 Row		01h		
6	Data width of this assembly	72 bits		48h		
7	..... Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x4		04h		
14	Error checking SDRAM width	x4		04h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	1 Row of 128MB		20h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		3Fh	6Fh	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	..... Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	..... Manufacturer part # (Data bits)	7		37h		
77	..... Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	1		31h		
80	..... Manufacturer part # (Module depth)	6		36h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	0		30h		
83	Manufacturer part # (Component revision)	C		43h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	3		33h		
86	Manufacturer part # (Hyphen)	"-"		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	3		33h		
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)		43h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.



Module Specification

3

PC133 Registered DIMM

M390S0823DT1 SDRAM DIMM

8Mx72 SDRAM DIMM with PLL & Register based on 8Mx8, 4Banks 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M390S0823DT1 is a 8M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M390S0823DT1 consists of nine CMOS 8Mx8 bit Synchronous DRAMs in TSOP-II 400mil packages, two 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M390S0823DT1 is a Dual In-line Memory Module and is intented for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high band-width, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M390S0823DT1-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,500mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	*CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Colume address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

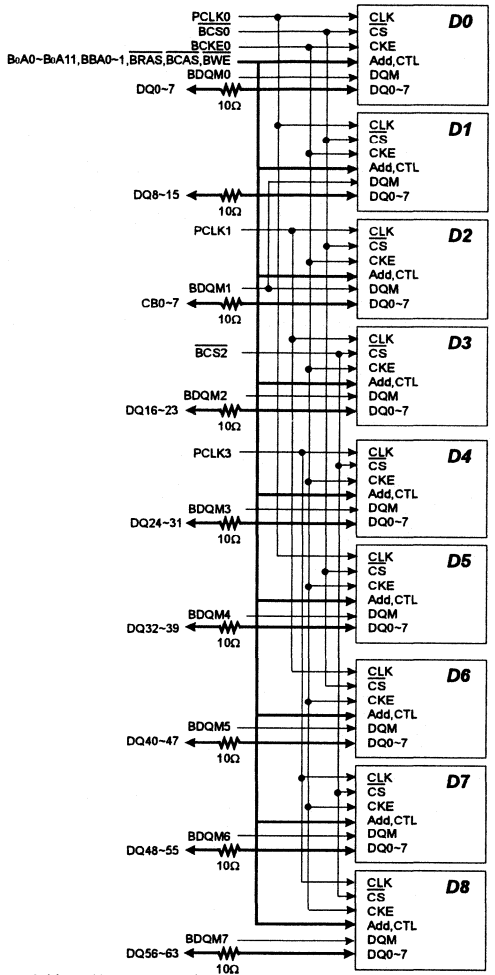
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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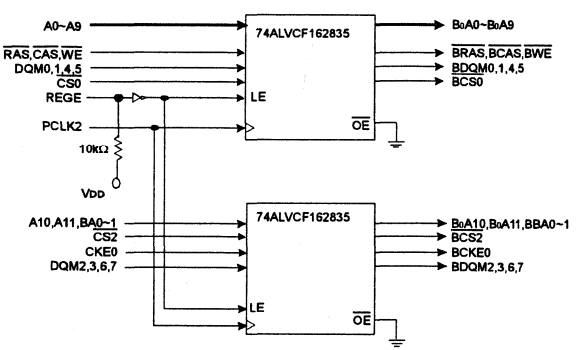
PIN CONFIGURATION DESCRIPTION

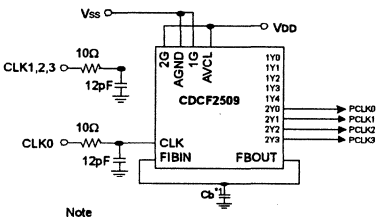
Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	*Register enable*	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to V_{DD} through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
WP	*Write protection*	WP pin is connected to V_{SS} through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM

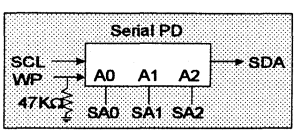


Notes : Address/Control Signals are connected to D2 through 100 ohms resistor.



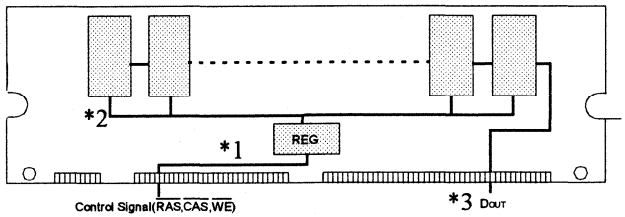


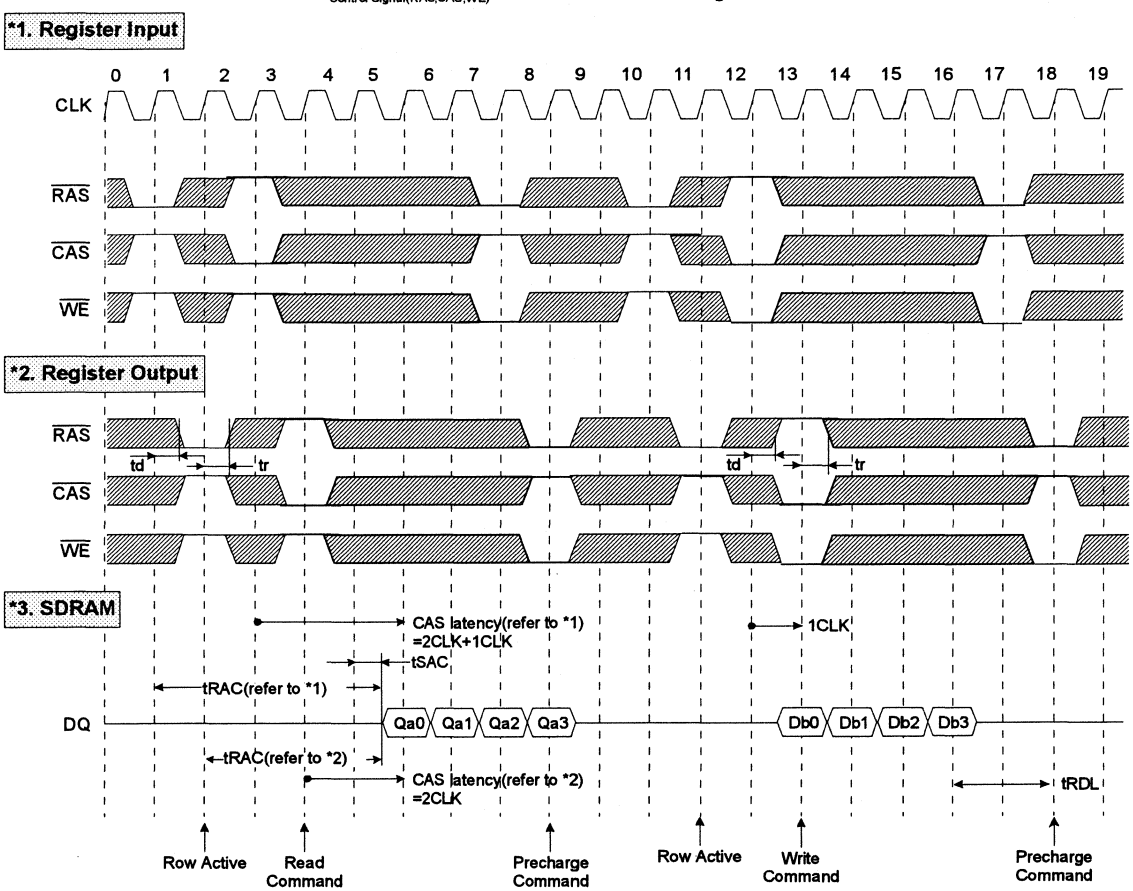
Note
1. The actual values of Cb will depend upon the PLL chosen.



SAMSUNG ELECTRONICS

STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)





td, tr = Delay of register (74ALVCF162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVCF162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

: Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	9	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended Operating Conditions (Voltage Referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11})	C_{IN1}	-	15	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	15	pF
Input capacitance (CKE0)	C_{IN3}	-	15	pF
Input capacitance (CLK0)	C_{IN4}	-	23	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	15	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	15	pF
Input capacitance (BA0 ~ BA1)	C_{IN7}	-	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	16	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT1}	-	16	pF

DC CHARACTERISTICS

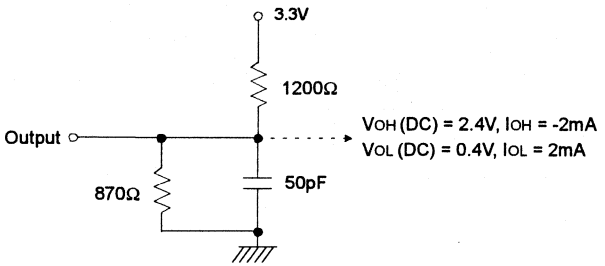
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	1,175	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	359	mA	3
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	11		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	485	mA	3
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	56		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	377	mA	3
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	29		
Active standby current in non power-down mode	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	575	mA	3
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	137	mA	3
Operating current (Burst mode)	I_{CC4}	I_O = 0mA Page burst 4Banks activated t_{CCD}=2CLK	1,535	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	1,715	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	359	mA	3

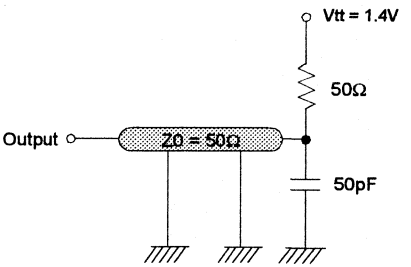
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Measured with 1 PLL & 2 Drive ICs.
4. Unless otherwise noticed, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-75		
Row active to row active delay		tRRD(min)	15	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	ns	1
Row precharge time		tRP(min)	20	ns	1
Row active time		tRAS(min)	45	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	65	ns	1
Last data in to row precharge		tRDL(min)	2	CLK	2
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns	-	-
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	-		-		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-75		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	ns	1
CLK to valid output delay	CAS latency=3	tSAC	-	5.4	ns	1,2
Output data hold time	CAS latency=3	tOH	2.7		ns	1,2
CLK high pulse width		tCH	2.5		ns	3
CLK low pulse width		tCL	2.5		ns	3
Input setup time		tSS	1.5		ns	3
Input hold time		tSH	0.8		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSLZ		5.4	ns	

Notes :

1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

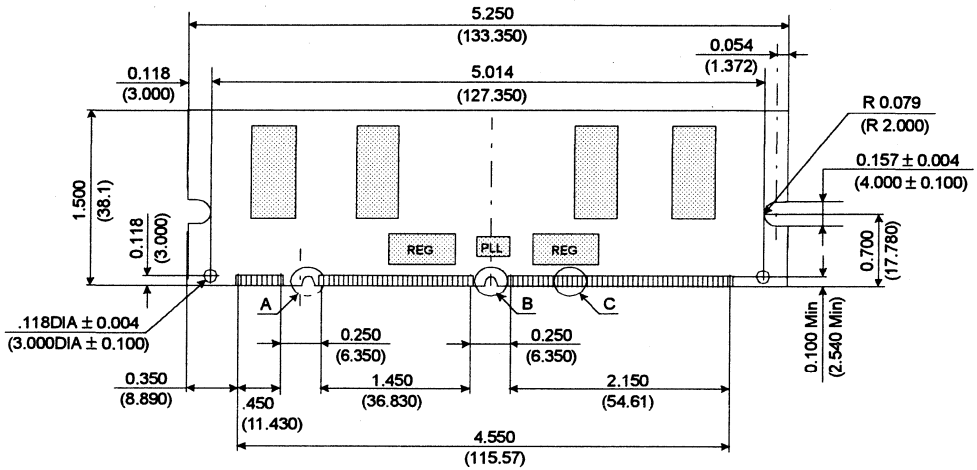
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

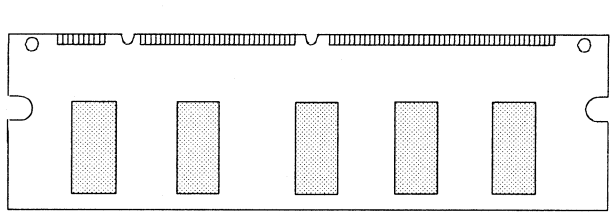
6. Burst stop command is valid at every burst length.

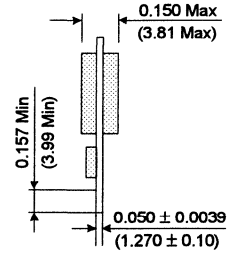
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

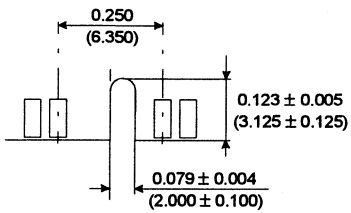
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

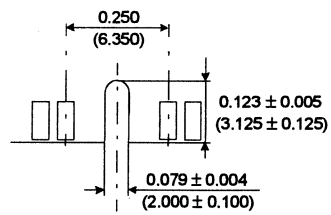




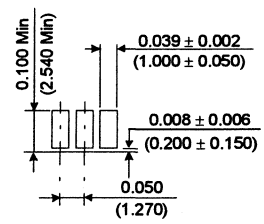




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832D-TC75

This module is based on JEDEC PC133 Specification

M390S0823DT1-C75

- Organization : 8MX72
- Composition : 8MX8 *9
- Used component part # : K4S640832D-TC75
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,500 mil height & double sided component
- Refresh : 4K/64ms
- **Contents** :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	72 bits	48h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	x8	08h	
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL	1Fh	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	
24	SDRAM access time @CAS latency of 2	-	00h	
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 64MB	10h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	BDh	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	9	39h	
77	..... Manufacturer part # (Data bits)	0	30h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	8	38h	
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	D	44h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	1	31h	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	1	31h	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Module Supports this CLK Frequency	100MHz	64h	
127	Attributes for CLK Frequency defined	CLK0, CL-3, ConAP	85h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M390S1620DT1 SDRAM DIMM

16Mx72 SDRAM DIMM with PLL & Register based on 16Mx4, 4Banks 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M390S1620DT1 is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M390S1620DT1 consists of eighteen CMOS 16Mx4 bit Synchronous DRAMs in TSOP-II 400mil packages, three 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M390S1620DT1 is a Dual In-line Memory Module and is intented for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M390S1620DT1-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,700mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	*CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Colume address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

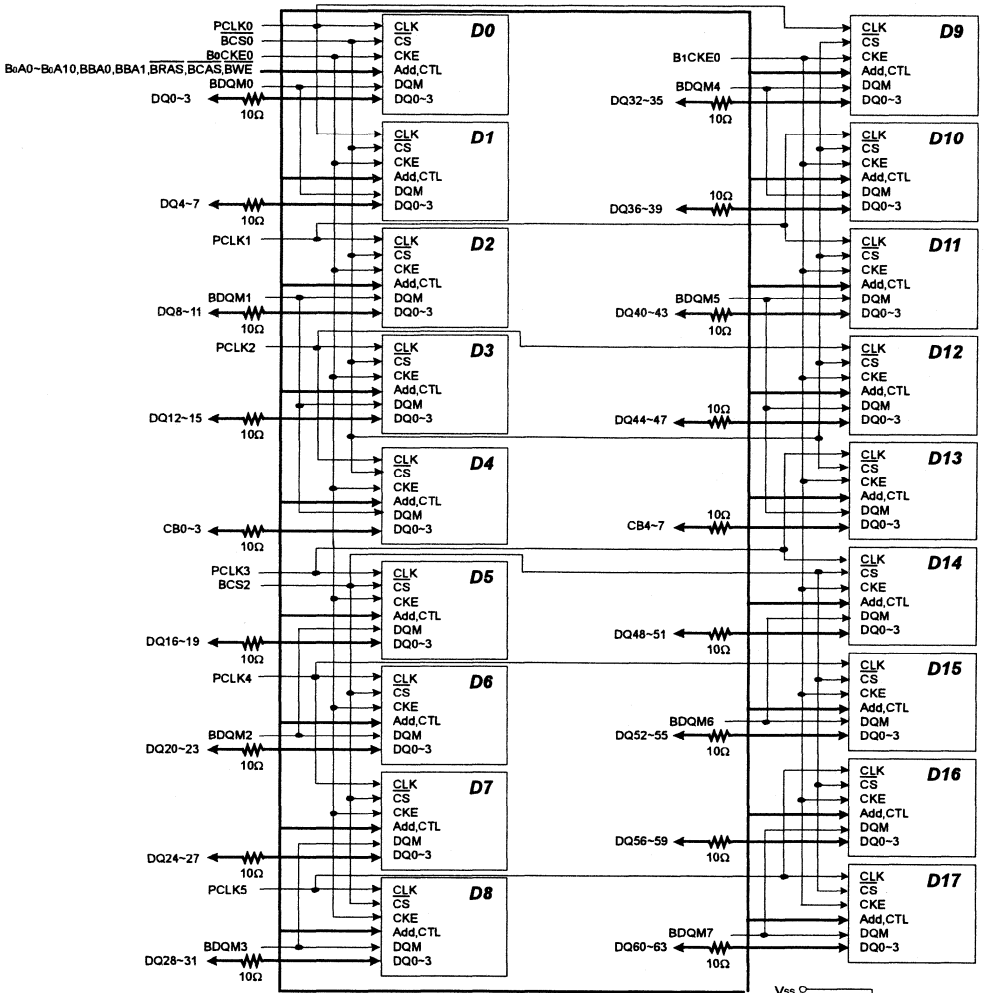
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

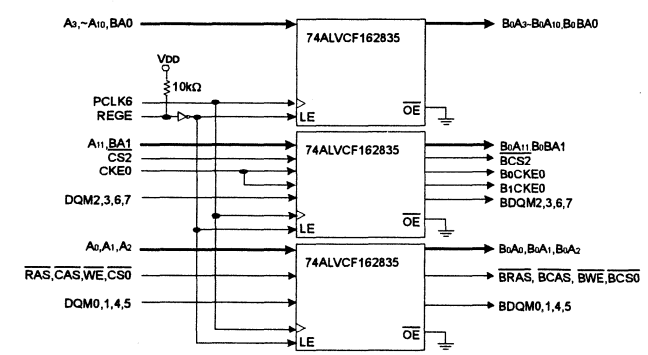
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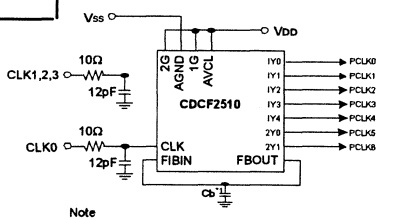
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	*Register enable*	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to V_{DD} through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
WP	*Write protection*	WP pin is connected to V_{SS} through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.

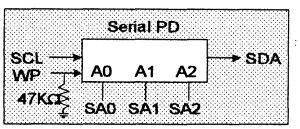
FUNCTIONAL BLOCK DIAGRAM



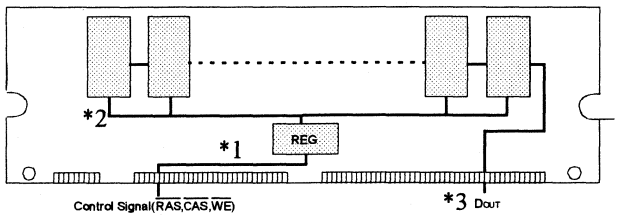


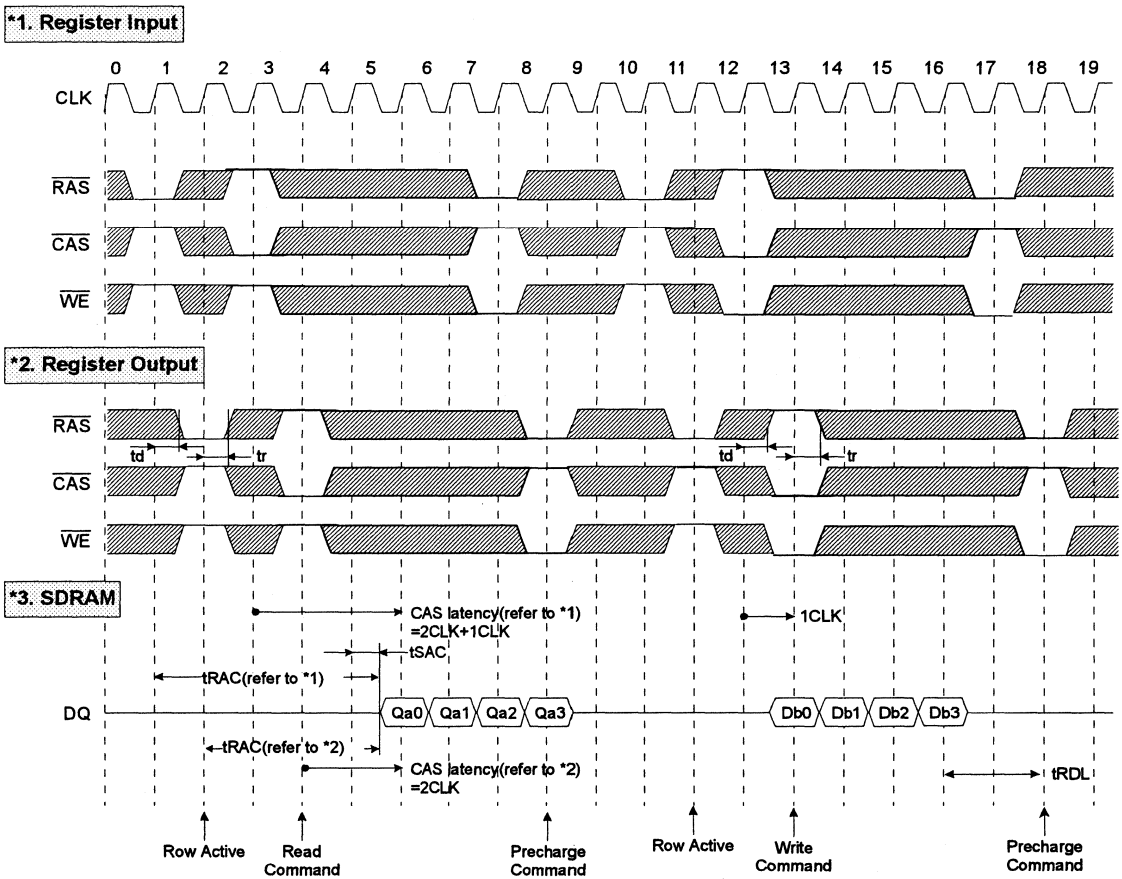


Note
1. The actual values of Cb will depend upon the PLL chosen.



STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)





td, tr = Delay of register (74ALVCF162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVCF162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

: Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	18	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11})	C_{IN1}	-	15	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	15	pF
Input capacitance (CKE0)	C_{IN3}	-	15	pF
Input capacitance (CLK0)	C_{IN4}	-	20	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	15	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	15	pF
Input capacitance (BA0 ~ BA1)	C_{IN7}	-	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	16	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT1}	-	16	pF

DC CHARACTERISTICS

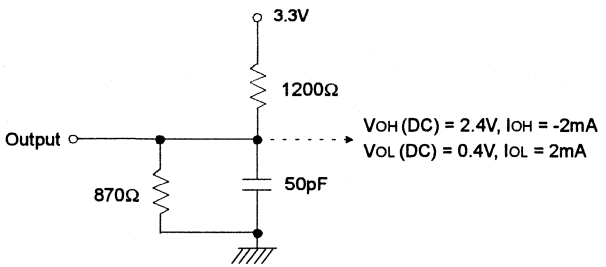
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	1,760	mA	1,3
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	368	mA	3
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	20		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	620	mA	3
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable	110		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	404	mA	3
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	56		
Active Standby current in non power-down mode	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	800	mA	3
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	272	mA	3
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0mA Page burst 4 Banks activated t_{CCD}=2CLK	2,570	mA	1,3
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	2,930	mA	2,3
Self refresh current	I_{CC6}	CKE ≤ 0.2V	368	mA	3

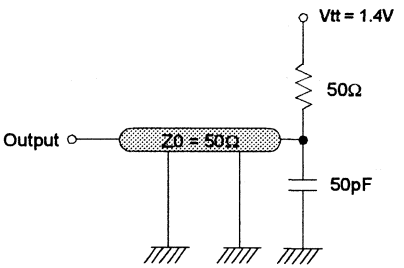
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Measured with 1 PLL & 3 Drive ICs.
4. Unless otherwise noticed, Input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ})

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-75		
Row active to row active delay		tRRD(min)	15	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	ns	1
Row precharge time		tRP(min)	20	ns	1
Row active time		tRAS(min)	45	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	65	ns	1
Last data in to row precharge		tRDL(min)	2	CLK	2
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns	-	-
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	-		-		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-75		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	ns	1
CLK to valid output delay	CAS latency=3	tSAC	-	5.4	ns	1,2
Output data hold time	CAS latency=3	tOH	2.7	-	ns	1,2
CLK high pulse width		tCH	2.5		ns	3
CLK low pulse width		tCL	2.5		ns	3
Input setup time		tSS	1.5		ns	3
Input hold time		tSH	0.8		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4	ns	1

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

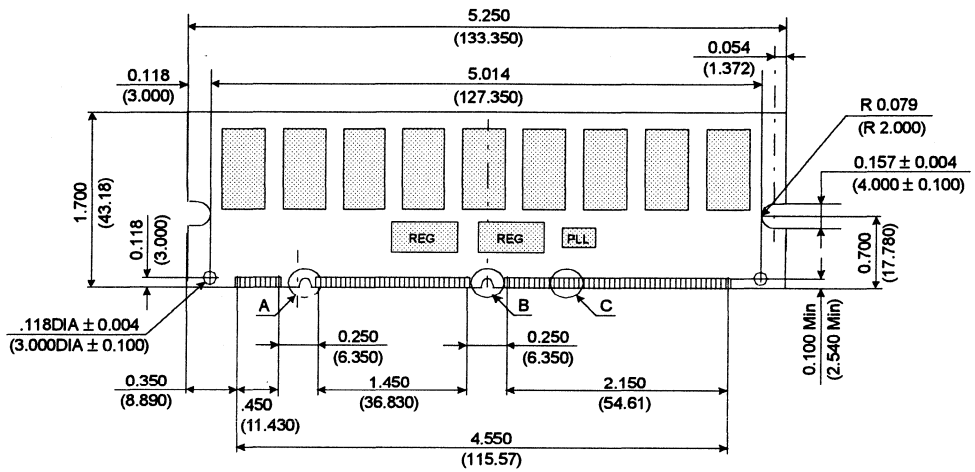
Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

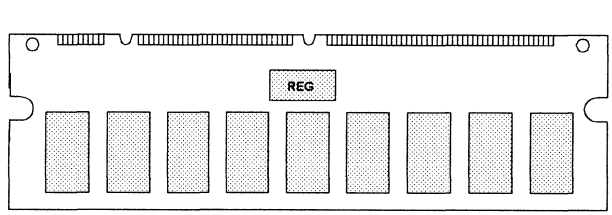
(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

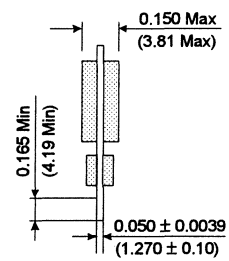
Notes : 1. OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

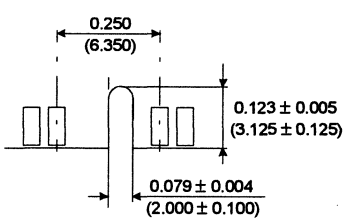
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

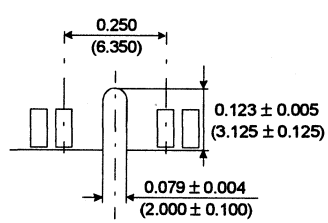




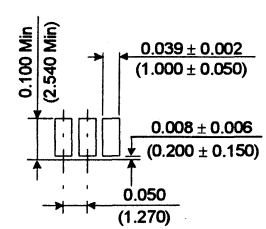




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 16Mx4 SDRAM, TSOP
SDRAM Part No. : K4S640432D-TC75

This module is based on JEDEC PC133 Specification

M390S1620DT1-C75

- Organization : 16MX72
- Composition : 16MX4 *18
- Used component part # : K4S640432D-TC75
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 4K/64ms
- **Contents** :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	72 bits	48h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x4	04h	
14	Error checking SDRAM width	x4	04h	
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL	1Fh	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	
24	SDRAM access time @CAS latency of 2	-	00h	
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 128MB	20h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	C6h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	9	39h	
77	..... Manufacturer part # (Data bits)	0	30h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	..... Manufacturer part # (Module depth)	6	36h	
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2	32h	
82	Manufacturer part # (Composition component)	0	30h	
83	Manufacturer part # (Component revision)	D	44h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	1	31h	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	1	31h	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Module Supports this CLK Frequency	100MHz	64h	
127	Attributes for CLK Frequency defined	CLK0, CL-3, ConAP	85h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

Module Specification

3

PC100 Unbuffered DIMM

M366S0424DTS SDRAM DIMM

4Mx64 SDRAM DIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S0424DTS is a 4M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S0424DTS consists of four CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S0424DTS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S0424DTS-C80	125MHz (8ns @ CL=3)
M366S0424DTS-C1H	100MHz (10ns @ CL=2)
M366S0424DTS-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,000mil)** , Single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	NC	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	NC	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0, CLK2	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

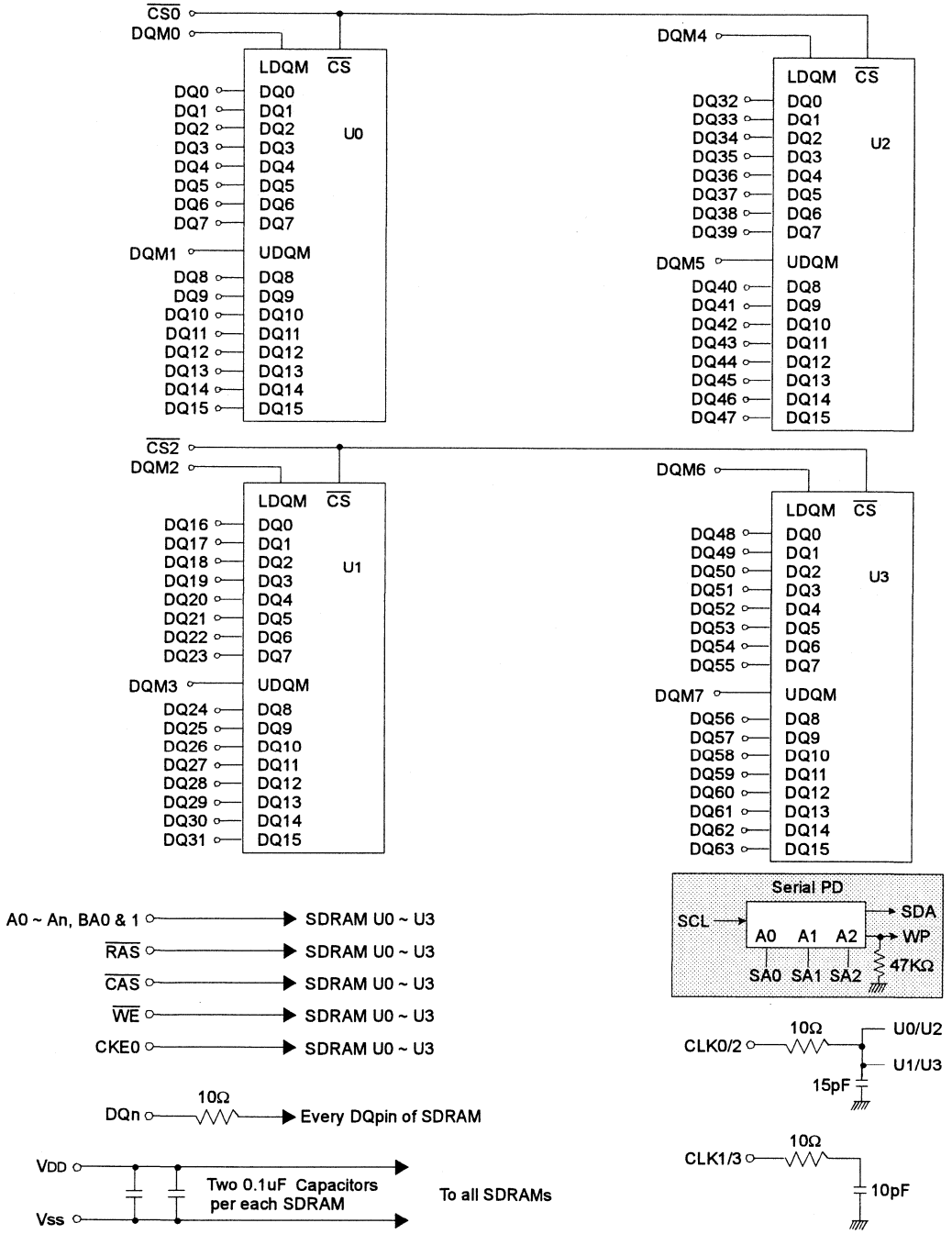
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA7
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
WP	*Write protection*	WP pin is connected to VSS through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	4	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C_{ADD}	15	25	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN}	15	25	pF
CKE (CKE0)	C_{CKE}	15	25	pF
Clock (CLK0, CLK2)	C_{CLK}	10	13	pF
$\overline{CS}$ ($\overline{CS0}$, $\overline{CS2}$)	C_{CS}	10	15	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	8	10	pF
DQ (DQ0 ~ DQ63)	C_{OUT}	9	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-80	-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	440	400	400	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	4			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	4				
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	60			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	24				
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	12			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	12				
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	100			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	60			mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs	520	440	440	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	520	500	500	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	4			mA	

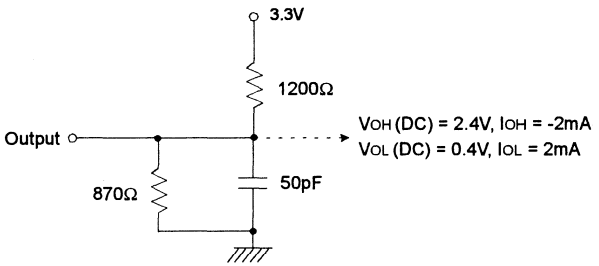
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

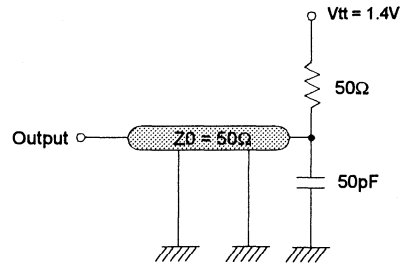
3. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	2			CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns			-	5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		-	1			

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -80/1H/1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		10		12			
CLK to valid output delay	CAS latency=3	t_{SAC}		6		6		6	ns	1, 2
	CAS latency=2			-		6		7		
Output data hold time	CAS latency=3	t_{OH}	3		3		3		ns	2
	CAS latency=2		-		3		3			
CLK high pulse width		t_{CH}	3		3		3		ns	3
CLK low pulse width		t_{CL}	3		3		3		ns	3
Input setup time		t_{SS}	2		2		2		ns	3
Input hold time		t_{SH}	1		1		1		ns	3
CLK to output in Low-Z		t_{SLZ}	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		6		6		6	ns	
	CAS latency=2			-		6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
		Entry		L									3
	Self refresh	Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A7)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A7)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

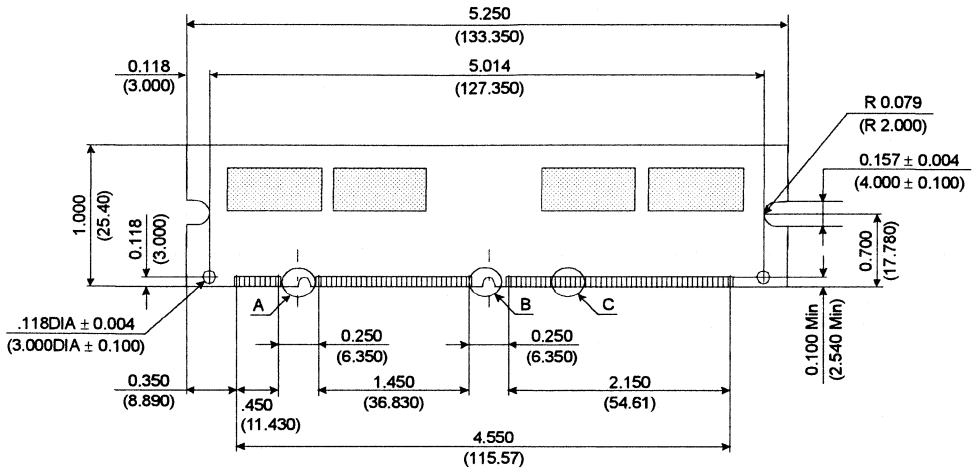
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

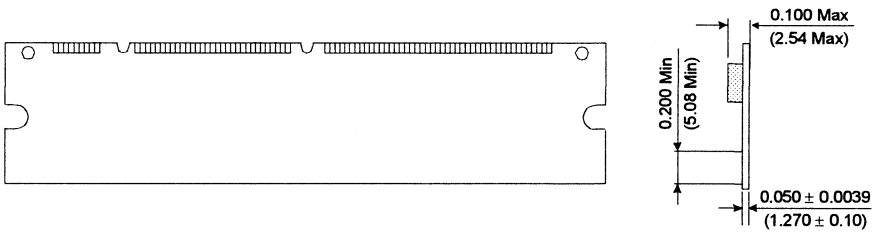
6. Burst stop command is valid at every burst length.

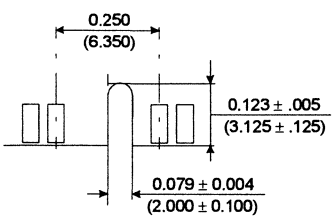
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

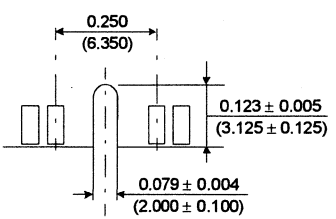
Units : Inches (Millimeters)



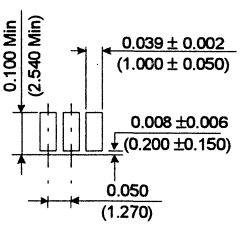




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : K4S641632D

M366S0424DTS-C80/C1H/C1L

- Organization : 4Mx64
- Composition : 4Mx16 *4
- Used component part # : K4S641632D-TC80/C1H/C1L
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,000mil height & single sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	8			08h			1
5	# of module rows on this assembly	1 row			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module row density	1 row of 32MB			08h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8O	-1H	-1L	-8O	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec.Ver.1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			DEh	04h	34h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	..... Manufacturer part # (Data bits)	6			36h			
77	..... Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	0			30h			
80	..... Manufacturer part # (Module depth)	4			34h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	4			34h			
83	Manufacturer part # (Component revision)	D			44h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	S			53h			
86	Manufacturer part # (Hyphen)	"-"			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	S			53h			
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)			44h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M366S0823DTS SDRAM DIMM

8Mx64 SDRAM DIMM based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S0823DTS is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S0823DTS consists of eight CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. One 0.1uF and one 0.33 uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S0823DTS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S0823DTS-C80	125MHz (8ns @ CL=3)
M366S0823DTS-C1H	100MHz (10ns @ CL=2)
M366S0823DTS-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)** , single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0, CLK2	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

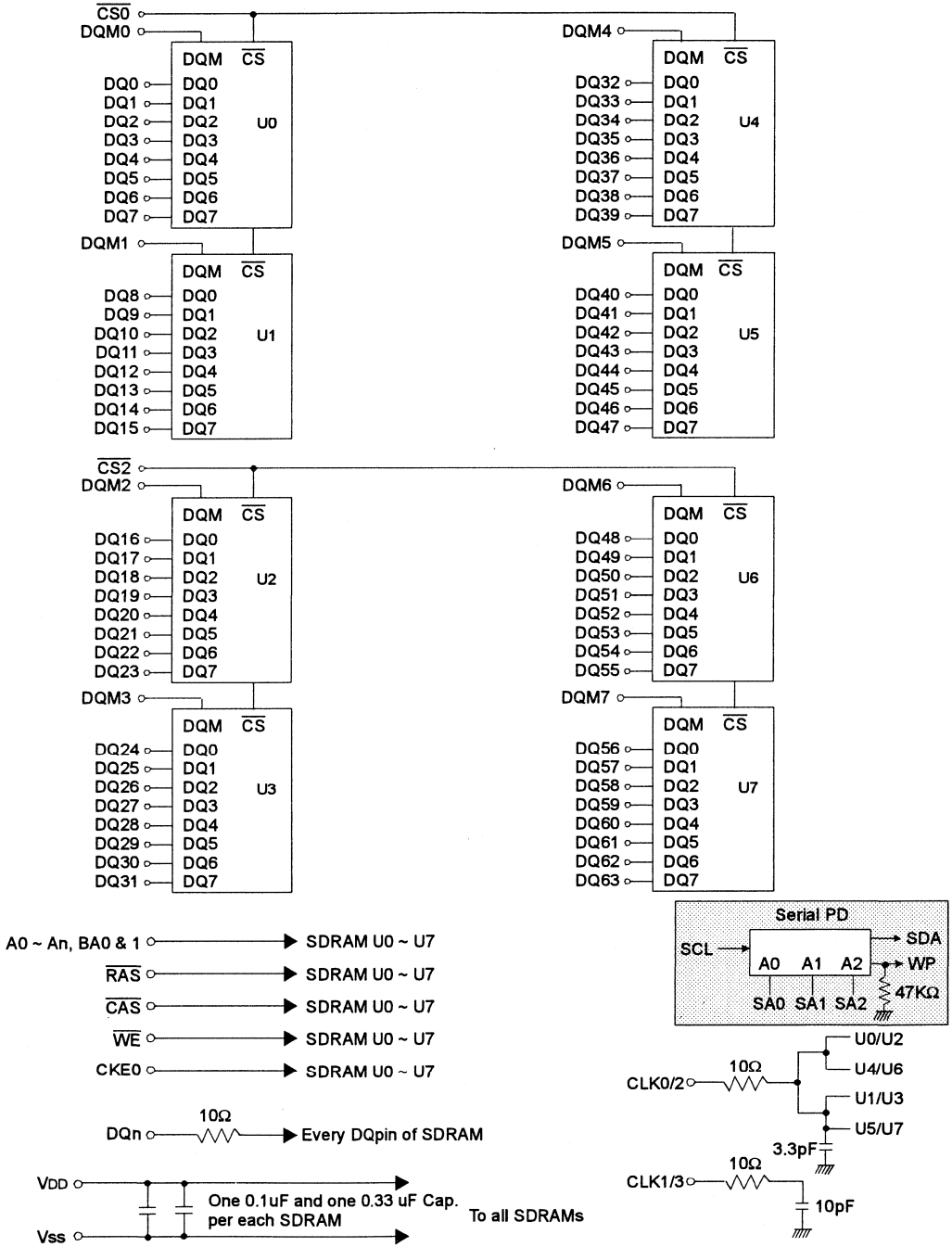
** These pins should be NC in the system which does not support SPD.

SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
WP	*Write protection*	WP pin is connected to Vss through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write - protected.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high votlage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C_{ADD}	25	45	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN}	25	45	pF
CKE (CKE0)	C_{CKE}	25	45	pF
Clock (CLK0, CLK2)	C_{CLK}	15	21	pF
$\overline{CS}$ ($\overline{CS0}$, $\overline{CS2}$)	C_{CS}	15	25	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	8	12	pF
DQ (DQ0 ~ DQ63)	C_{OUT}	9	12	pF

DC CHARACTERISTICS

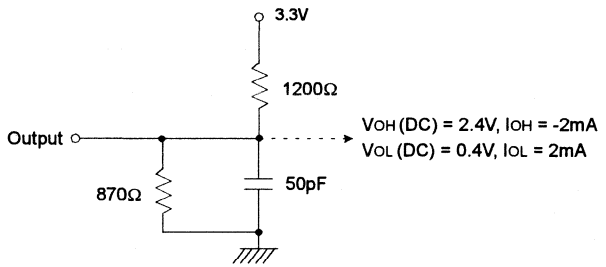
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-80	-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length =1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	600	560	560	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	8			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	8				
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	120			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	48				
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	24			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	24				
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	200			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	120			mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs	880	760	760	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	1,040	1,000	1,000	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	8			mA	

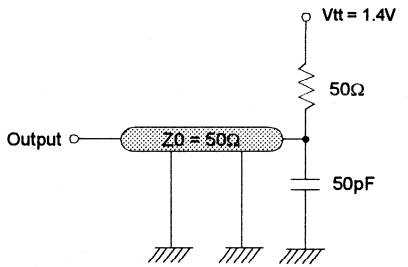
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	2			CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns			-	5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		-	1			

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -80/1H/1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported . SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6	ns	1,2
	CAS latency=2			-		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		-		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			-		6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

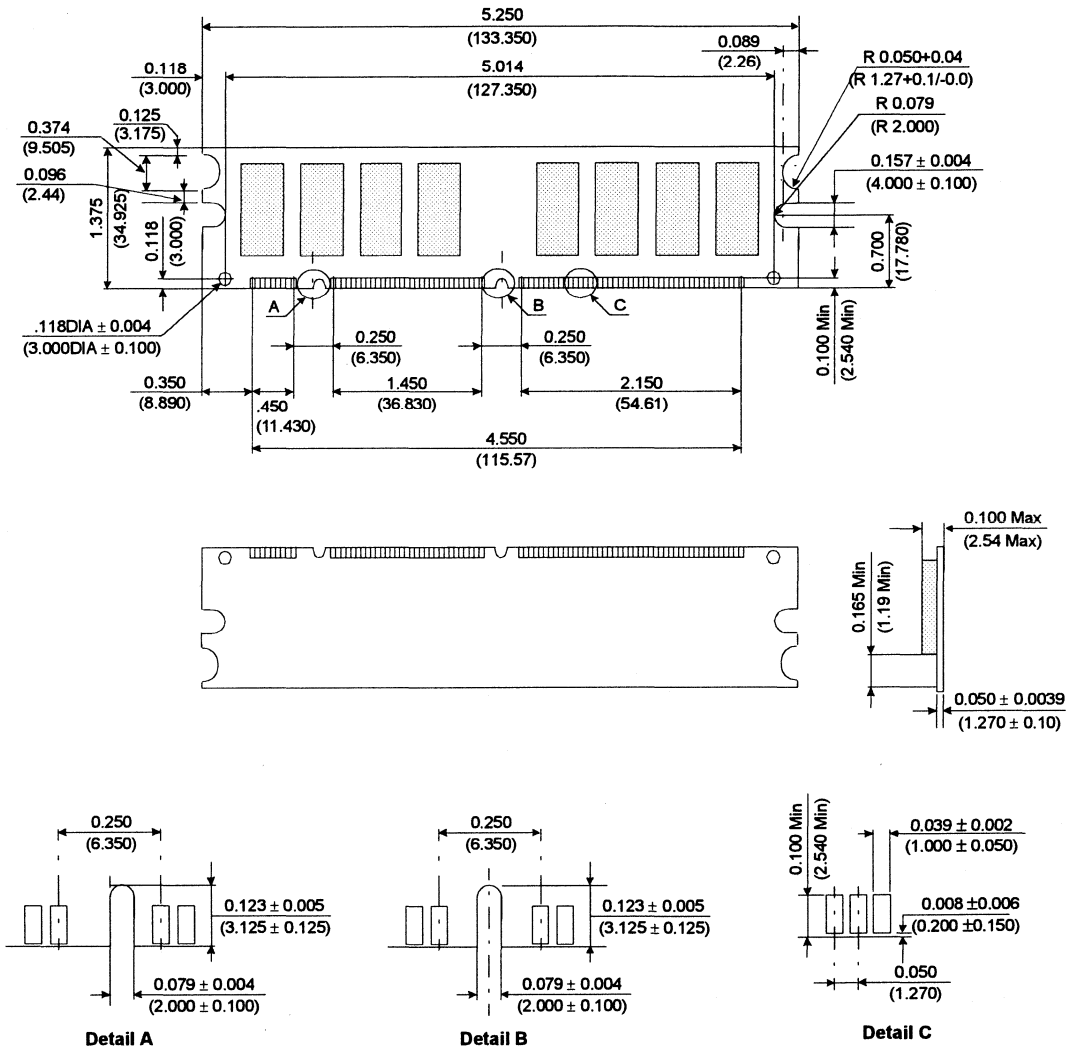
Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832D

M366S0823DTS-C80/C1H/C1L

- Organization : 8Mx64
- Composition : 8Mx8 *8
- Used component part # : K4S640832D-TC80/C1H/C1L
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module rows on this assembly	1 row			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module row density	1 row of 64MB			10h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8B	-1H	-1L	-8B	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			DFh	05h	35h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	..... Manufacturer part # (Data bits)	6			36h			
77	..... Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	0			30h			
80	..... Manufacturer part # (Module depth)	8			38h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	D			44h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	S			53h			
86	Manufacturer part # (Hyphen)	"-"			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	S			53h			
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)			44h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M366S0824DT0 SDRAM DIMM

8Mx64 SDRAM DIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S0824DT0 is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S0824DT0 consists of eight CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S0824DT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S0824DT0-C80	125MHz (8ns @ CL=3)
M366S0824DT0-C1H	100MHz (10ns @ CL=2)
M366S0824DT0-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	NC	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	NC	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

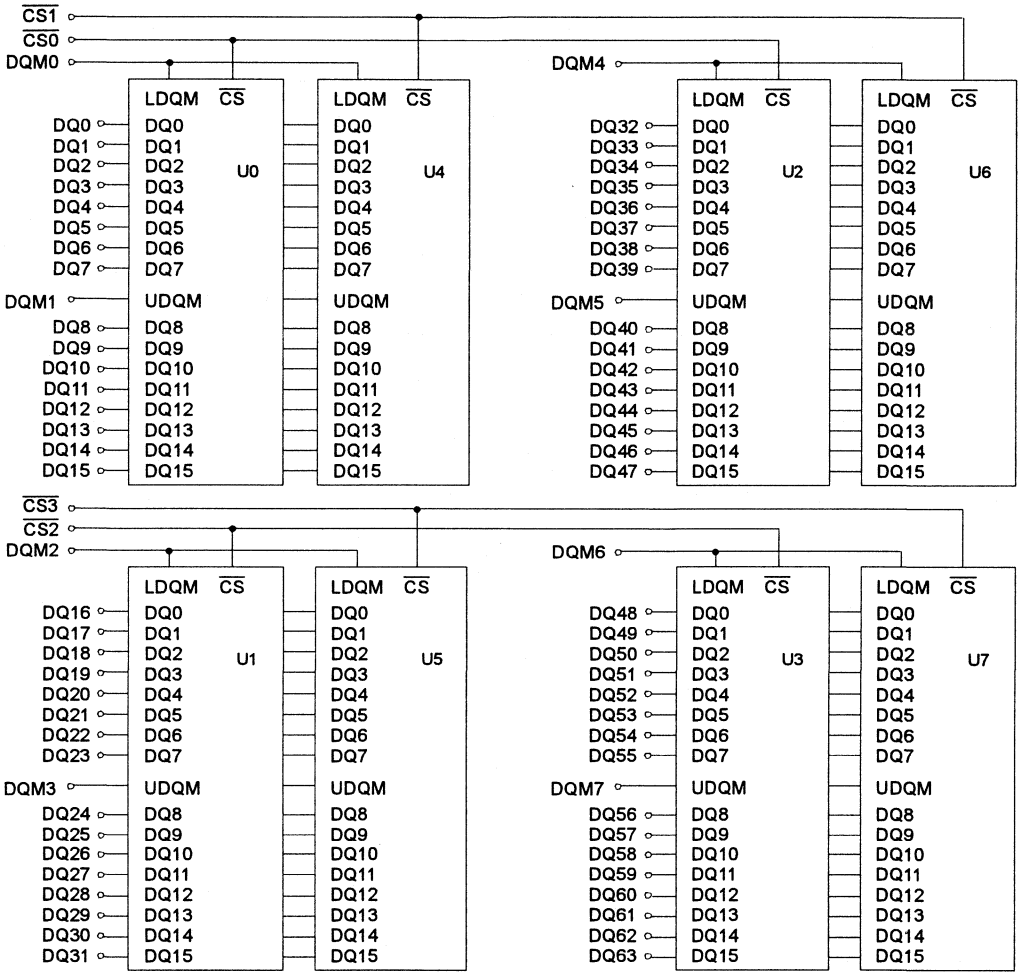
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

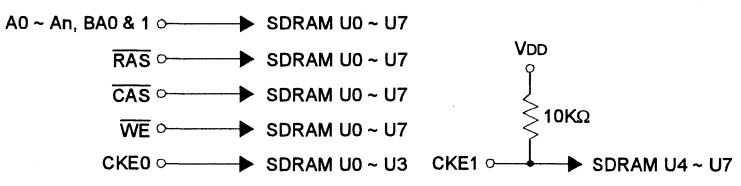
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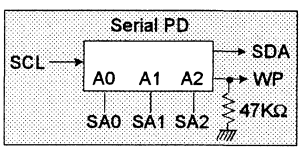
PIN CONFIGURATION DESCRIPTION

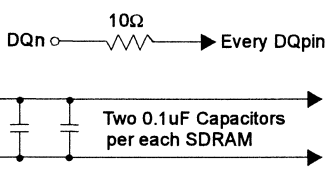
Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, column address : CA0 ~ CA7
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
WP	*Write protection*	WP pin is connected to VSS through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

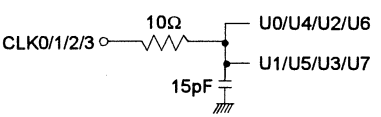
FUNCTIONAL BLOCK DIAGRAM











ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Note : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C_{ADD}	25	45	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN}	25	45	pF
CKE (CKE0)	C_{CKE}	15	25	pF
Clock (CLK0, CLK2)	C_{CLK}	10	13	pF
$\overline{CS}$ ($\overline{CS0}$, $\overline{CS2}$)	C_{CS}	10.	15	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	8	10	pF
DQ (DQ0 ~ DQ63)	C_{OUT}	9	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-80	-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length =1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	540	500	500	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	8			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	8				
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns.	120			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	48				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	24			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	24				
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	200			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	120			mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs	620	540	540	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	620	600	600	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	8			mA	

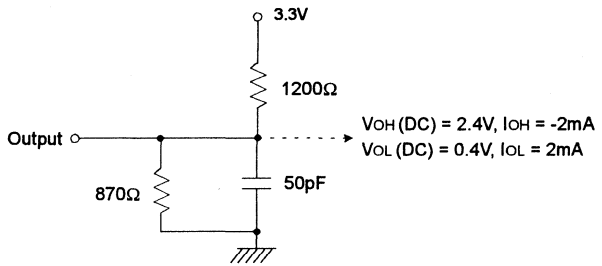
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

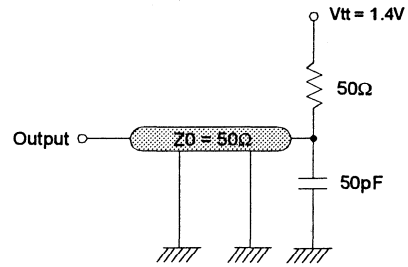
3. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	2			CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns			-	5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		-	1			

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -80/1H/1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported . SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6	ns	1,2
	CAS latency=2			-		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		-		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			-		6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

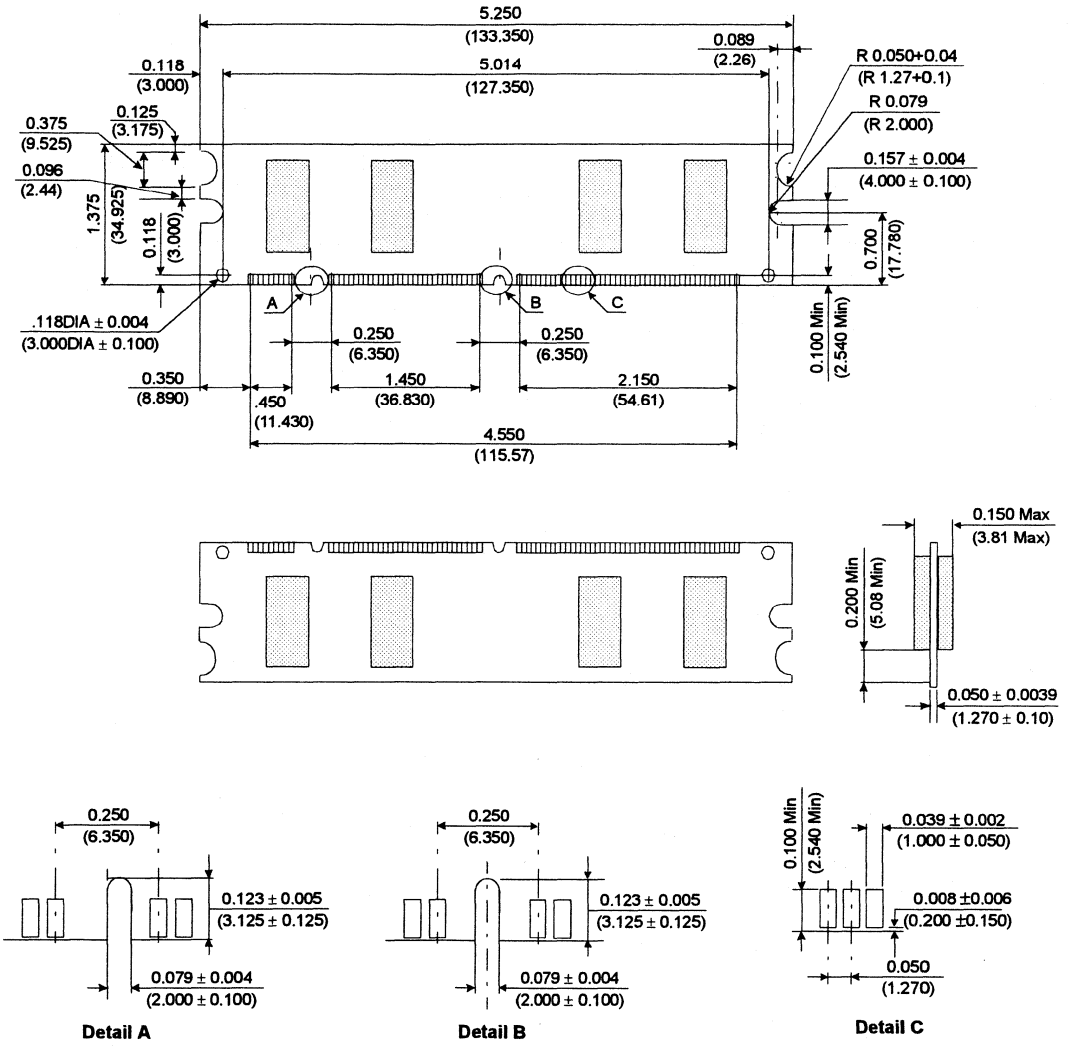
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : K4S641632D

M366S0824DT0-C80/C1H/C1L

- Organization : 8Mx64
- Composition : 4Mx16 *8
- Used component part # : K4S641632D-TC80/C1H/C1L
- # of rows in module : 2 rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	8			08h			1
5	# of module rows on this assembly	2 rows			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module row density	2 rows of 32MB			08h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8G	-1H	-1L	-8G	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			DFh	05h	35h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	..... Manufacturer part # (Data bits)	6			36h			
77	..... Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	0			30h			
80	..... Manufacturer part # (Module depth)	8			38h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	4			34h			
83	Manufacturer part # (Component revision)	D			44h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	0			30h			
86	Manufacturer part # (Hyphen)	"-"			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	0			30h			
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)			44h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			FDh	FFh	FDh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M366S1623DT0 SDRAM DIMM

16Mx64 SDRAM DIMM based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S1623DT0 is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S1623DT0 consists of sixteen CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S1623DT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S1623DT0-C80	125MHz (8ns @ CL=3)
M366S1623DT0-C1H	100MHz (10ns @ CL=2)
M366S1623DT0-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

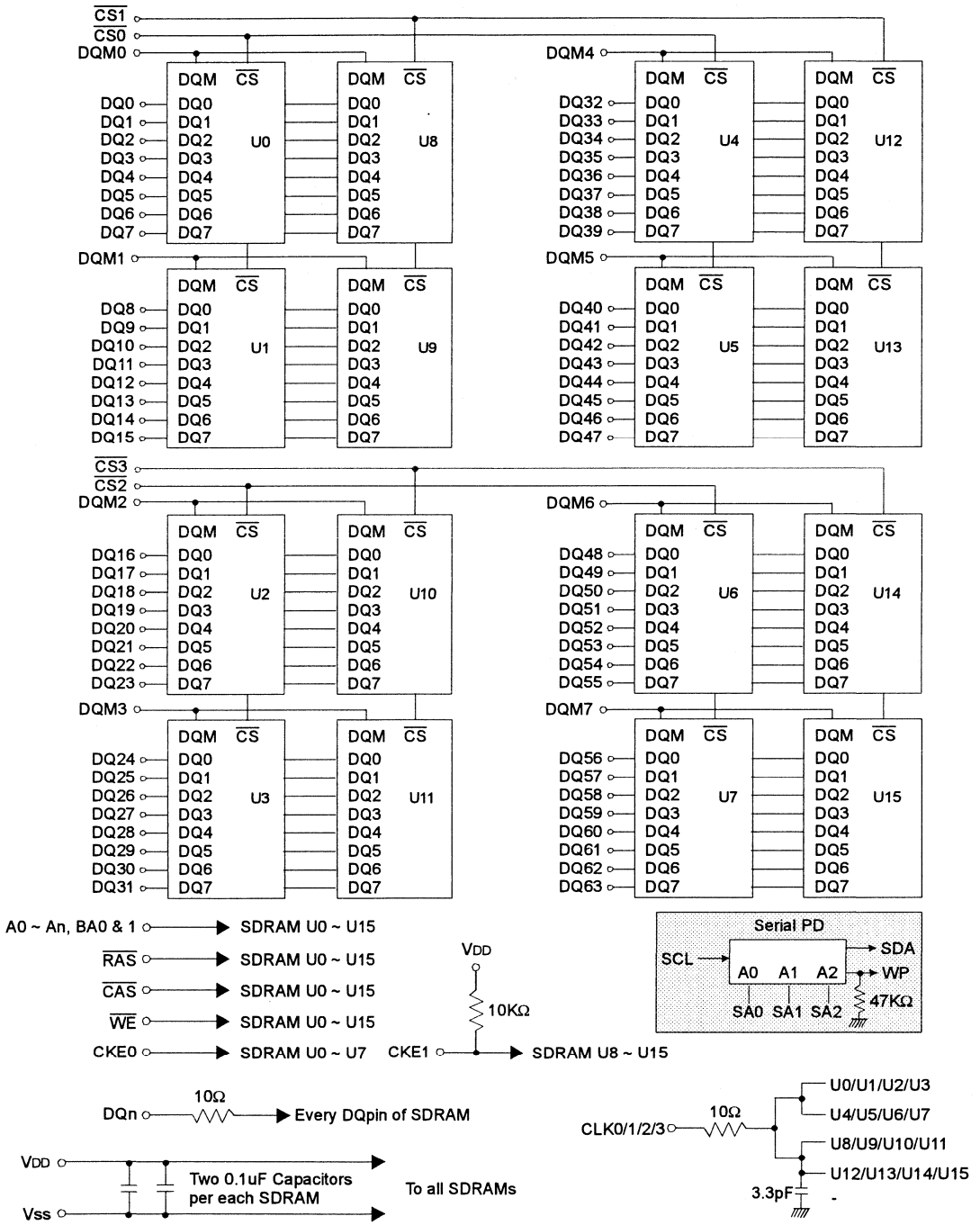
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
WP	*Write protection*	WP pin is connected to VSS through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	16	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Note : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C_{ADD}	45	85	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN}	45	85	pF
CKE (CKE0 ~ CKE1)	C_{CKE}	25	45	pF
Clock (CLK0 ~ CLK3)	C_{CLK}	15	21	pF
$\overline{CS}$ ($\overline{CS0}$~$\overline{CS3}$)	C_{CS}	15	25	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	10	15	pF
DQ (DQ0 ~ DQ63)	C_{OUT}	13	18	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-80	-1H	-1L		
Operating current (one Bank Active)	I_{CC1}	Burst length =1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	800	760	760	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	16			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	16				
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	240			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	96				
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	48			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	48				
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	400			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	240			mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs	1,080	960	960	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	1,240	1,200	1,200	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	16			mA	

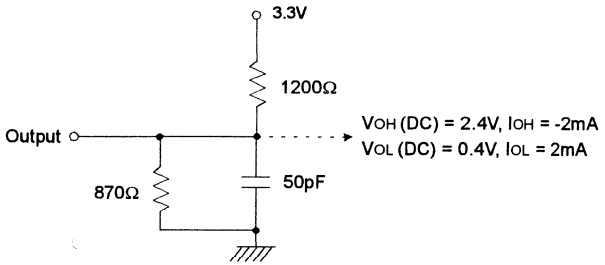
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

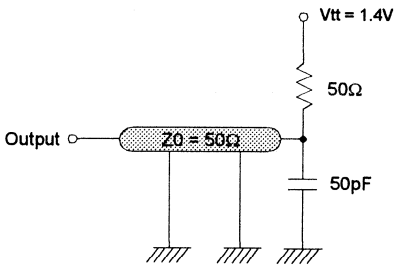
3. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	2			CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns			-	5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		-	1			

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -80/1H/1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported . SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6	ns	1,2
	CAS latency=2			-		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		-		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			-		6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

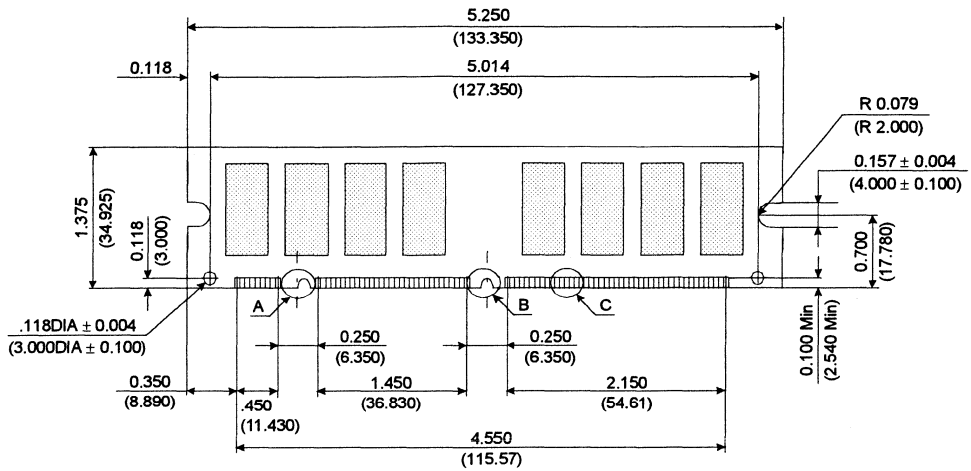
Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

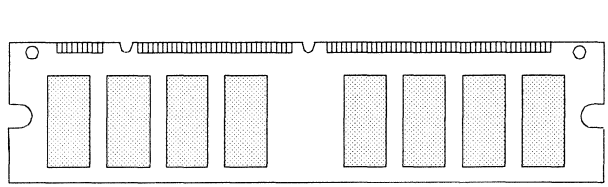
(V=Valid, X=Don't care, H=Logic high, L=Logic low)

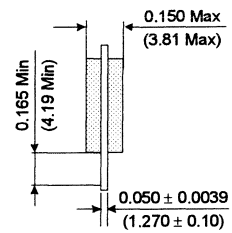
Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

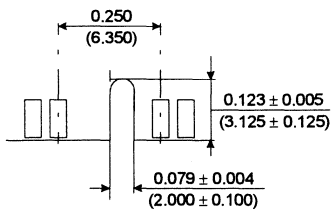
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

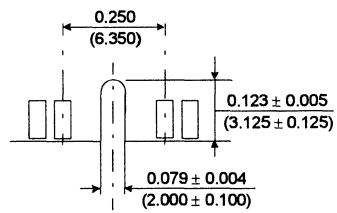




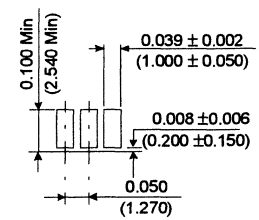




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832D

M366S1623DT0- C80/C1H/C1L

- Organization : 16Mx64
- Composition : 8Mx8 *16
- Used component part # : K4S640832D-TC80/C1H/C1L
- # of rows in module : 2 rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-11L	-80	-H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module rows on this assembly	2 rows			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time from clock@CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock@CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module row density	2 rows of 64MB			10h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			E0h	06h	36h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	..... Manufacturer part # (Data bits)	6			36h			
77	..... Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	1			31h			
80	..... Manufacturer part # (Module depth)	6			36h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	D			44h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	0			30h			
86	Manufacturer part # (Hyphen)	"-"			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	0			30h			
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)			44h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			FDh	FFh	FDh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M374S0823DTS SDRAM DIMM

8Mx72 SDRAM DIMM with ECC based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S0823DTS is a 8M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S0823DTS consists of nine CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. One 0.1uF and one 0.33 uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M374S0823DTS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S0823DTS-C80	125MHz (8ns @ CL=3)
M374S0823DTS-C1H	100MHz (10ns @ CL=2)
M374S0823DTS-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)** , single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0, CLK2	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

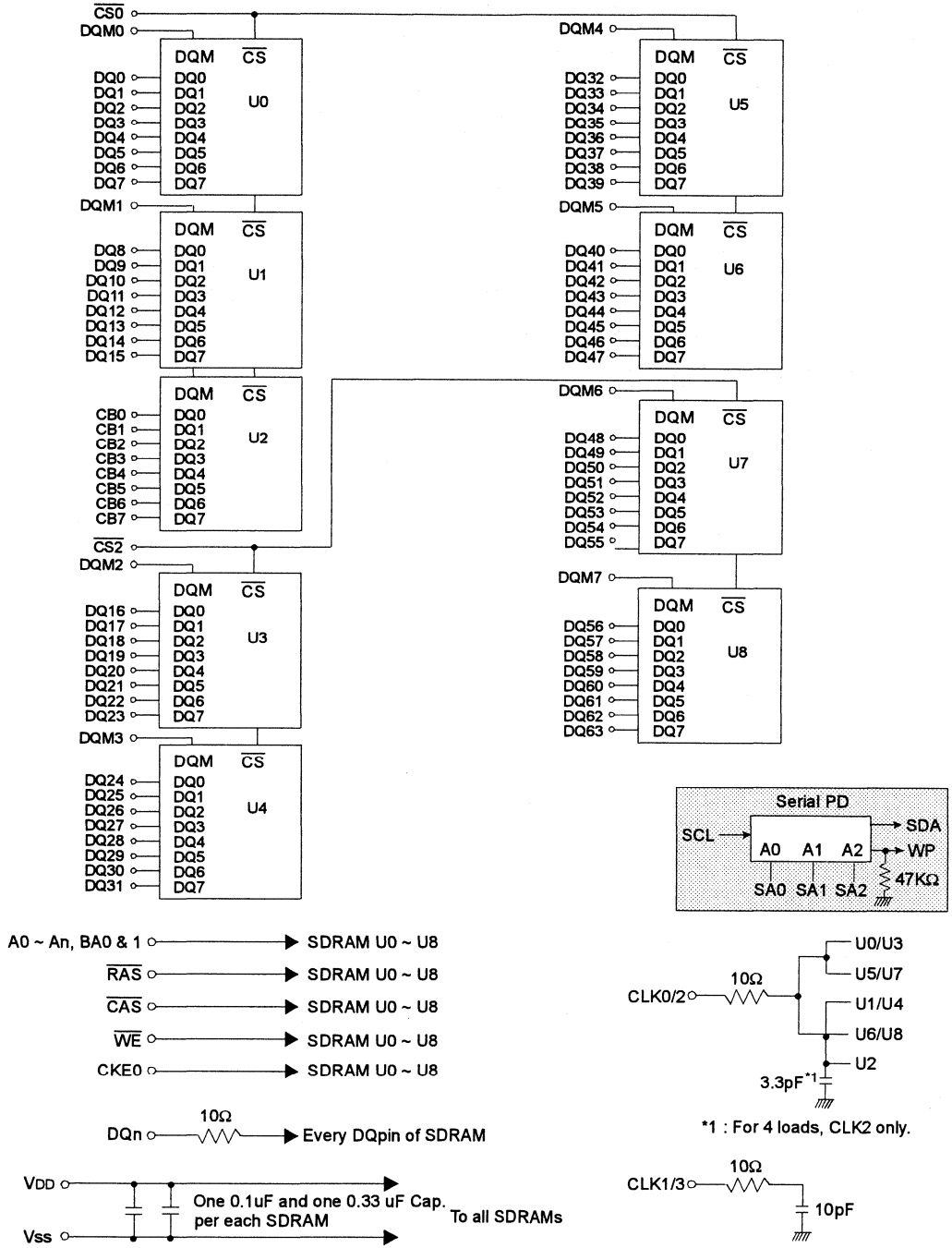
SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

SAMSUNG ELECTRONICS

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
WP	*Write protection*	WP pin is connected to Vss through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write - protected.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	9	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Note : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C_{ADD}	28	50	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN}	28	50	pF
CKE (CKE0)	C_{CKE}	28	50	pF
Clock (CLK0, CLK2)	C_{CLK}	18	25	pF
$\overline{CS}$ ($\overline{CS0}$, $\overline{CS2}$)	C_{CS}	18	30	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	8	10	pF
DQ (DQ0 ~ DQ63)	C_{OUT1}	9	12	pF
CB (CB0 ~ CB7)	C_{OUT2}	9	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-80	-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	675	630	630	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	9			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	9				
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	135			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	54				
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	27			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	27				
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	225			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	135			mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs	990	855	855	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	1,170	1,125	1,125	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	9			mA	

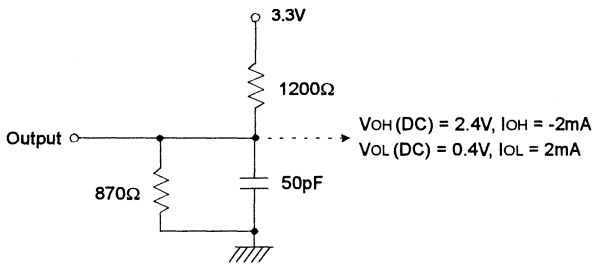
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

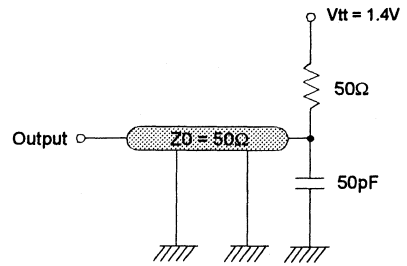
3. Unless otherwise noted, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ})

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	2			CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns			-	5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		-	1			

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -80/1H/1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported . SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6	ns	1,2
	CAS latency=2			-		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		-		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			-		6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

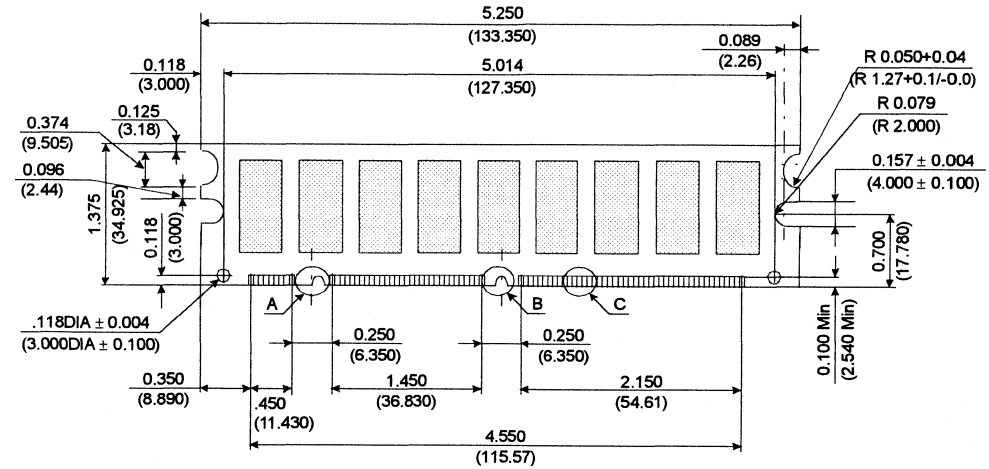
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

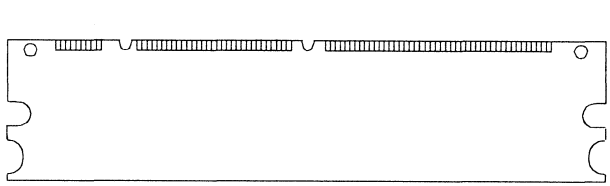
6. Burst stop command is valid at every burst length.

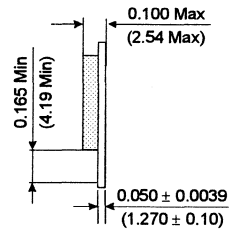
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

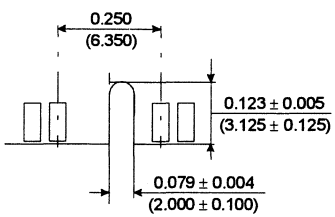
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

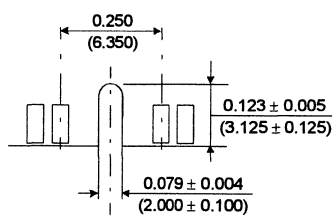




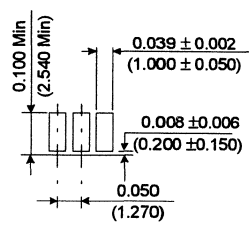




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832D

M374S0823DTS-C80/C1H/C1L

- Organization : 8Mx72
- Composition : 8Mx8 *9
- Used component part # : K4S640832D-TC80/C1H/C1L
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module rows on this assembly	1 row			01h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module row density	1 row of 64MB			10h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			F1h	17h	47h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	..... Manufacturer part # (Data bits)	7			37h			
77	..... Manufacturer part # (Data bits)	4			34h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	0			30h			
80	..... Manufacturer part # (Module depth)	8			38h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	D			44h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	S			53h			
86	Manufacturer part # (Hyphen)	"-"			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	S			53h			
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)			44h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M374S1623DT0 SDRAM DIMM

16Mx72 SDRAM DIMM with ECC based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S1623DT0 is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S1623DT0 consists of eighteen CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M374S1623DT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S1623DT0-C80	125MHz (8ns @ CL=3)
M374S1623DT0-C1H	100MHz (10ns @ CL=2)
M374S1623DT0-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ 7	Check bit (Data-in/data-out)
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

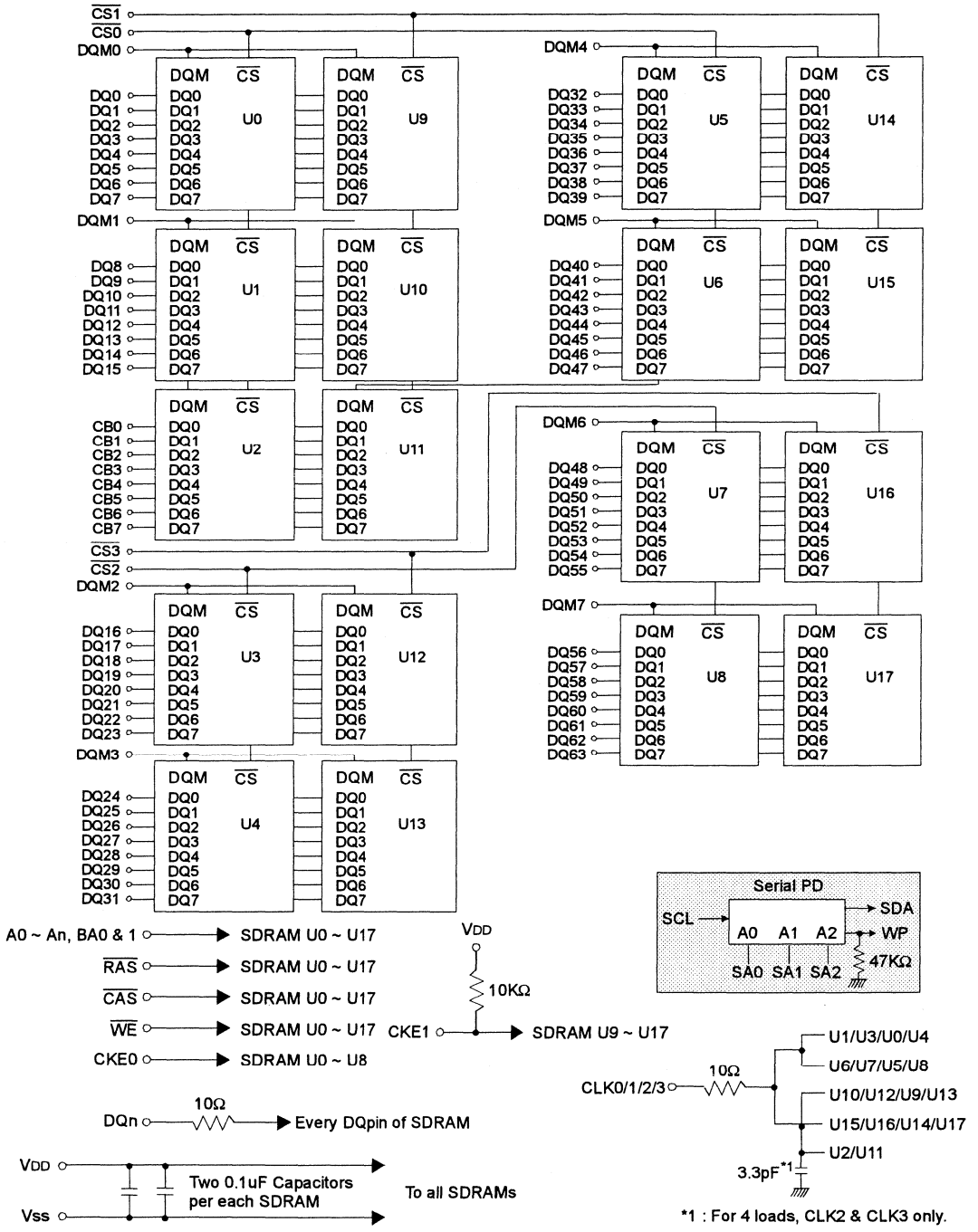
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SAMSUNG ELECTRONICS

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
WP	*Write protection*	WP pin is connected to Vss through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be wirte-protected.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	18	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C_{ADD}	50	95	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN}	50	95	pF
CKE (CKE0 ~ CKE1)	C_{CKE}	28	50	pF
Clock (CLK0 ~ CLK3)	C_{CLK}	18	25	pF
$\overline{CS}$ ($\overline{CS0}$ ~ $\overline{CS3}$)	C_{CS}	18	30	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	13	20	pF
DQ (DQ0 ~ DQ63)	C_{OUT1}	13	18	pF
CB (CB0 ~ CB7)	C_{OUT2}	13	18	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-80	-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length =1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	900	855	855	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	18			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	18				
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	270			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	108				
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	54			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	54				
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	450			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	270			mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs	1,215	1,080	1,080	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	1,395	1,350	1,350	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	18			mA	

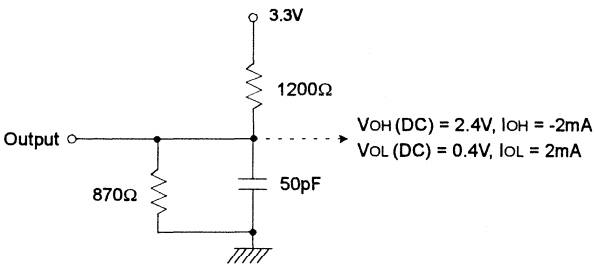
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

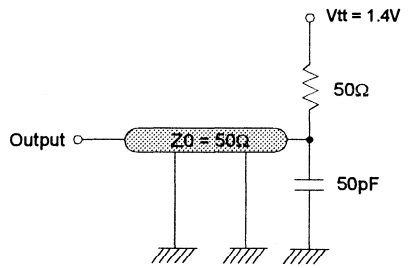
3. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	2			CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns			-	5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		-	1			

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -80/1H/1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6	ns	1,2
	CAS latency=2			-		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		-		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			-		6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A8)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A8)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

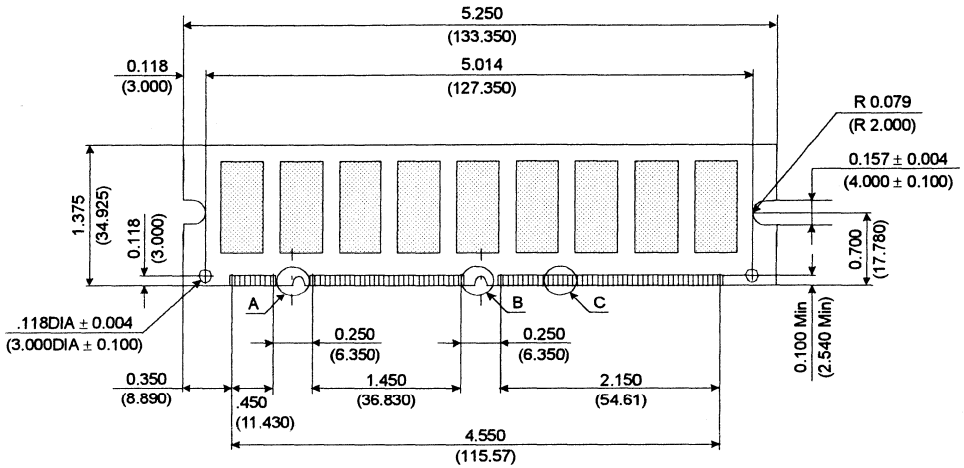
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

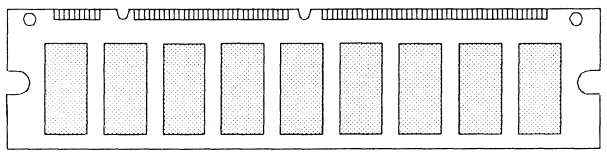
6. Burst stop command is valid at every burst length.

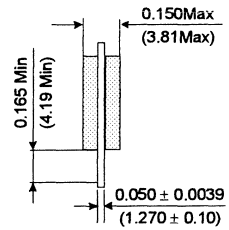
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

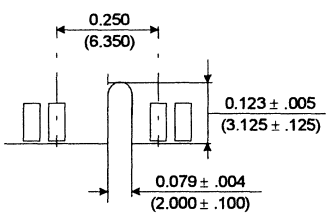
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

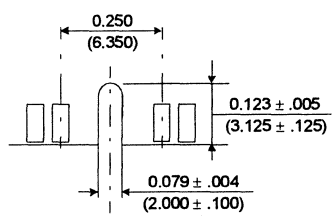




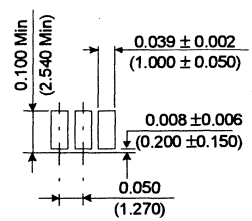




Detail A



Detail B



Detail C

Tolerances : ± .005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832D

M374S1623DT0-C80/C1H/C1L

- Organization : 16Mx72
- Composition : 8Mx8 *18
- Used component part # : K4S640832D-TC80/C1H/C1L
- # of rows in module : 2 rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module rows on this assembly	2 rows			02h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module row density	2 rows of 64MB			10h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			F2h	18h	48h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	..... Manufacturer part # (Data bits)	7			37h			
77	..... Manufacturer part # (Data bits)	4			34h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	1			31h			
80	..... Manufacturer part # (Module depth)	6			36h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	D			44h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	0			30h			
86	Manufacturer part # (Hyphen)	"-"			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	0			30h			
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)			44h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			FDh	FFh	FDh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M366S0424CT0 SDRAM DIMM

4Mx64 SDRAM DIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S0424CT0 is a 4M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S0424CT0 consists of four CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S0424CT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S0424CT0-C80	125MHz (8ns @ CL=3)
M366S0424CT0-C1H	100MHz (10ns @ CL=2)
M366S0424CT0-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)** , single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	NC	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	NC	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0, CLK2	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

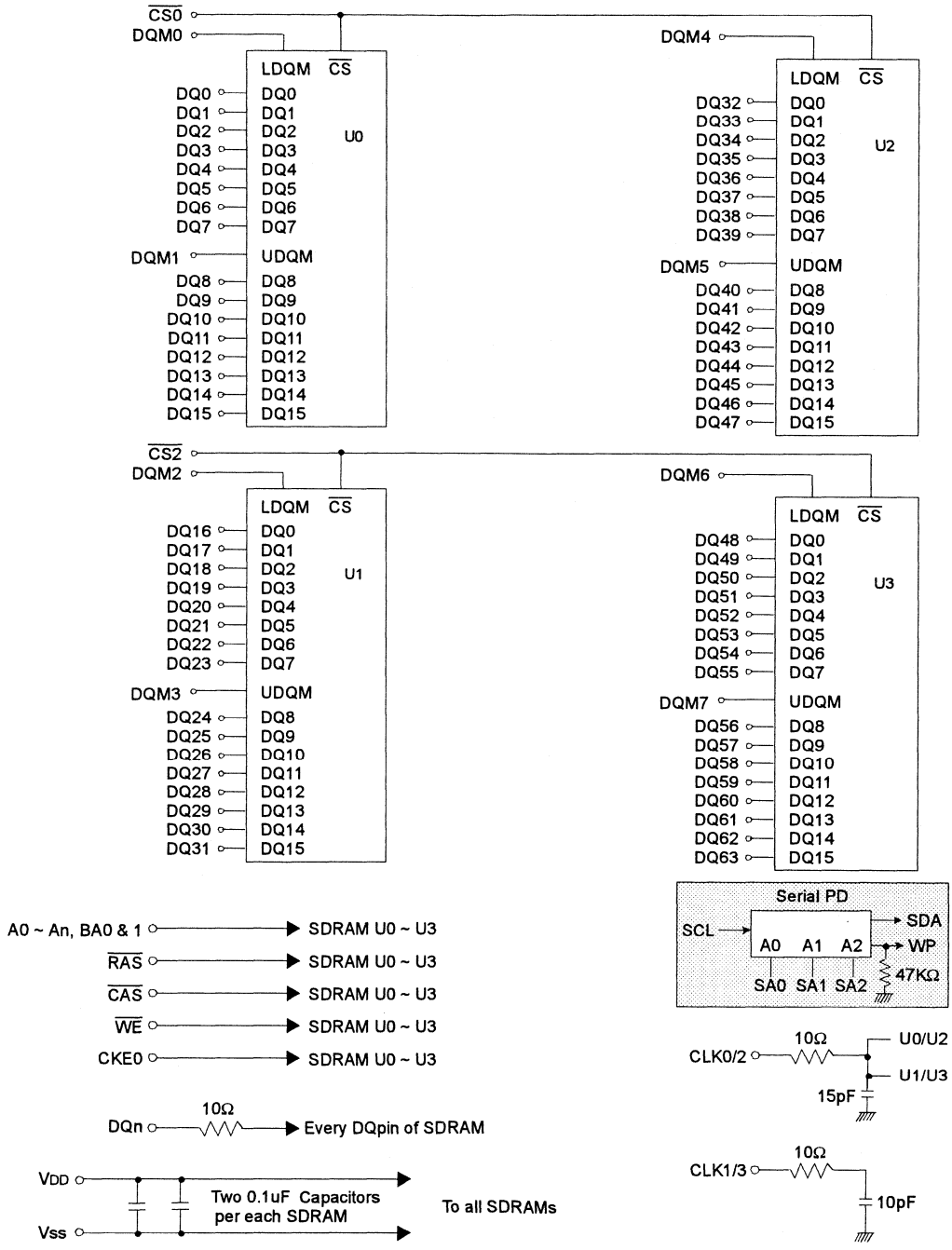
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA7
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
WP	*Write protection*	WP pin is connected to VSS through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	4	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-4	-	4	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C_{ADD}	30	40	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN}	30	40	pF
CKE (CKE0)	C_{CKE}	25	35	pF
Clock (CLK0, CLK2)	C_{CLK}	15	25	pF
$\overline{CS}$ ($\overline{CS0}$, $\overline{CS2}$)	C_{CS}	15	25	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	5	15	pF
DQ (DQ0 ~ DQ63)	C_{OUT}	5	15	pF

DC CHARACTERISTICS

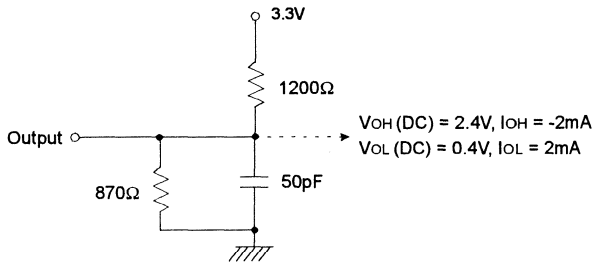
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-80	-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		300	280	280	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		4			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		4				
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		48			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		24				
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		8			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		8				
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		80			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		40			mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	380	300	300	mA	1
			2	300	300	280		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		500			mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		4			mA	

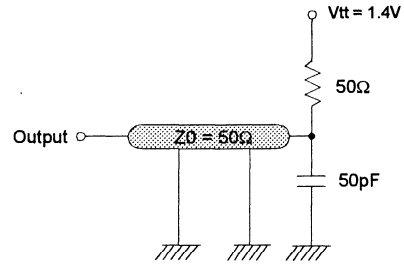
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		10		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6	ns	1, 2
	CAS latency=2			6		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			6		6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes :1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

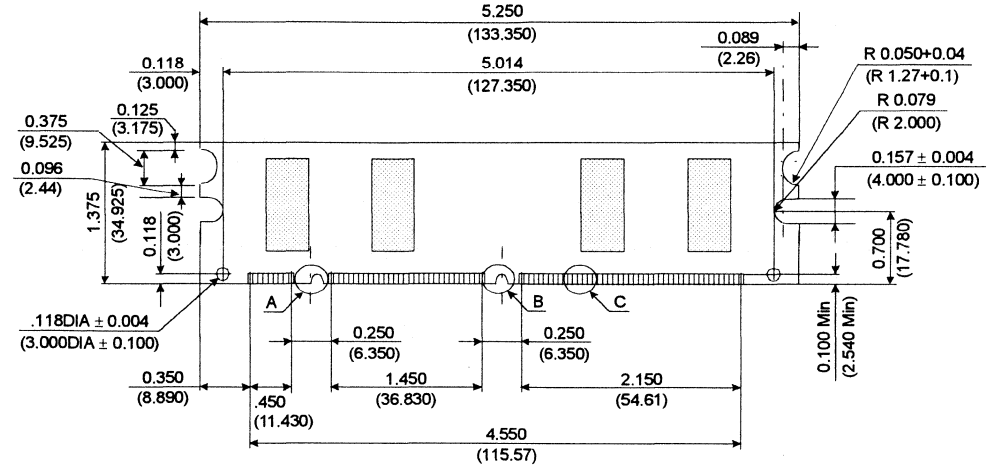
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

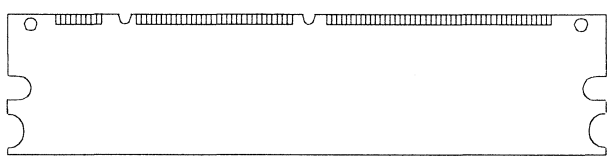
6. Burst stop command is valid at every burst length.

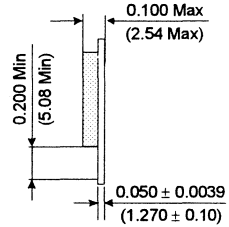
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

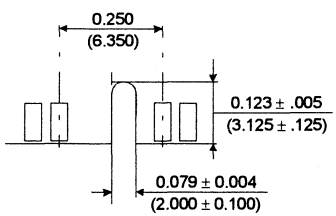
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

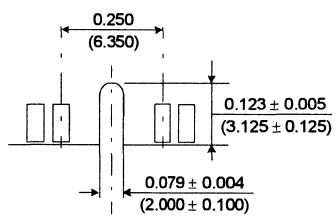




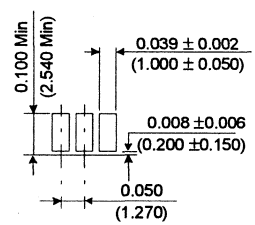




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : K4S641632C

M366S0424CT0-C80/C1H/C1L

- Organization : 4Mx64
- Composition : 4Mx16 *4
- Used component part # : K4S641632C-TC80/C1H/C1L
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	8			08h			1
5	# of module rows on this assembly	1 row			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module row density	1 row of 32MB			08h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec.Ver.1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			DEh	04h	34h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	..... Manufacturer part # (Data bits)	6			36h			
77	..... Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	0			30h			
80	..... Manufacturer part # (Module depth)	4			34h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	4			34h			
83	Manufacturer part # (Component revision)	C			43h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	0			30h			
86	Manufacturer part # (Hyphen)	"-"			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	0			30h			
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)			43h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M366S0424CTS SDRAM DIMM

4Mx64 SDRAM DIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S0424CTS is a 4M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S0424CTS consists of four CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S0424CTS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S0424CTS-C80	125MHz (8ns @ CL=3)
M366S0424CTS-C1H	100MHz (10ns @ CL=2)
M366S0424CTS-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,000mil)** , Single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	NC	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	NC	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0, CLK2	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

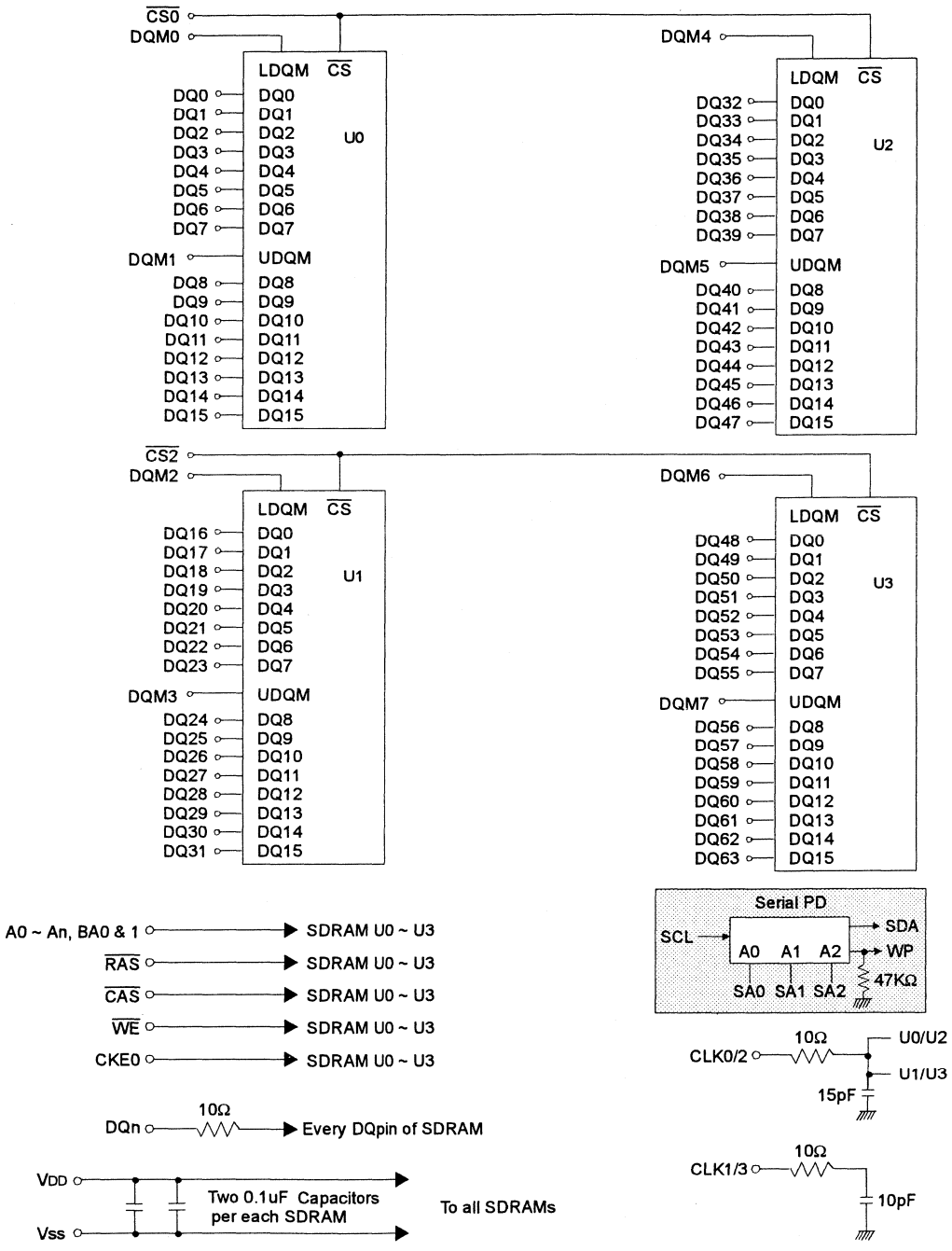
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA7
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
WP	*Write protection*	WP pin is connected to VSS through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	4	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-4	-	4	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C_{ADD}	30	40	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN}	30	40	pF
CKE (CKE0)	C_{CKE}	25	35	pF
Clock (CLK0, CLK2)	C_{CLK}	15	25	pF
$\overline{CS}$ ($\overline{CS0}$, $\overline{CS2}$)	C_{CS}	15	25	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	5	15	pF
DQ (DQ0 ~ DQ63)	C_{OUT}	5	15	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

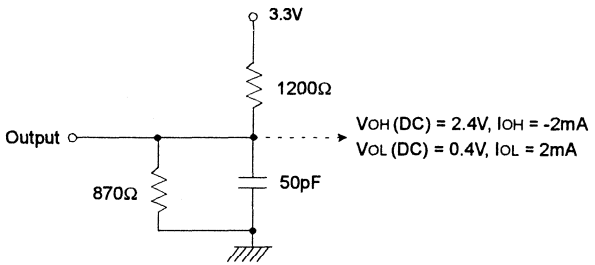
Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-80	-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		300	280	280	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		4			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		4				
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		48			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		24				
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		8			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		8				
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		80			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		40			mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	380	300	300	mA	1
			2	300	300	280		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		500			mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		4			mA	

Notes : 1. Measured with outputs open.

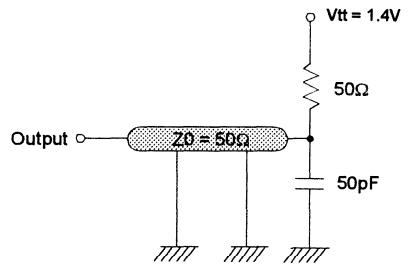
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		10		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6	ns	1, 2
	CAS latency=2			6		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			6		6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A7)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A7)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

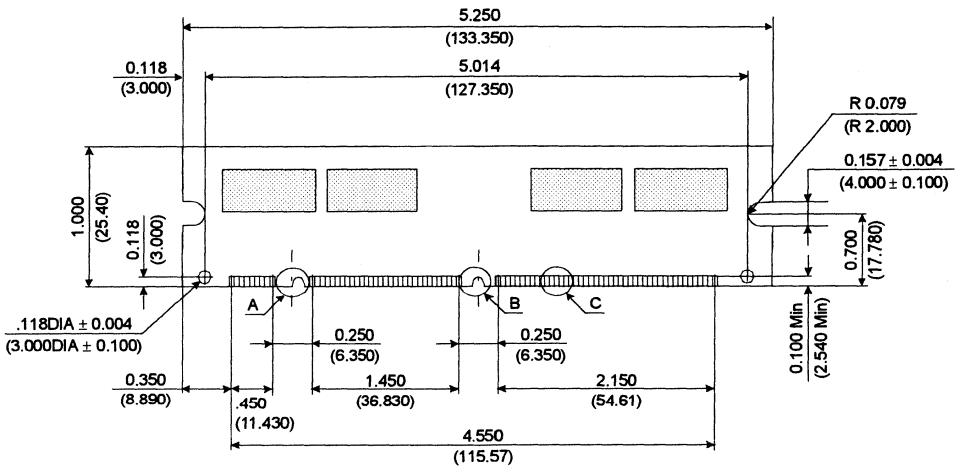
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

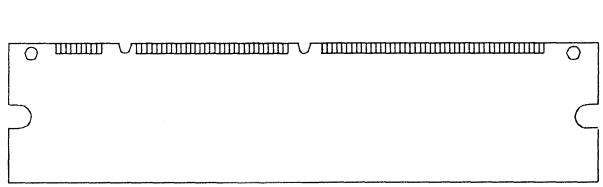
6. Burst stop command is valid at every burst length.

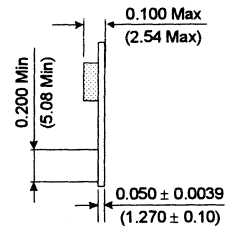
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

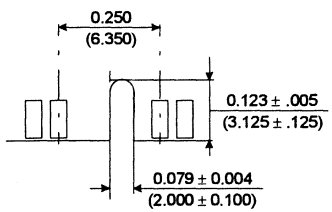
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

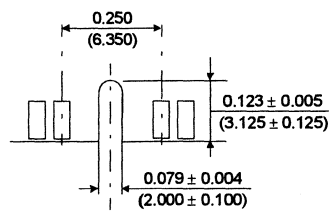




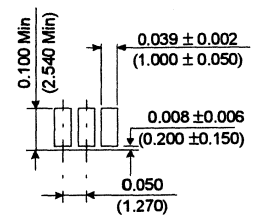




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : K4S641632C

M366S0424CTS-C80/C1H/C1L

- Organization : 4Mx64
- Composition : 4Mx16 *4
- Used component part # : K4S641632C-TC80/C1H/C1L
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,000mil height & single sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	8			08h			1
5	# of module rows on this assembly	1 row			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module row density	1 row of 32MB			08h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec.Ver.1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			DEh	04h	34h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	..... Manufacturer part # (Data bits)	6			36h			
77	..... Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	0			30h			
80	..... Manufacturer part # (Module depth)	4			34h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	4			34h			
83	Manufacturer part # (Component revision)	C			43h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	S			53h			
86	Manufacturer part # (Hyphen)	"-"			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	S			53h			
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)			43h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M366S0823CT0 SDRAM DIMM

8Mx64 SDRAM DIMM based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S0823CT0 is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S0823CT0 consists of eight CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S0823CT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S0823CT0-C80	125MHz (8ns @ CL=3)
M366S0823CT0-C1H	100MHz (10ns @ CL=2)
M366S0823CT0-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)** , single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0, CLK2	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

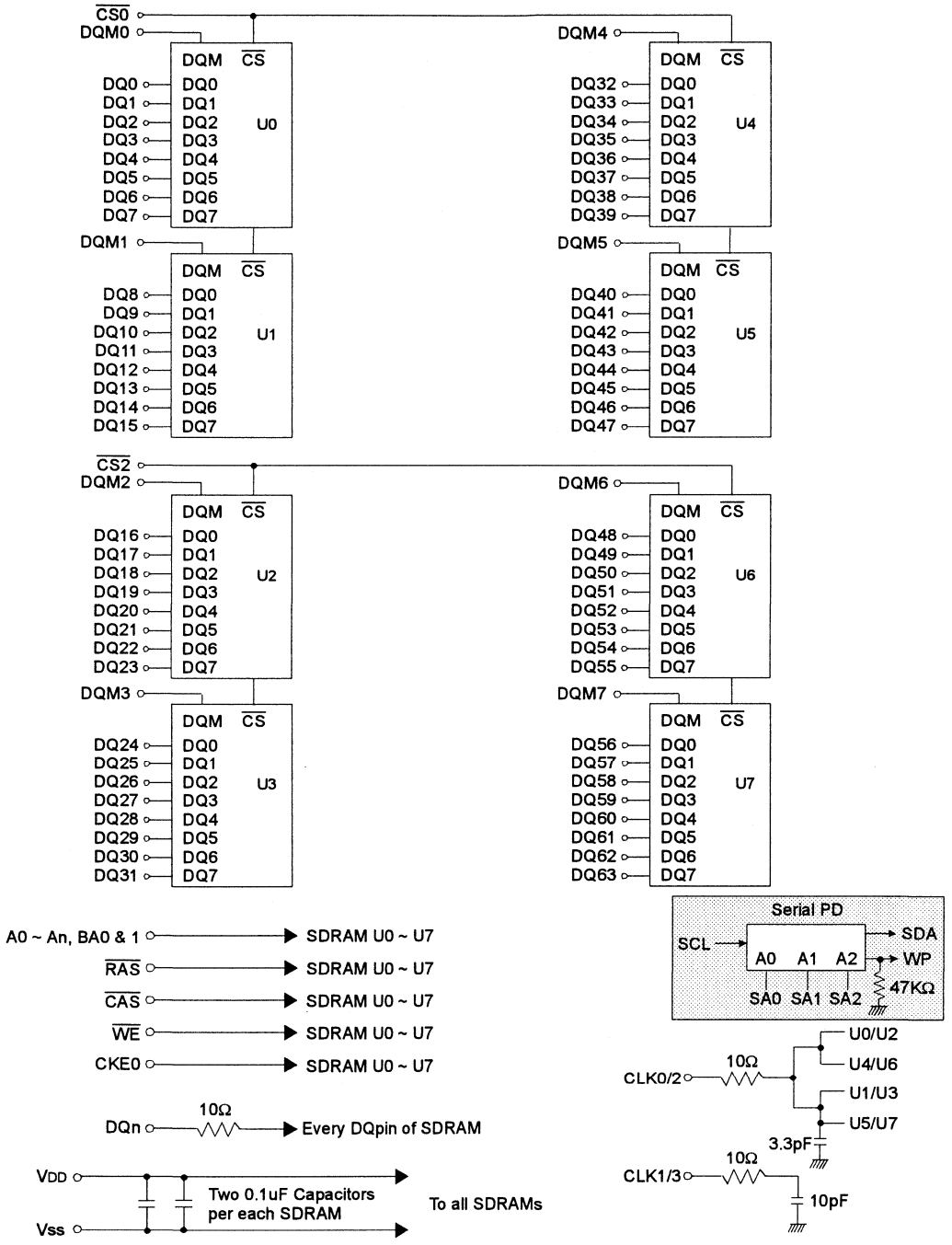
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
WP	*Write protection*	WP pin is connected to VSS through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write - protected.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high votlage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-8	-	8	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C_{ADD}	40	60	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN}	40	60	pF
CKE (CKE0)	C_{CKE}	35	55	pF
Clock (CLK0, CLK2)	C_{CLK}	25	35	pF
$\overline{CS}$ ($\overline{CS0}$, $\overline{CS2}$)	C_{CS}	25	35	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	5	15	pF
DQ (DQ0 ~ DQ63)	C_{OUT}	5	15	pF

DC CHARACTERISTICS

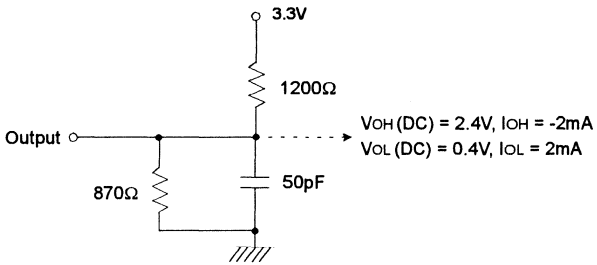
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-80	-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		600	560	560	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		8			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		8				
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		96			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		48				
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		16			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		16				
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		160			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		80			mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	760	600	600	mA	1
			2	600	600	560		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,000			mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		8			mA	

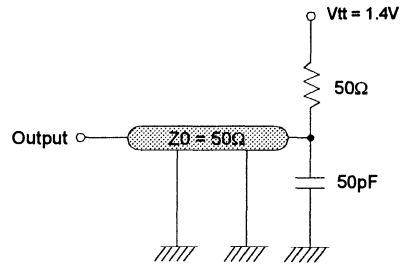
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS Latency=3		2			ea	4
	CAS Latency=2		1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		10		10		12			
CLK to valid output delay	CAS latency=3	t_{SAC}		6		6		6	ns	1,2
	CAS latency=2			6		6		7		
Output data hold time	CAS latency=3	t_{OH}	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		t_{CH}	3		3		3		ns	3
CLK low pulse width		t_{CL}	3		3		3		ns	3
Input setup time		t_{SS}	2		2		2		ns	3
Input hold time		t_{SH}	1		1		1		ns	3
CLK to output in Low-Z		t_{SLZ}	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		6		6		6	ns	
	CAS latency=2			6		6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

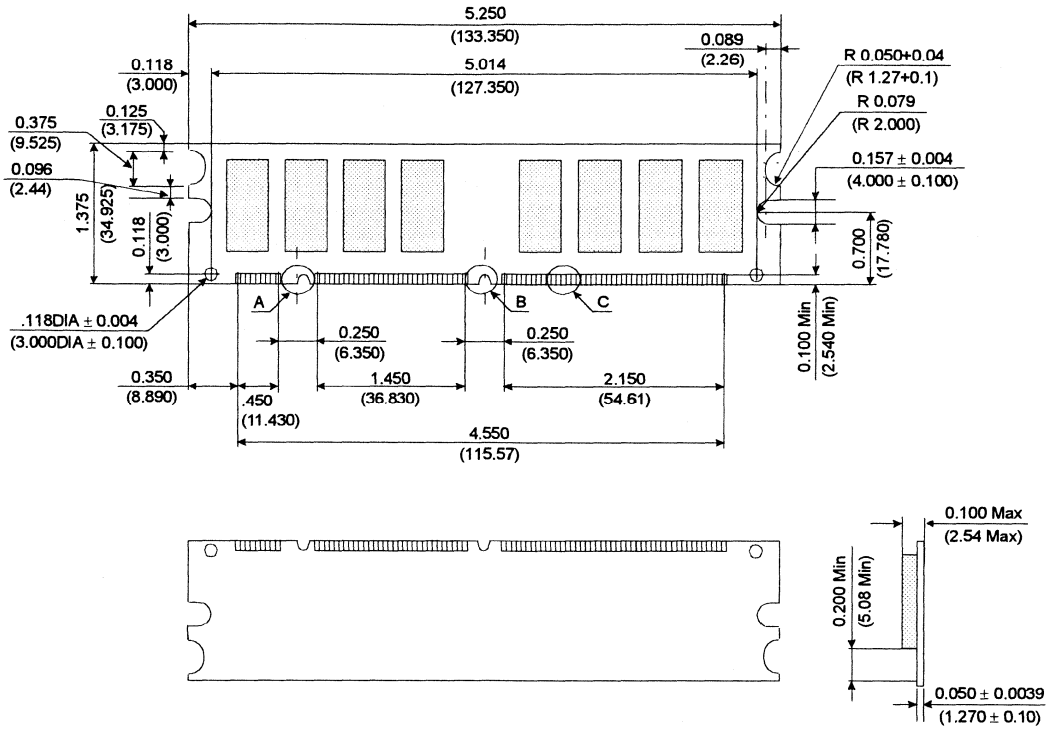
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

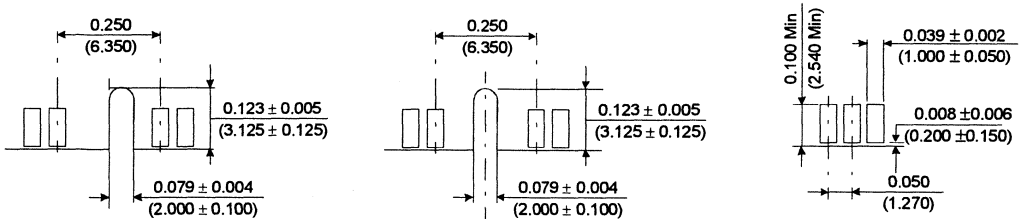
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)





Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832C

SAMSUNG ELECTRONICS

M366S0823CT0-C80/C1H/C1L

- Organization : 8Mx64
- Composition : 8Mx8 *8
- Used component part # : K4S640832C-TC80/C1H/C1L
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module rows on this assembly	1 row			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module row density	1 row of 64MB			10h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8O	-1H	-1L	-8O	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			DFh	05h	35h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	..... Manufacturer part # (Data bits)	6			36h			
77	..... Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	0			30h			
80	..... Manufacturer part # (Module depth)	8			38h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	C			43h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	0			30h			
86	Manufacturer part # (Hyphen)	"-"			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	0			30h			
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)			43h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M366S0823CTS SDRAM DIMM

8Mx64 SDRAM DIMM based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S0823CTS is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S0823CTS consists of eight CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. One 0.1uF and one 0.33 uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S0823CTS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S0823CTS -C80	125MHz (8ns @ CL=3)
M366S0823CTS -C1H	100MHz (10ns @ CL=2)
M366S0823CTS -C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)** , single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0, CLK2	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

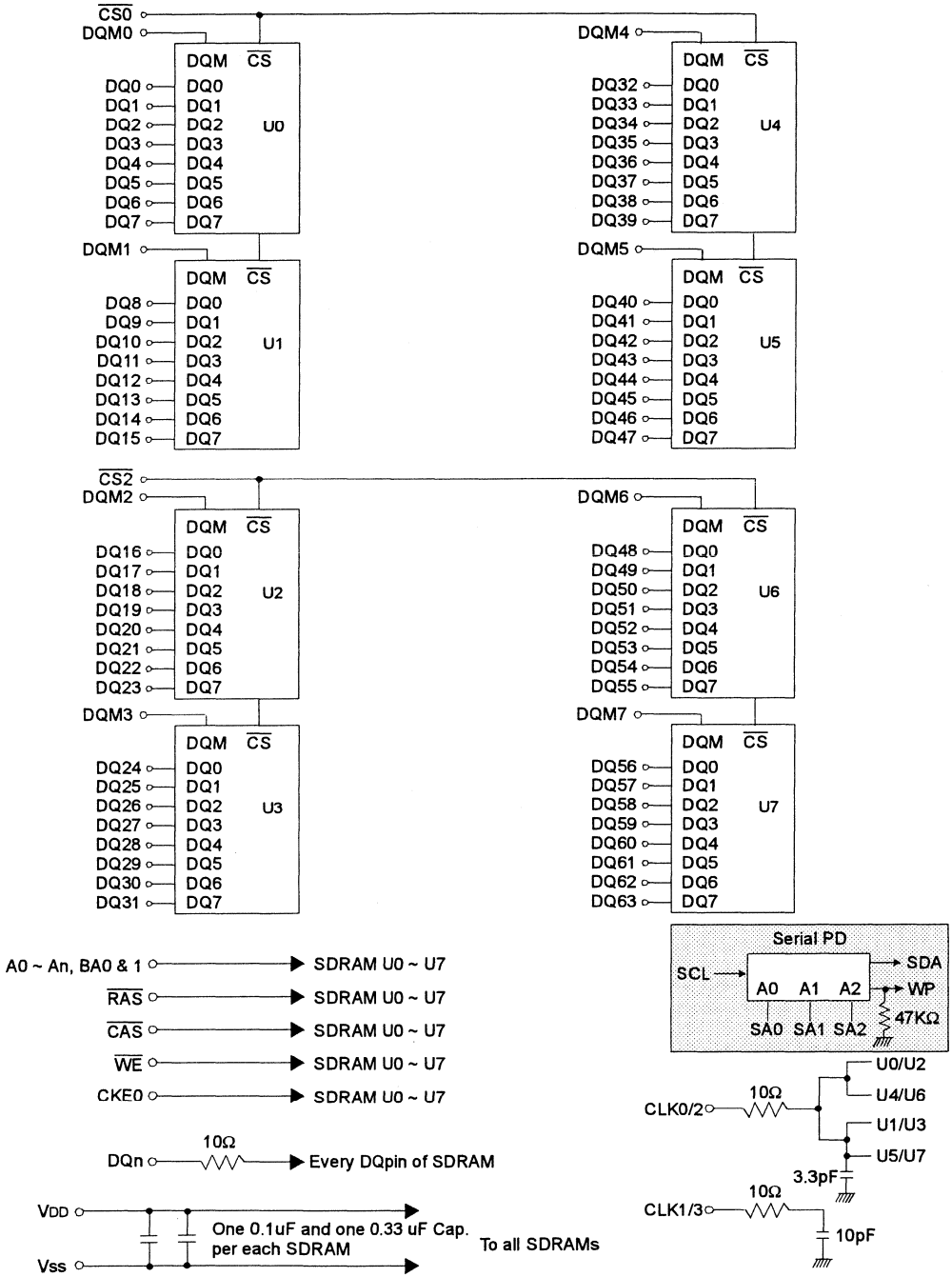
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
WP	*Write protection*	WP pin is connected to VSS through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write - protected.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high votlage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-8	-	8	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C_{ADD}	40	60	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN}	40	60	pF
CKE (CKE0)	C_{CKE}	35	55	pF
Clock (CLK0, CLK2)	C_{CLK}	25	35	pF
$\overline{CS}$ ($\overline{CS0}$, $\overline{CS2}$)	C_{CS}	25	35	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	5	15	pF
DQ (DQ0 ~ DQ63)	C_{OUT}	5	15	pF

DC CHARACTERISTICS

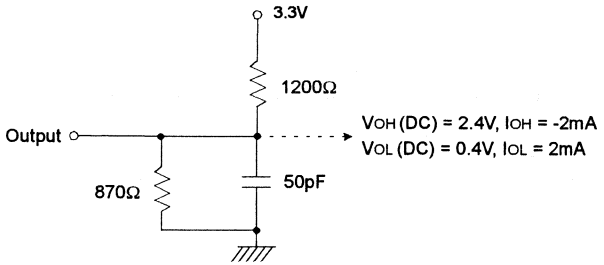
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-80	-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		600	560	560	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		8			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		8				
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		96			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		48				
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		16			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		16				
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		160			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		80			mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	760	600	600	mA	1
			2	600	600	560		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,000			mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		8			mA	

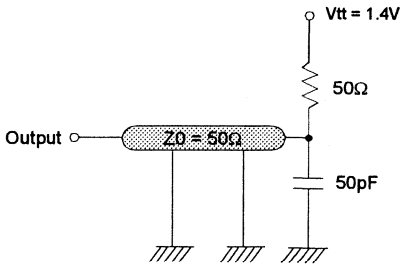
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS Latency=3		2			ea	4
	CAS Latency=2		1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		10		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6	ns	1,2
	CAS latency=2			6		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			6		6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

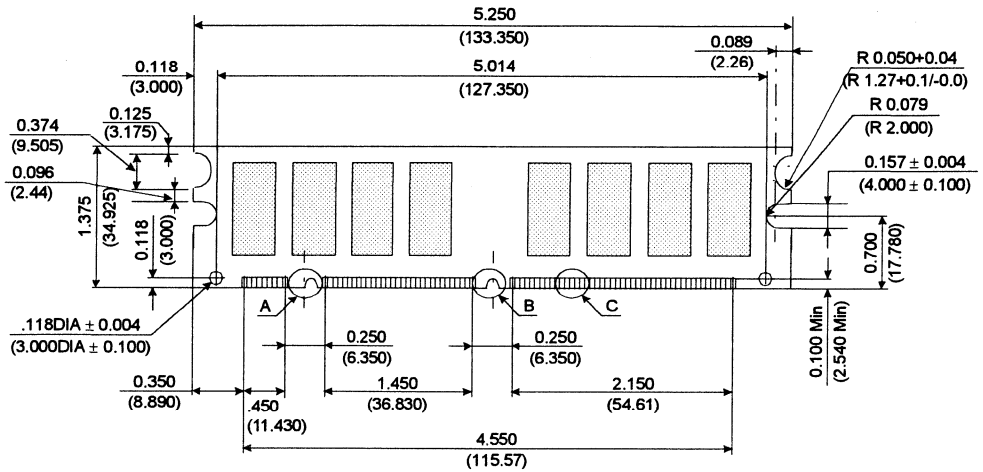
Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A8)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A8)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

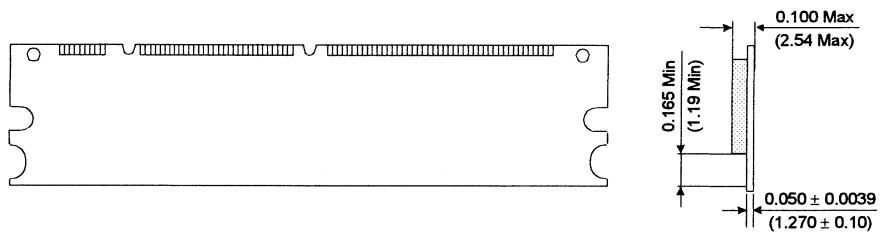
(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

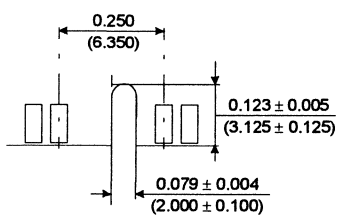
Notes : 1. OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at tRP after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

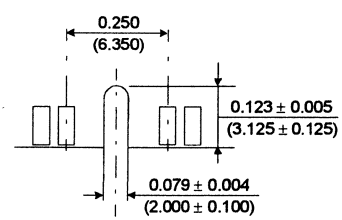
Units : Inches (Millimeters)



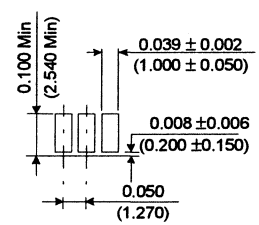




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832C

M366S0823CTS-C80/C1H/C1L

- Organization : 8Mx64
- Composition : 8Mx8 *8
- Used component part # : K4S640832C-TC80/C1H/C1L
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module rows on this assembly	1 row			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module row density	1 row of 64MB			10h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8O	-1H	-1L	-8O	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			DFh	05h	35h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	..... Manufacturer part # (Data bits)	6			36h			
77	..... Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	0			30h			
80	..... Manufacturer part # (Module depth)	8			38h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	C			43h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	S			53h			
86	Manufacturer part # (Hyphen)	"-"			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	S			53h			
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)			43h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M366S0824CT0 SDRAM DIMM

8Mx64 SDRAM DIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S0824CT0 is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S0824CT0 consists of eight CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S0824CT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S0824CT0-C80	125MHz (8ns @ CL=3)
M366S0824CT0-C1H	100MHz (10ns @ CL=2)
M366S0824CT0-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	NC	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	NC	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

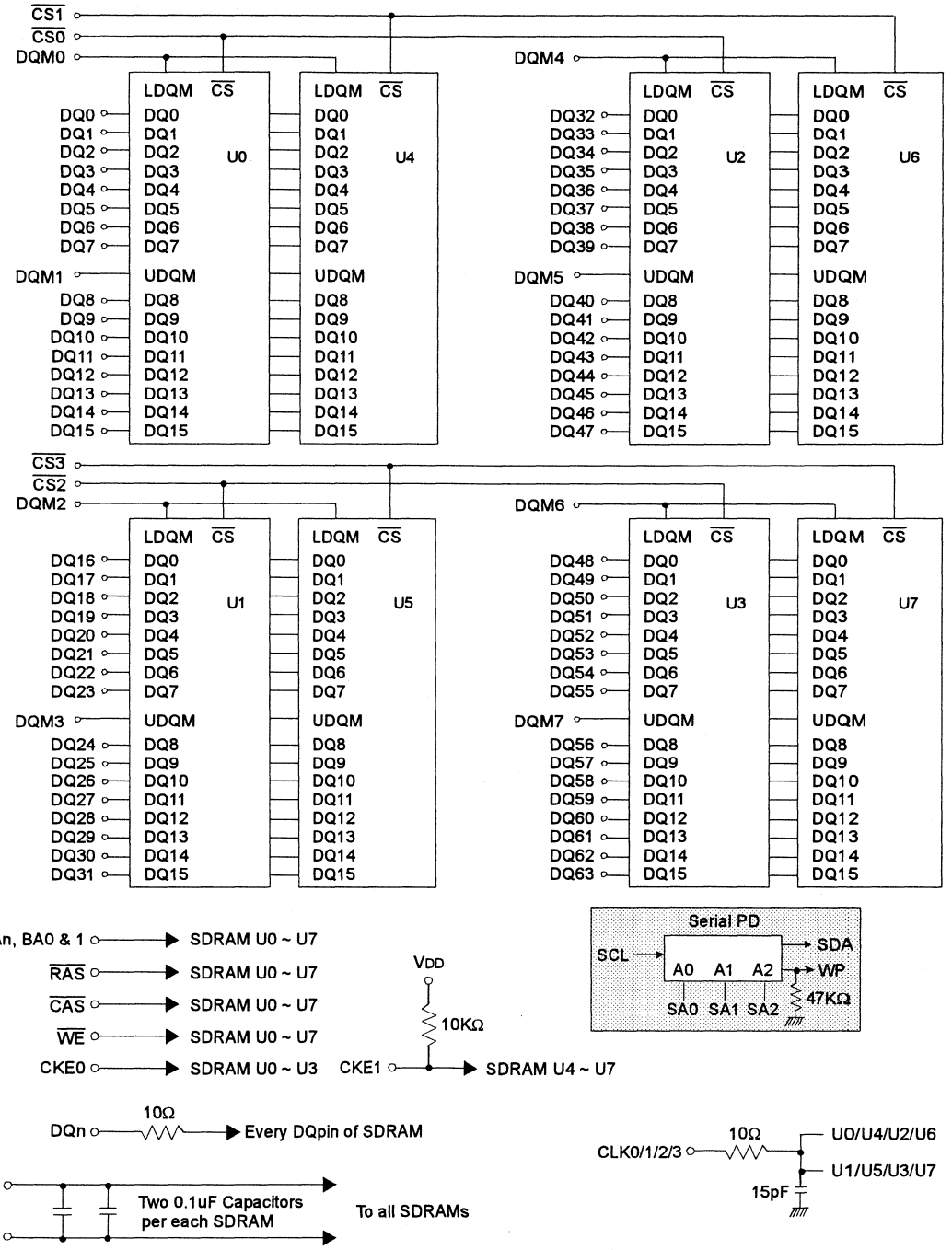
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, column address : CA0 ~ CA7
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
WP	*Write protection*	WP pin is connected to VSS through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-8	-	8	uA	3
Input leakage current (I/O pins)	I_{IL}	-3	-	3	uA	3,4

Note : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C_{ADD}	40	60	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN}	40	60	pF
CKE (CKE0)	C_{CKE}	25	35	pF
Clock (CLK0, CLK2)	C_{CLK}	15	25	pF
$\overline{CS}$ ($\overline{CS0}$, $\overline{CS2}$)	C_{CS}	15	25	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	5	15	pF
DQ (DQ0 ~ DQ63)	C_{OUT}	5	15	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

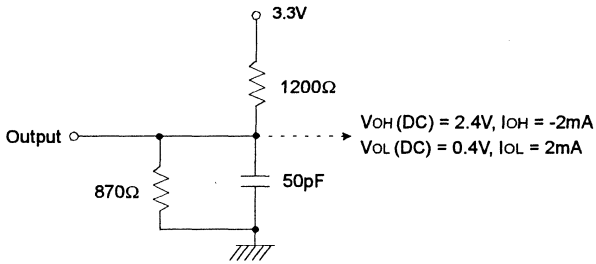
Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-80	-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		380	360	360	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		8			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		8				
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		96			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		48				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		16			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		16				
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		160			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		80			mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	460	380	380	mA	1
			2	380	380	360		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,000			mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		8			mA	

Notes : 1. Measured with outputs open.

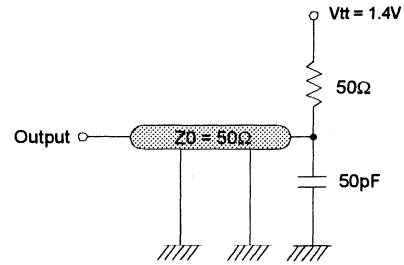
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		10		10		12			
CLK to valid output delay	CAS latency=3	t_{SAC}		6		6		6	ns	1,2
	CAS latency=2			6		6		7		
Output data hold time	CAS latency=3	t_{OH}	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		t_{CH}	3		3		3		ns	3
CLK low pulse width		t_{CL}	3		3		3		ns	3
Input setup time		t_{SS}	2		2		2		ns	3
Input hold time		t_{SH}	1		1		1		ns	3
CLK to output in Low-Z		t_{SLZ}	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		6		6		6	ns	
	CAS latency=2			6		6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

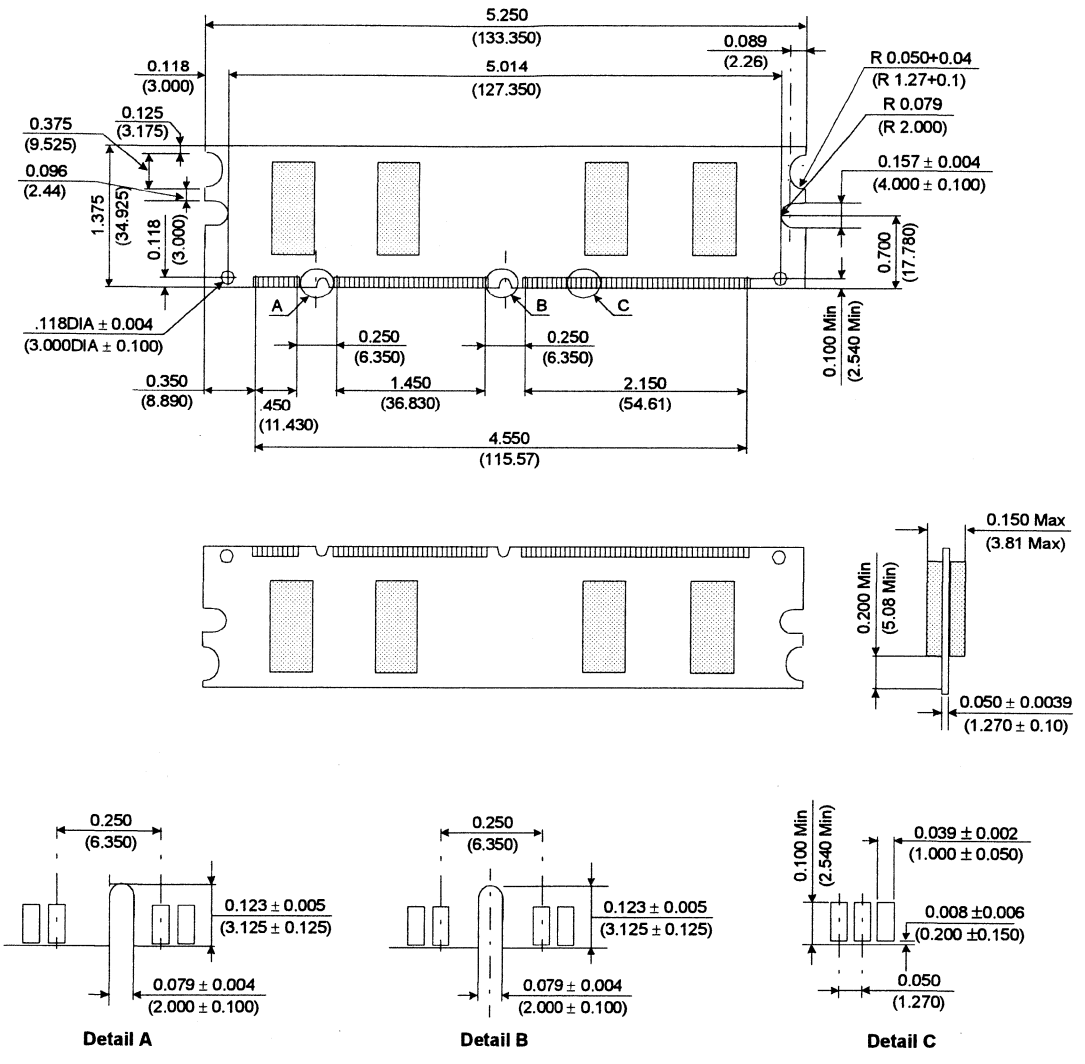
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : K4S641632C

M366S0824CT0-C80/C1H/C1L

- Organization : 8Mx64
- Composition : 4Mx16 *8
- Used component part # : K4S641632C-TC80/C1H/C1L
- # of rows in module : 2 rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	8			08h			1
5	# of module rows on this assembly	2 rows			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module row density	2 rows of 32MB			08h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			DFh	05h	35h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	..... Manufacturer part # (Data bits)	6			36h			
77	..... Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	0			30h			
80	..... Manufacturer part # (Module depth)	8			38h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	4			34h			
83	Manufacturer part # (Component revision)	C			43h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	0			30h			
86	Manufacturer part # (Hyphen)	"-"			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	0			30h			
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)			43h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			FDh	FFh	FDh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M366S1623CT0 SDRAM DIMM

16Mx64 SDRAM DIMM based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S1623CT0 is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S1623CT0 consists of sixteen CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S1623CT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
KMM366S1623CT-C80	125MHz (8ns @ CL=3)
KMM366S1623CT-C1H	100MHz (10ns @ CL=2)
KMM366S1623CT-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

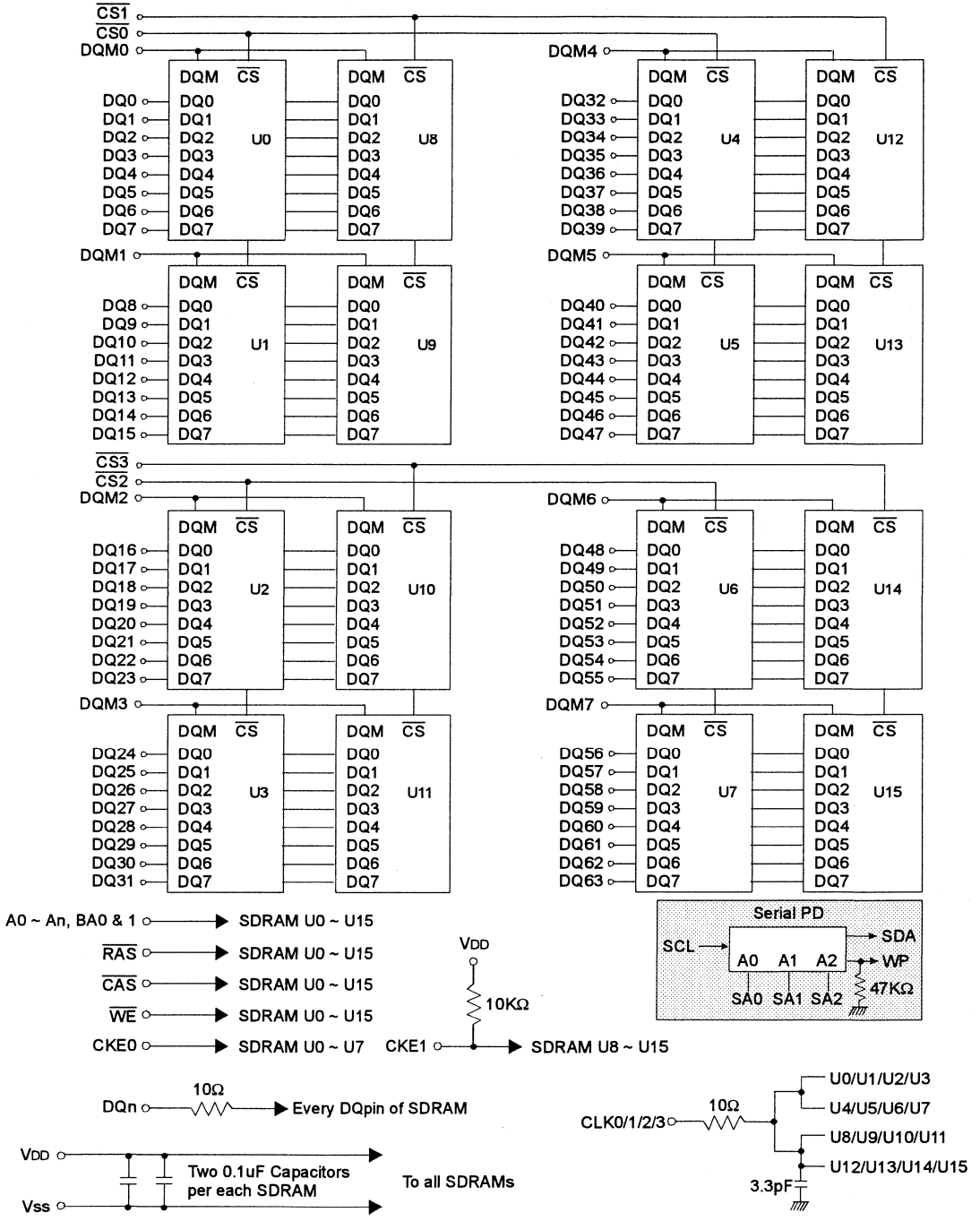
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
WP	*Write protection*	WP pin is connected to VSS through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	16	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-16	-	16	uA	3
Input leakage current (I/O pins)	I_{IL}	-3	-	3	uA	3,4

Note : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C_{ADD}	60	90	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN}	60	90	pF
CKE (CKE0 ~ CKE1)	C_{CKE}	35	55	pF
Clock (CLK0 ~ CLK3)	C_{CLK}	25	35	pF
$\overline{CS}$ ($\overline{CS0}$~$\overline{CS3}$)	C_{CS}	25	35	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	15	25	pF
DQ (DQ0 ~ DQ63)	C_{OUT}	10	20	pF

DC CHARACTERISTICS

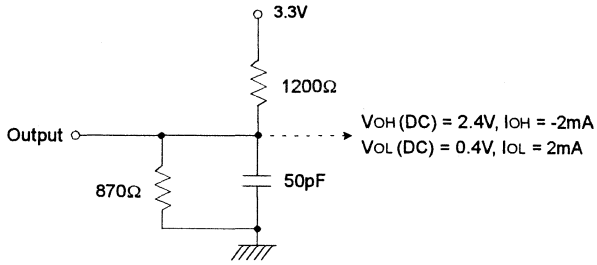
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-80	-1H	-1L		
Operating current (one Bank Active)	I_{CC1}	Burst length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		760	720	720	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		16			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		16				
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		192			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		96				
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		32			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		32				
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		320			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		160			mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	920	760	760	mA	1
			2	760	760	720		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		2,000			mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		16			mA	

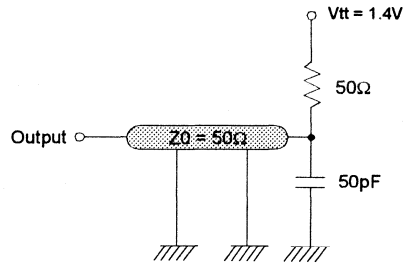
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		10		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6	ns	1,2
	CAS latency=2			6		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			6		6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

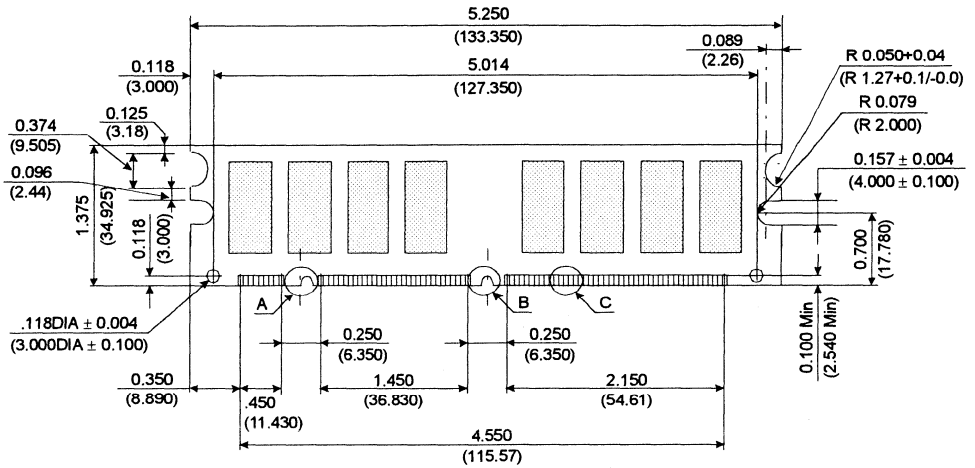
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

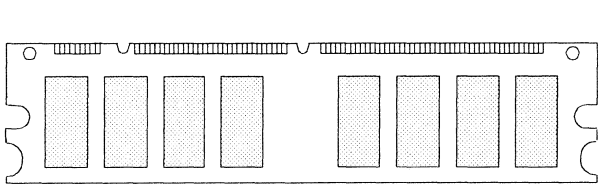
6. Burst stop command is valid at every burst length.

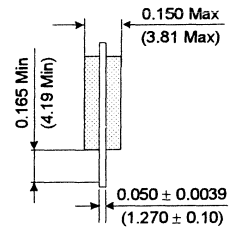
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

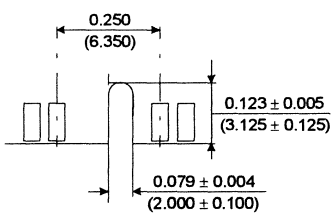
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

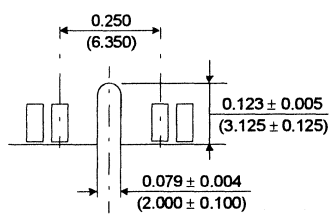




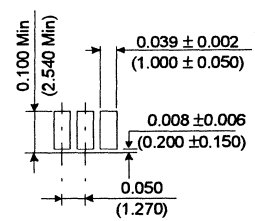




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832C

M366S1623CT0- C80/C1H/C1L

- Organization : 16Mx64
- Composition : 8Mx8 *16
- Used component part # : K4S640832C-TC80/C1H/C1L
- # of rows in module : 2 rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-11L	-80	-H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module rows on this assembly	2 rows			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time from clock@CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock@CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module row density	2 rows of 64MB			10h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8D	-1H	-1L	-8D	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			E0h	06h	36h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	..... Manufacturer part # (Data bits)	6			36h			
77	..... Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	1			31h			
80	..... Manufacturer part # (Module depth)	6			36h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	C			43h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	0			30h			
86	Manufacturer part # (Hyphen)	"-"			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	0			30h			
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)			43h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			FDh	FFh	FDh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M374S0823CT0 SDRAM DIMM

8Mx72 SDRAM DIMM with ECC based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S0823CT0 is a 8M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S0823CT0 consists of nine CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M374S0823CT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S0823CT0-C80	125MHz (8ns @ CL=3)
M374S0823CT0-C1H	100MHz (10ns @ CL=2)
M374S0823CT0-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)** , single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0, CLK2	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

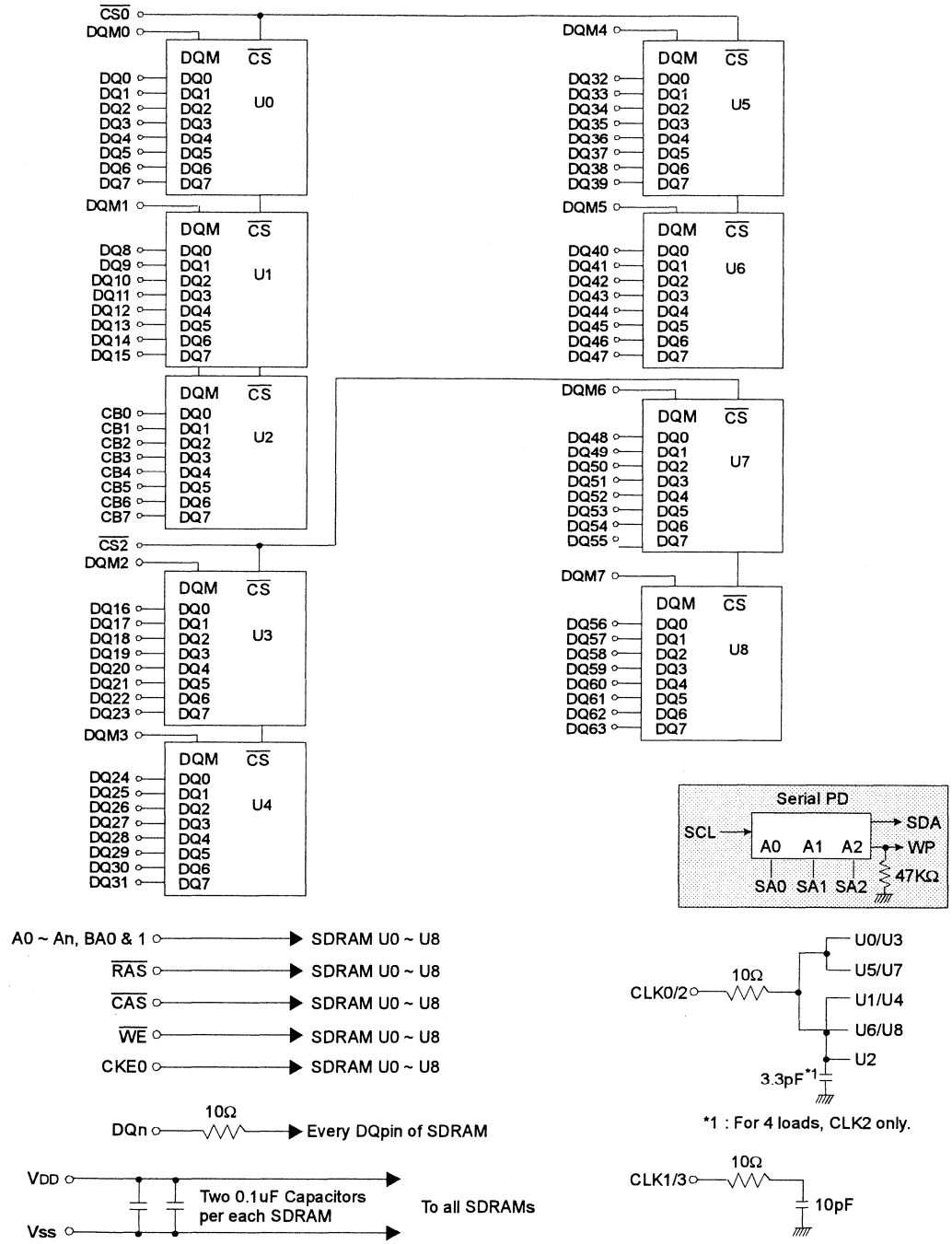
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
WP	*Write protection*	WP pin is connected to VSS through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write - protected.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	9	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-9	-	9	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Note : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C_{ADD}	45	65	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN}	45	65	pF
CKE (CKE0)	C_{CKE}	40	60	pF
Clock (CLK0, CLK2)	C_{CLK}	30	40	pF
$\overline{CS}$ ($\overline{CS0}$, $\overline{CS2}$)	C_{CS}	30	40	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	5	15	pF
DQ (DQ0 ~ DQ63)	C_{OUT1}	5	15	pF
CB (CB0 ~ CB7)	C_{OUT2}	5	15	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

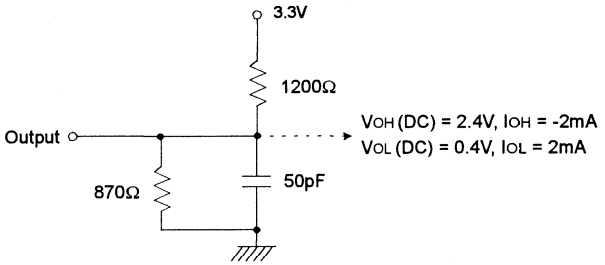
Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-80	-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		675	630	630	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		9			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		9				
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		108			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		54				
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		18			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		18				
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		180			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		90			mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	855	675	675	mA	1
			2	675	675	630		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,125			mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		9			mA	

Notes : 1. Measured with outputs open.

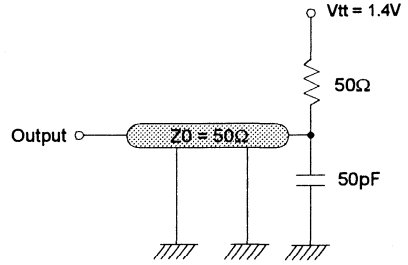
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		12		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6	ns	1,2
	CAS latency=2			6		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			6		6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

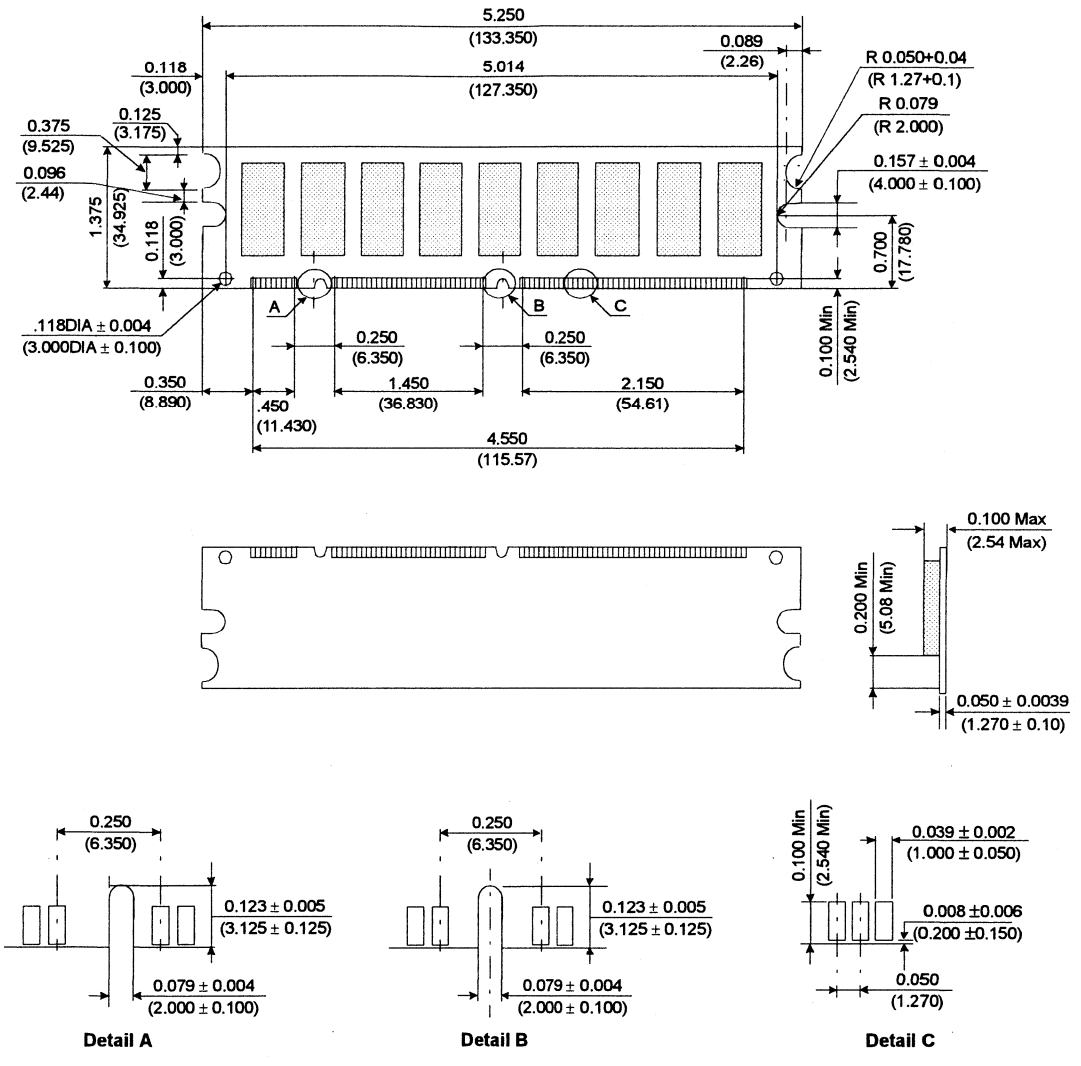
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832C

M374S0823CT0-C80/C1H/C1L

- Organization : 8Mx72
- Composition : 8Mx8 *9
- Used component part # : K4S640832C-TC80/C1H/C1L
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module rows on this assembly	1 row			01h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module row density	1 row of 64MB			10h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8D	-1H	-1L	-8D	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			F1h	17h	47h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	..... Manufacturer part # (Data bits)	7			37h			
77	..... Manufacturer part # (Data bits)	4			34h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	0			30h			
80	..... Manufacturer part # (Module depth)	8			38h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	C			43h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	0			30h			
86	Manufacturer part # (Hyphen)	"-"			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	0			30h			
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)			43h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M374S0823CTS SDRAM DIMM

8Mx72 SDRAM DIMM with ECC based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S0823CTS is a 8M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S0823CTS consists of nine CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. One 0.1uF and one 0.33 uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M374S0823CTS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S0823CTS-C80	125MHz (8ns @ CL=3)
M374S0823CTS-C1H	100MHz (10ns @ CL=2)
M374S0823CTS-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)** , single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0, CLK2	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

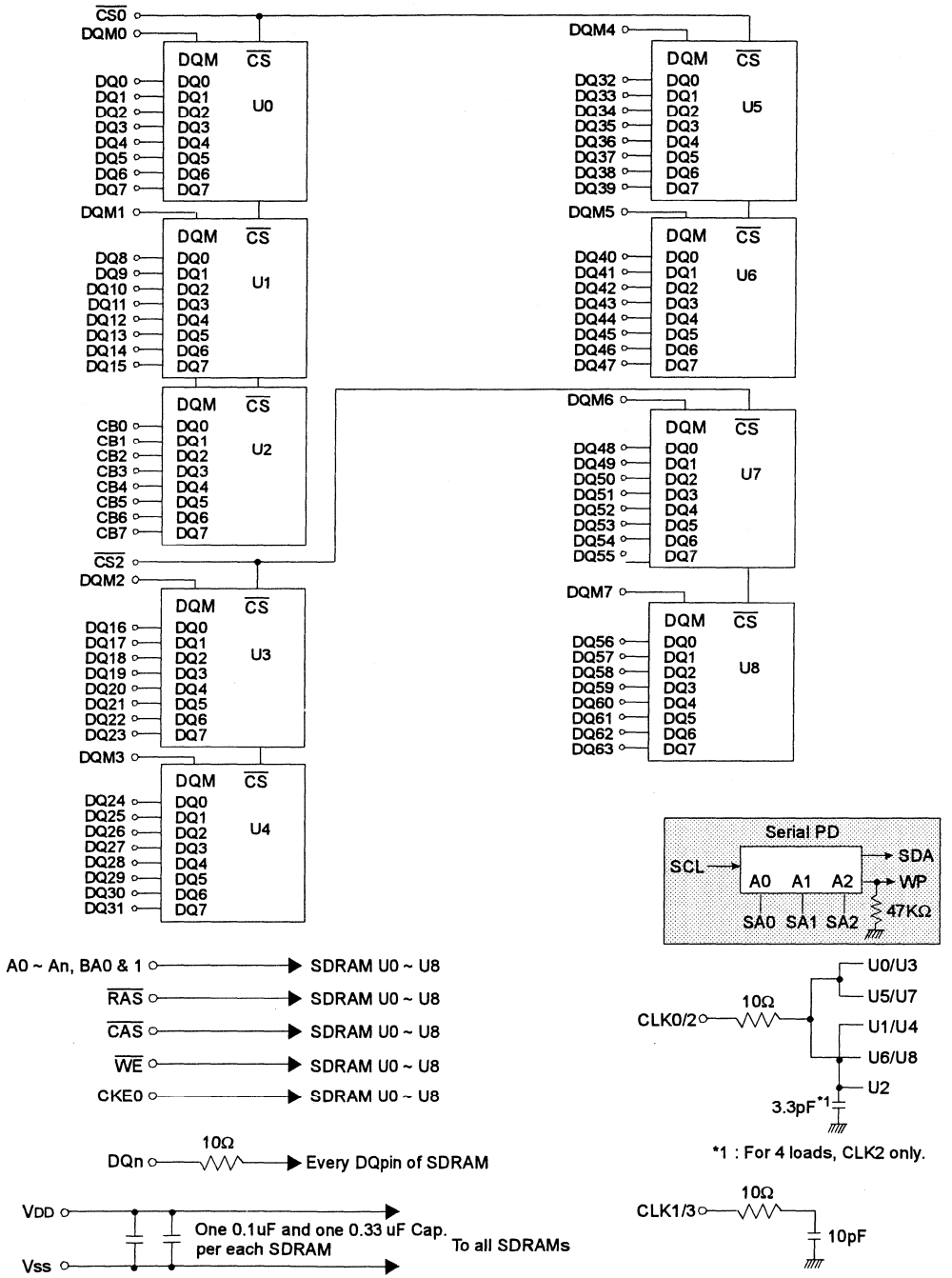
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
WP	*Write protection*	WP pin is connected to VSS through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write - protected.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	9	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-9	-	9	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Note : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C_{ADD}	45	65	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN}	45	65	pF
CKE (CKE0)	C_{CKE}	40	60	pF
Clock (CLK0, CLK2)	C_{CLK}	30	40	pF
$\overline{CS}$ ($\overline{CS0}$, $\overline{CS2}$)	C_{CS}	30	40	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	5	15	pF
DQ (DQ0 ~ DQ63)	C_{OUT1}	5	15	pF
CB (CB0 ~ CB7)	C_{OUT2}	5	15	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

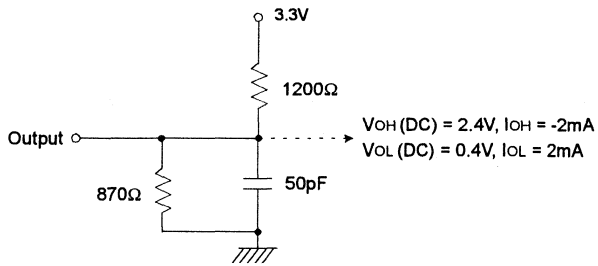
Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-80	-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		675	630	630	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		9			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		9				
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		108			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		54				
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		18			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		18				
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		180			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		90			mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	855	675	675	mA	1
			2	675	675	630		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,125			mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		9			mA	

Notes : 1. Measured with outputs open.

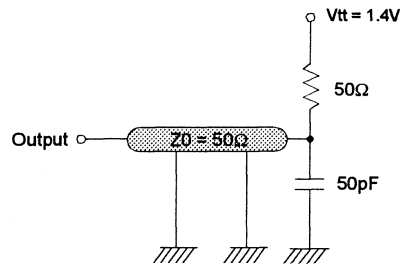
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		12		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6	ns	1,2
	CAS latency=2			6		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			6		6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A8)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A8)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

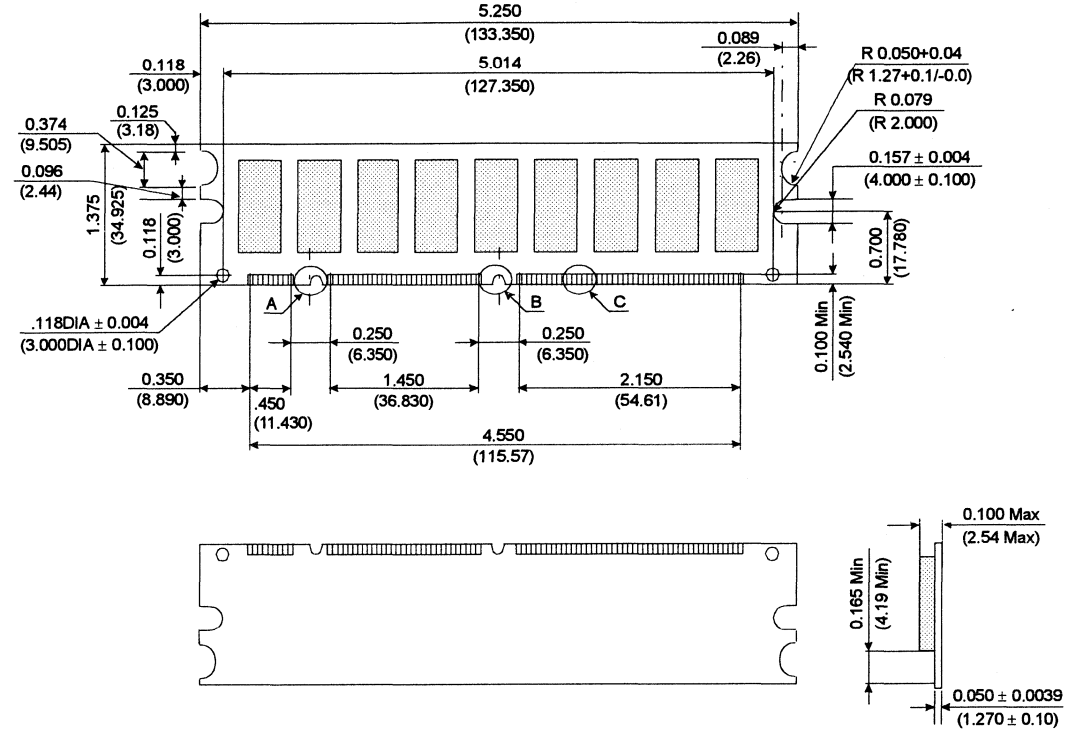
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

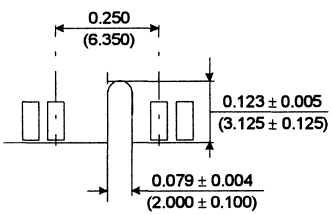
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

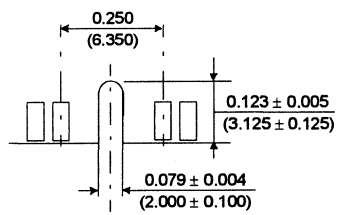
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

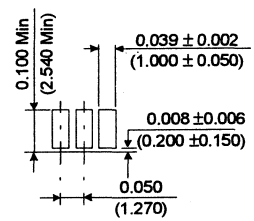




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832C

M374S0823CTS-C80/C1H/C1L

- Organization : 8Mx72
- Composition : 8Mx8 *9
- Used component part # : K4S640832C-TC80/C1H/C1L
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module rows on this assembly	1 row			01h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module row density	1 row of 64MB			10h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			F1h	17h	47h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	..... Manufacturer part # (Data bits)	7			37h			
77	..... Manufacturer part # (Data bits)	4			34h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	0			30h			
80	..... Manufacturer part # (Module depth)	8			38h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	C			43h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	S			53h			
86	Manufacturer part # (Hyphen)	"-"			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	S			53h			
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)			43h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M374S1623CT0 SDRAM DIMM

16Mx72 SDRAM DIMM with ECC based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S1623CT0 is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S1623CT0 consists of eighteen CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M374S1623CT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S1623CT0-C80	125MHz (8ns @ CL=3)
M374S1623CT0-C1H	100MHz (10ns @ CL=2)
M374S1623CT0-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ 7	Check bit (Data-in/data-out)
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

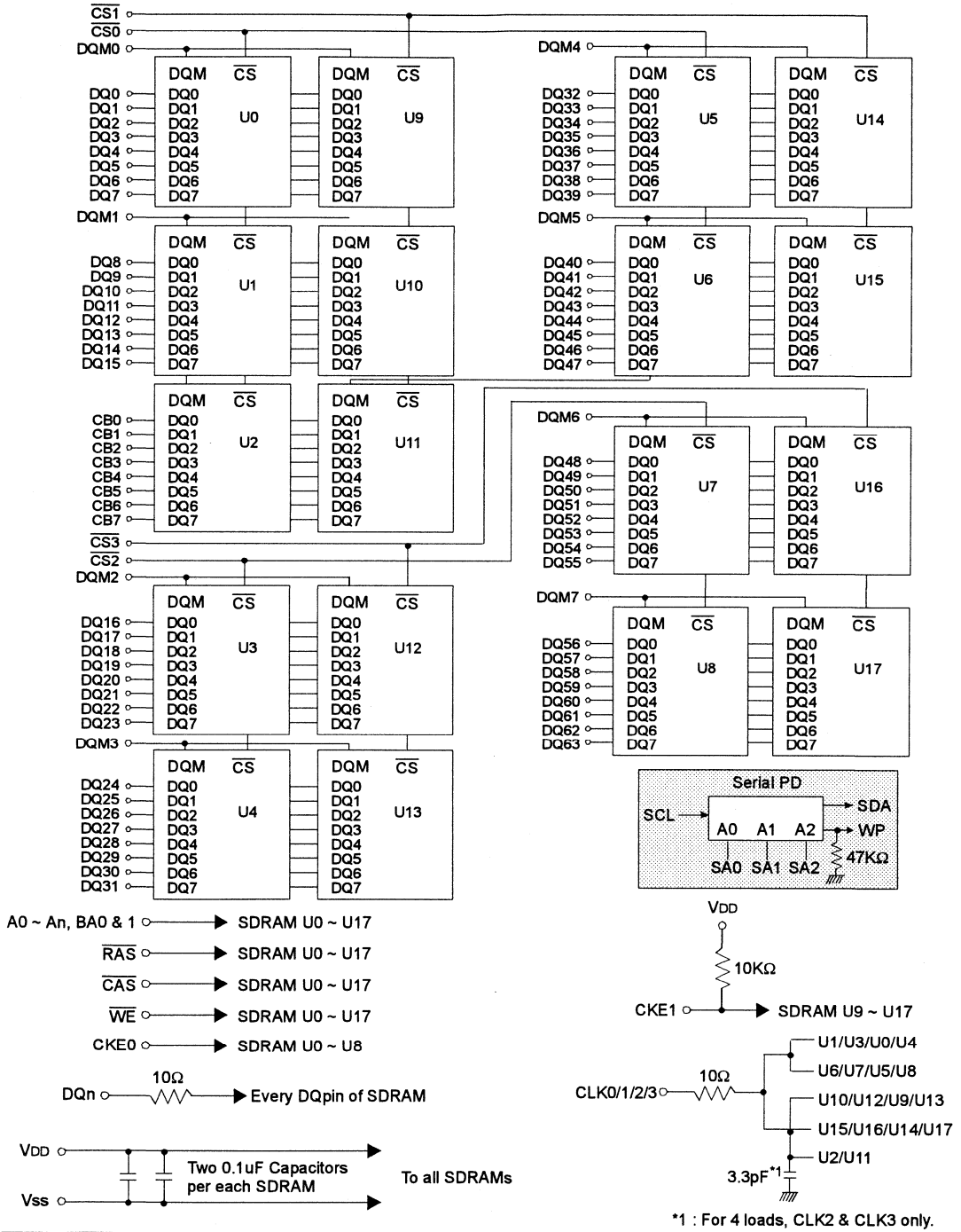
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
WP	*Write protection*	WP pin is connected to Vss through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be wirte-protected.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	18	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-18	-	18	uA	3
Input leakage current (I/O pins)	I_{IL}	-3	-	3	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C_{ADD}	65	95	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN}	65	95	pF
CKE (CKE0 ~ CKE1)	C_{CKE}	40	60	pF
Clock (CLK0 ~ CLK3)	C_{CLK}	30	40	pF
$\overline{CS}$ ($\overline{CS0}$ ~ $\overline{CS3}$)	C_{CS}	30	40	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	15	25	pF
DQ (DQ0 ~ DQ63)	C_{OUT1}	10	20	pF
CB (CB0 ~ CB7)	C_{OUT2}	10	20	pF

DC CHARACTERISTICS

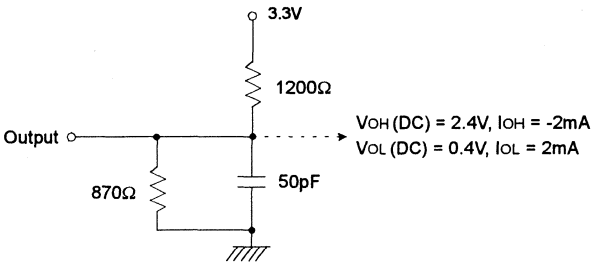
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-80	-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		855	810	810	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		18			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		18				
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		216			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		108				
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		36			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		36				
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		360			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		180			mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	1,035	855	855	mA	1
			2	855	855	810		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		2,250			mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		18			mA	

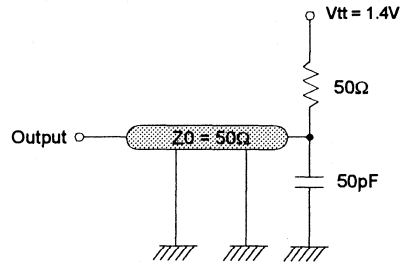
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		10		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6	ns	1,2
	CAS latency=2			6		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			6		6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A8)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A8)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes 1. OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

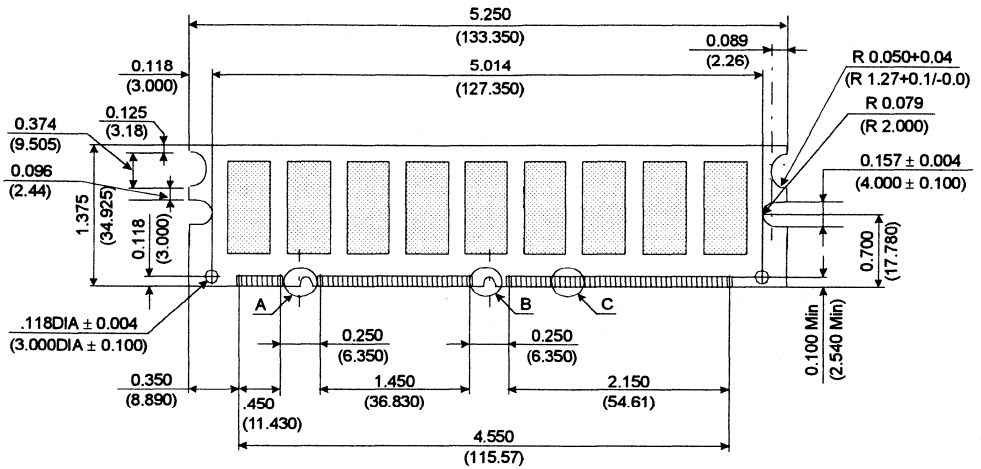
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at tRP after the end of burst.

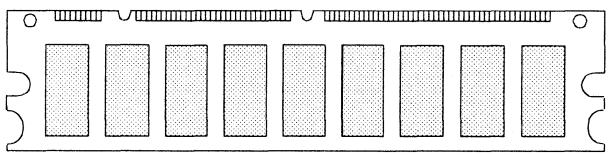
6. Burst stop command is valid at every burst length.

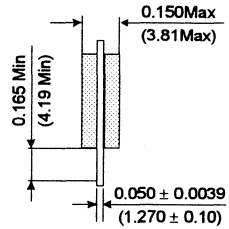
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

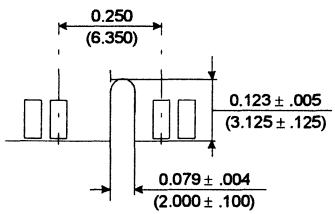
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

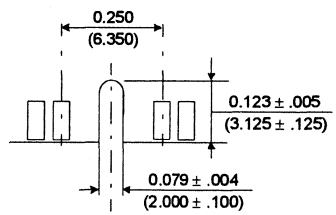




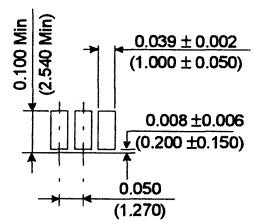




Detail A



Detail B



Detail C

Tolerances : ± .005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832C

M374S1623CT0-C80/C1H/C1L

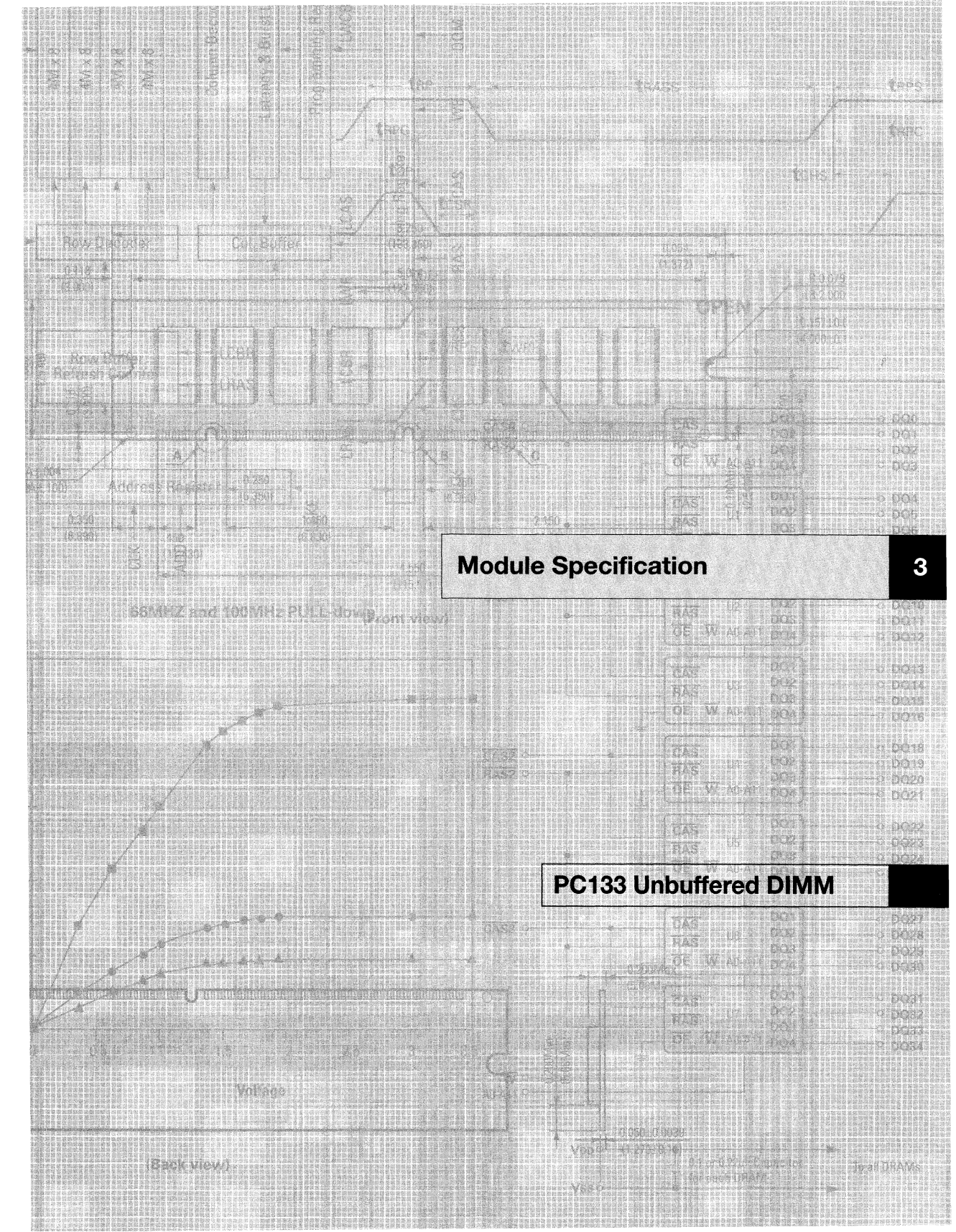
- Organization : 16Mx72
- Composition : 8Mx8 *18
- Used component part # : K4S640832C-TC80/C1H/C1L
- # of rows in module : 2 rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module rows on this assembly	2 rows			02h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module row density	2 rows of 64MB			10h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8D	-1H	-1L	-8D	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			F2h	18h	48h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	..... Manufacturer part # (Data bits)	7			37h			
77	..... Manufacturer part # (Data bits)	4			34h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	1			31h			
80	..... Manufacturer part # (Module depth)	6			36h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	C			43h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	0			30h			
86	Manufacturer part # (Hyphen)	"-"			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	0			30h			
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)			43h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			FDh	FFh	FDh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

NOTES



Module Specification

3

PC133 Unbuffered DIMM

M366S0424DTS SDRAM DIMM

4Mx64 SDRAM DIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S0424DTS is a 4M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S0424DTS consists of four CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S0424DTS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S0424DTS-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,000mil)**, Single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	NC	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	NC	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0, CLK2	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

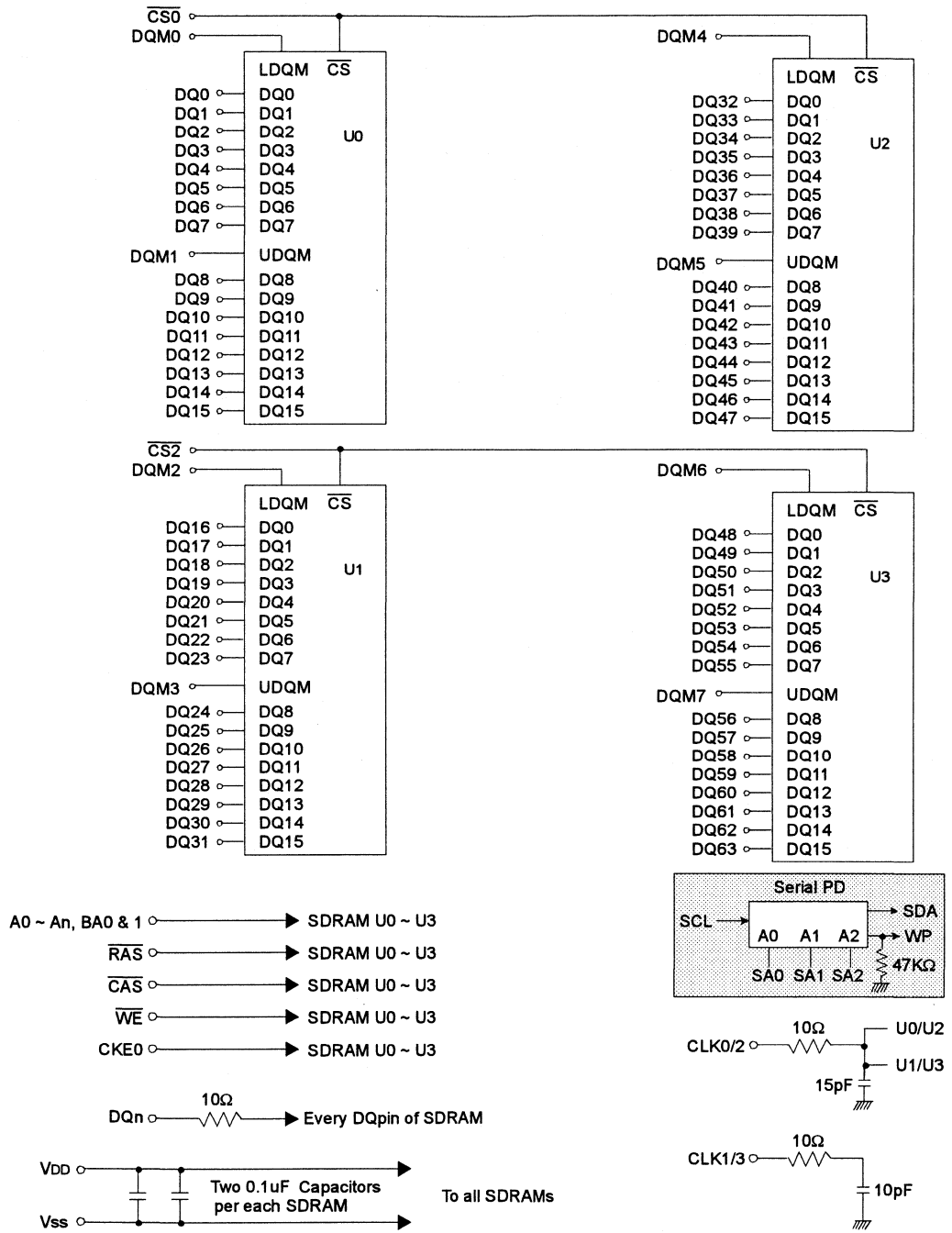
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA7
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
WP	*Write protection*	WP pin is connected to VSS through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	4	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C_{ADD}	25	30	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN}	25	30	pF
CKE (CKE0)	C_{CKE}	25	30	pF
Clock (CLK0, CLK2)	C_{CLK}	15	20	pF
$\overline{CS}$ ($\overline{CS0}$, $\overline{CS2}$)	C_{CS}	15	20	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	8	10	pF
DQ (DQ0 ~ DQ63)	C_{OUT}	8	10	pF

DC CHARACTERISTICS

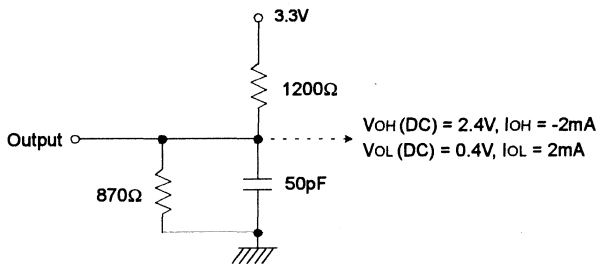
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		ey15 04
Operating current (One bank active)	I_{CC1}	Burst length =1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	440	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	4	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	4		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	60	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	24		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	12	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	12		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	100	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	60	mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs	540	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	540	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	4	mA	

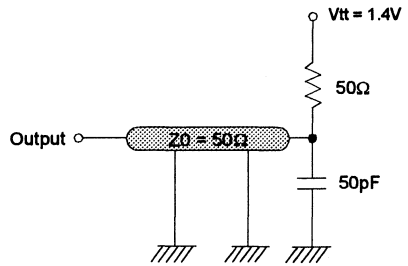
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noticed, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}).

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-75		
Row active to row active delay		tRRD(min)	15	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	ns	1
Row precharge time		tRP(min)	20	ns	1
Row active time		tRAS(min)	45	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	65	ns	1
Last data in to row precharge		tRDL(min)	2	CLK	2
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns	-	-
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	-		-		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter	Symbol	-75		Unit	Note
		Min	Max		
CLK cycle time	tCC	7.5	1000	ns	1
CLK to valid	tSAC		5.4	ns	1, 2
Output data	tOH	2.7		ns	2
CLK high pulse width	tCH	2.5		ns	3
CLK low pulse width	tCL	2.5		ns	3
Input setup time	tSS	1.5		ns	3
Input hold time	tSH	0.8		ns	3
CLK to output in Low-Z	tSLZ	1		ns	2
CLK to output	tSHZ		5.4	ns	

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A7)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A7)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

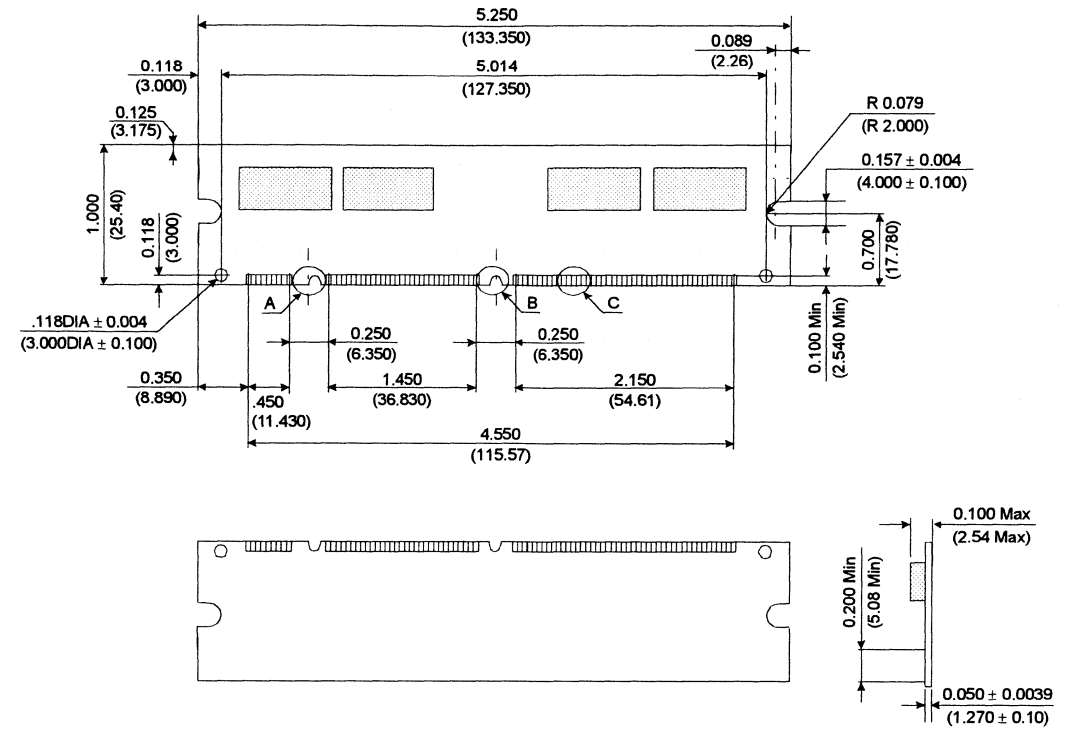
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

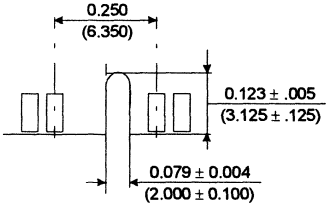
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

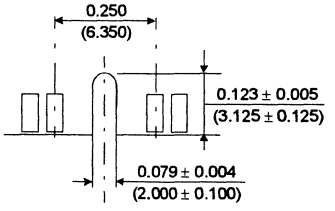
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

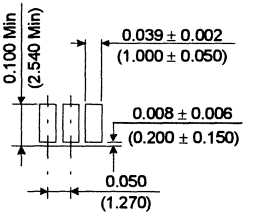




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : K4S641632D-TC75

M366S0424DTS-C75

- Organization : 4Mx64
- Composition : 4Mx16 *4
- Used component part # : K4S641632D-TC75
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,000mil height & single sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	8	08h	1
5	# of module rows on this assembly	1 row	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	
24	SDRAM access time from clock @CAS latency of 2	-	00h	
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module row density	1 row of 32MB	08h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	8Bh	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	4	34h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	D	44h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	S	53h	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	S	53h	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed 100MHz Information	ADh	6
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.
6. These values apply to PC100 application only, per Intel PC66/100 SPD standards.

M366S0823DTS SDRAM DIMM

8Mx64 SDRAM DIMM based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S0823DTS is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S0823DTS consists of eight CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S0823DTS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S0823DTS-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)**, single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0, CLK2	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

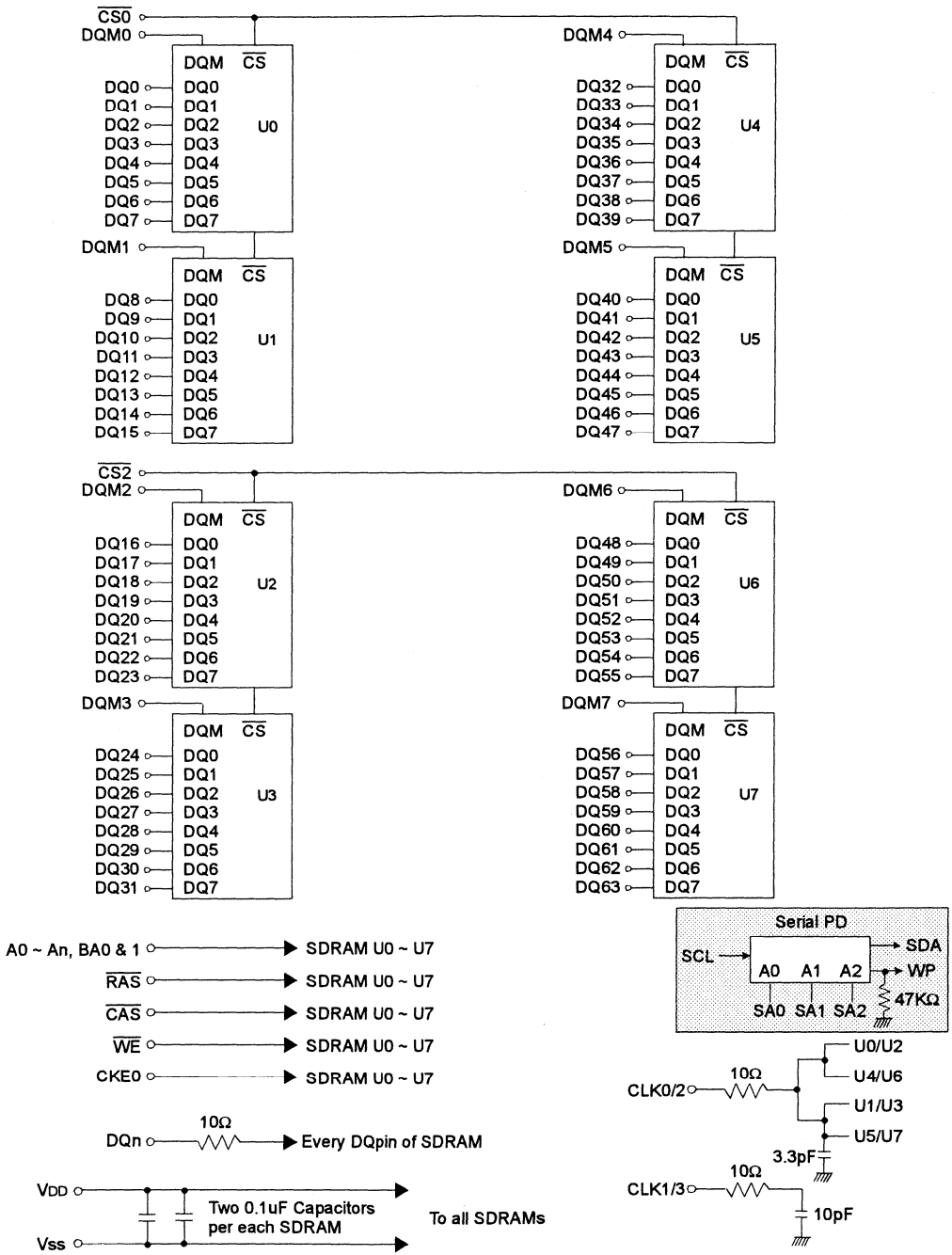
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
WP	*Write protection*	WP pin is connected to VSS through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write - protected.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high votlage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C_{ADD}	30	45	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN}	30	45	pF
CKE (CKE0)	C_{CKE}	30	45	pF
Clock (CLK0, CLK2)	C_{CLK}	22	30	pF
$\overline{CS}$ ($\overline{CS0}$, $\overline{CS2}$)	C_{CS}	15	25	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	6	8	pF
DQ (DQ0 ~ DQ63)	C_{OUT}	6	8	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note ey15 04
			-75		
Operating current (One bank active)	I_{CC1}	Burst length =1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	600	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	8	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	8		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	120	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	48		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	24	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	24		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	200	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	120	mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs	920	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	1,080	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	8	mA	

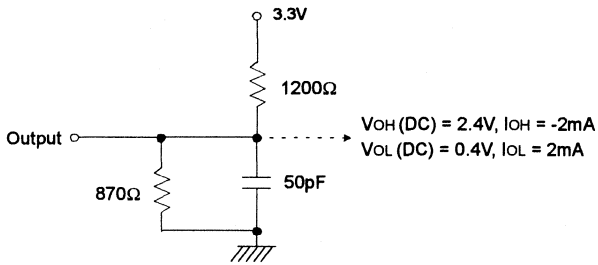
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

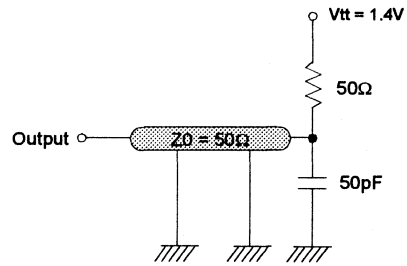
3. Unless otherwise noticed, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}).

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	tRRD(min)	15	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay	tRCD(min)	20	ns	1
Row precharge time	tRP(min)	20	ns	1
Row active time	tRAS(min)	45	ns	1
	tRAS(max)	100	us	
Row cycle time	tRC(min)	65	ns	1
Last data in to row precharge	tRDL(min)	2	CLK	2
Last data in to Active delay	tDAL(min)	2 CLK + 20 ns	-	-
Last data in to new col. address delay	tCDL(min)	1	CLK	2
Last data in to burst stop	tBDL(min)	1	CLK	2
Col. address to col. address delay	tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	-	-		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter	Symbol	-75		Unit	Note
		Min	Max		
CLK cycle time	t_{CC}	7.5	1000	ns	1
CLK to valid	t_{SAC}		5.4	ns	1,2
Output data	t_{OH}	2.7		ns	2
CLK high pulse width	t_{CH}	2.5		ns	3
CLK low pulse width	t_{CL}	2.5		ns	3
Input setup time	t_{SS}	1.5		ns	3
Input hold time	t_{SH}	0.8		ns	3
CLK to output in Low-Z	t_{SLZ}	1		ns	2
CLK to output	t_{SHZ}		5.4	ns	

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

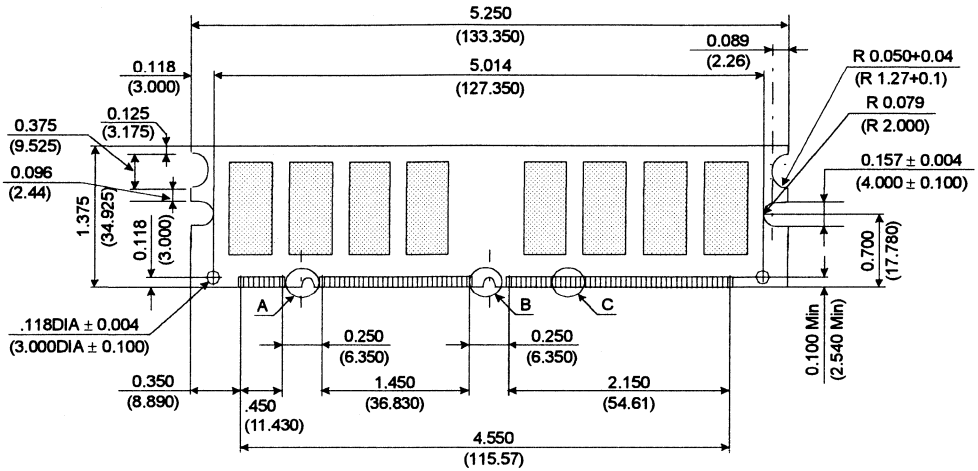
Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

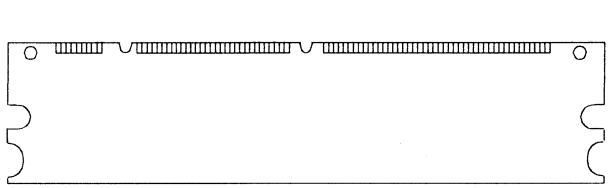
(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

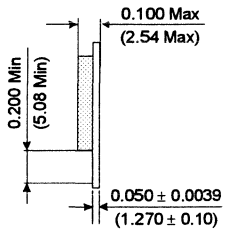
Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

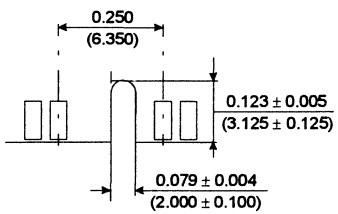
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

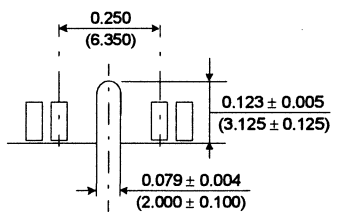




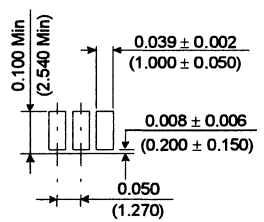




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832D-TC75

M366S0823DTS-C75

- Organization : 8Mx64
- Composition : 8Mx8 *8
- Used component part # : K4S640832D-TC75
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module rows on this assembly	1 row	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	
24	SDRAM access time from clock @CAS latency of 2	-	00h	
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module row density	1 row of 64MB	10h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	8Ch	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	8	38h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	D	44h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	S	53h	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	S	53h	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed 100MHz Information	ADh	6
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.
6. These values apply to PC100 application only, per Intel PC66/100 SPD standards.

M366S1623DT0 SDRAM DIMM

16Mx64 SDRAM DIMM based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S1623DT0 is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S1623DT0 consists of sixteen CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S1623DT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S1623DT0-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

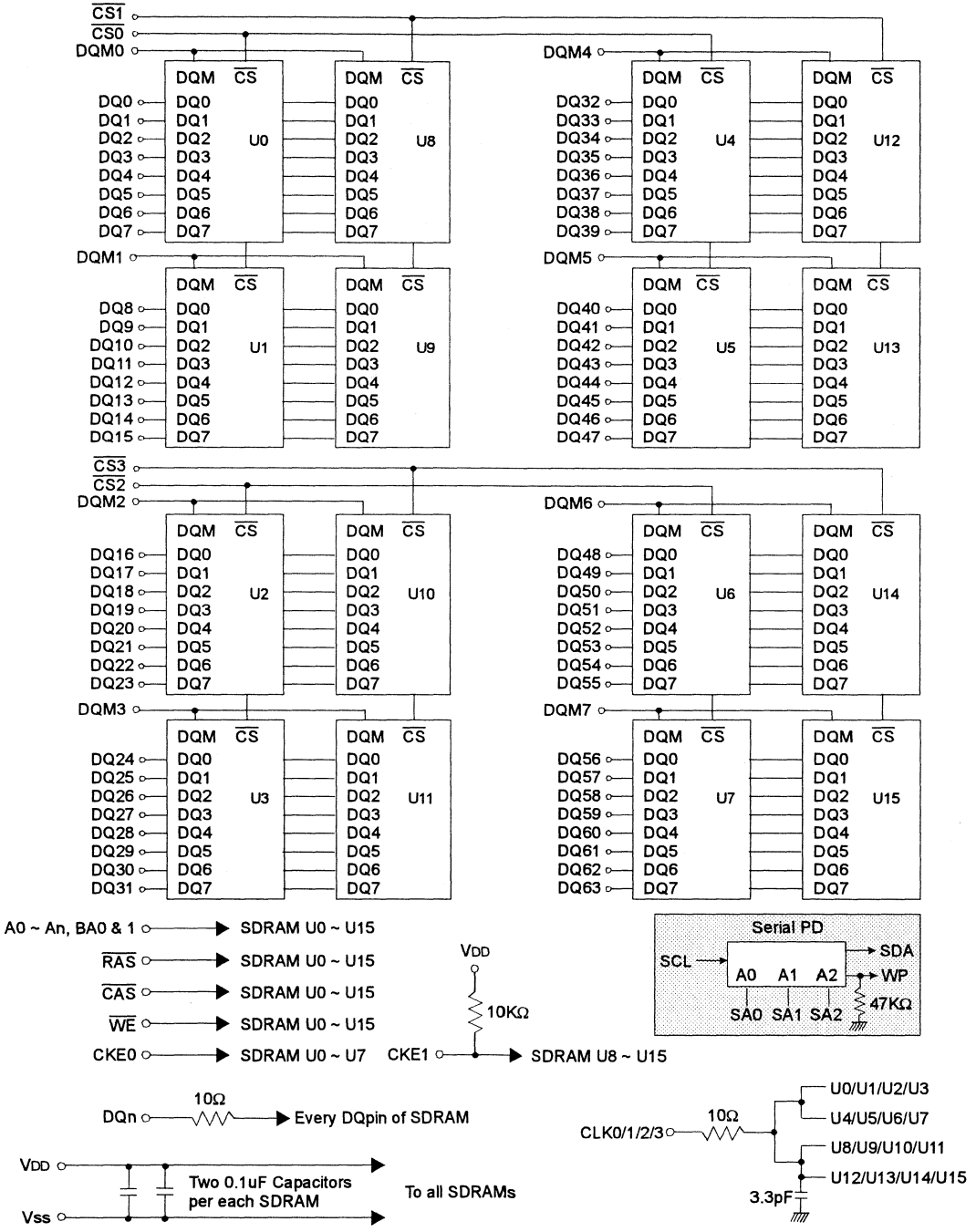
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
WP	*Write protection*	WP pin is connected to VSS through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	16	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Note : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C_{ADD}	70	95	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN}	70	95	pF
CKE (CKE0 ~ CKE1)	C_{CKE}	45	55	pF
Clock (CLK0 ~ CLK3)	C_{CLK}	35	40	pF
$\overline{CS}$ ($\overline{CS0}$, $\overline{CS2}$)	C_{CS}	25	30	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	15	20	pF
DQ (DQ0 ~ DQ63)	C_{OUT}	10	15	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (one Bank Active)	I_{CC1}	Burst length =1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	800	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	16	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	16		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	240	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	96		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	48	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	48		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	400	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	240	mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs	1,120	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	1,280	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	16	mA	

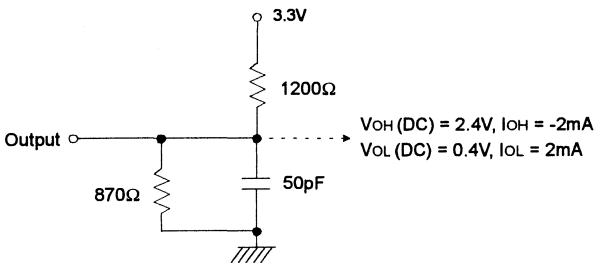
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

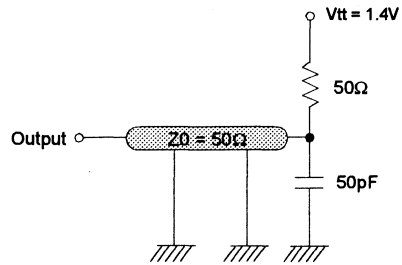
3. Unless otherwise noticed, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}).

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-75		
Row active to row active delay		tRRD(min)	15	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	ns	1
Row precharge time		tRP(min)	20	ns	1
Row active time		tRAS(min)	45	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	65	ns	1
Last data in to row precharge		tRDL(min)	2	CLK	2
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns	-	-
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	-		-		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter	Symbol	-75		Unit	Note
		Min	Max		
CLK cycle time	tCC	7.5	1000	ns	1
CLK to valid	tSAC		5.4	ns	1,2
Output data	tOH	2.7		ns	2
CLK high pulse width	tCH	2.5		ns	3
CLK low pulse width	tCL	2.5		ns	3
Input setup time	tSS	1.5		ns	3
Input hold time	tSH	0.8		ns	3
CLK to output in Low-Z	tSLZ	1		ns	2
CLK to output	tSHZ		5.4	ns	

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

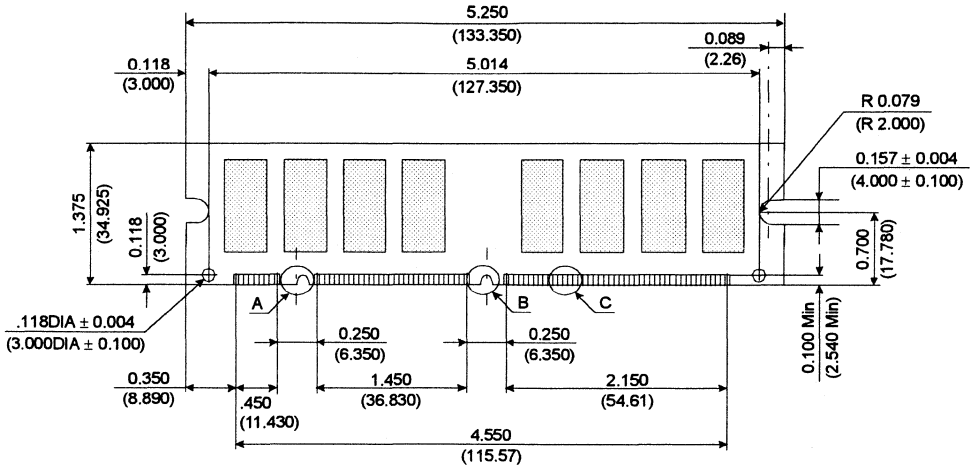
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

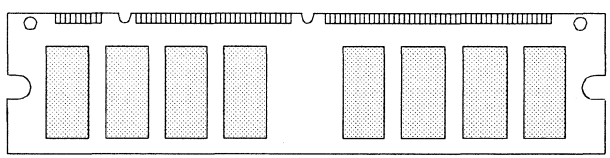
6. Burst stop command is valid at every burst length.

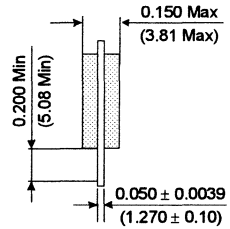
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

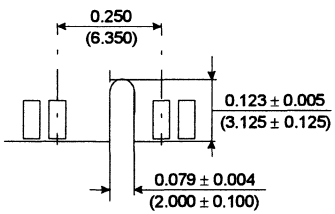
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

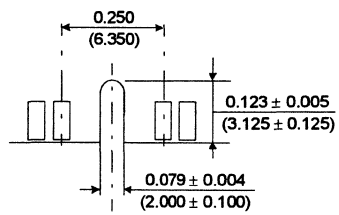




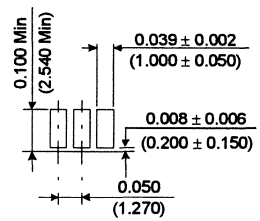




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832D-TC75

M366S1623DT0- C75

- Organization : 16Mx64
- Composition : 8Mx8 *16
- Used component part # : K4S640832D-TC75
- # of rows in module : 2 rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module rows on this assembly	2 rows	02h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	
24	SDRAM access time from clock@CAS latency of 2	-	00h	
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock@CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module row density	2 rows of 64MB	10h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	8Dh	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	..... Manufacturer part # (Module depth)	6	36h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	D	44h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	0	30h	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	0	30h	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed 100MHz Information	FDh	6
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.
6. These values apply to PC100 application only, per Intel PC66/100 SPD standards.

M374S0823DTS SDRAM DIMM

8Mx72 SDRAM DIMM with ECC based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S0823DTS is a 8M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S0823DTS consists of nine CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M374S0823DTS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S0823DTS-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)**, single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0, CLK2	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

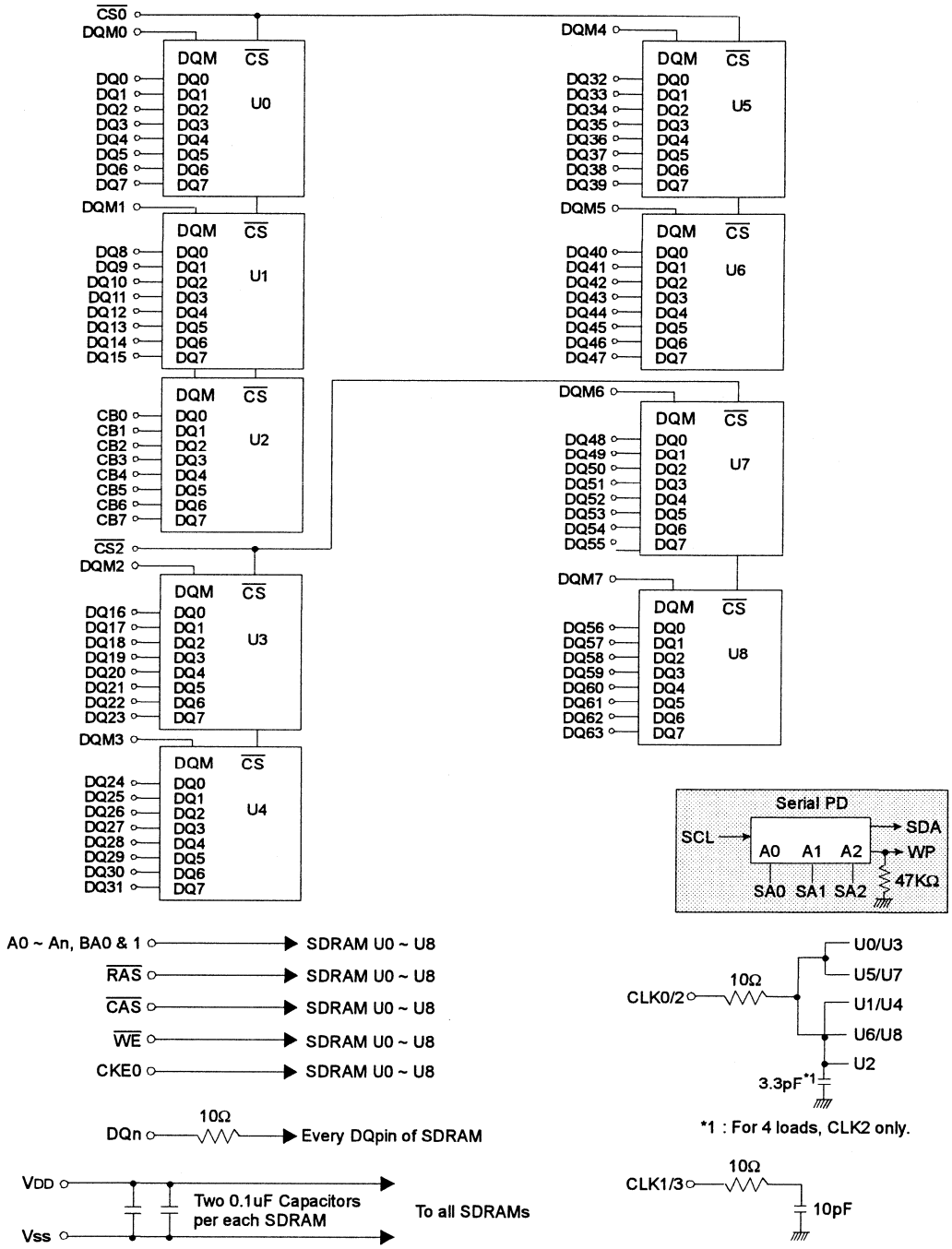
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
WP	*Write protection*	WP pin is connected to Vss through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write - protected.
VDD/Vss	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	9	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{LI}	-10	-	10	uA	3

Note : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C_{ADD}	35	60	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN}	35	60	pF
CKE (CKE0)	C_{CKE}	35	45	pF
Clock (CLK0, CLK2)	C_{CLK}	25	30	pF
$\overline{CS}$ ($\overline{CS0}$, $\overline{CS2}$)	C_{CS}	20	30	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	9	15	pF
DQ (DQ0 ~ DQ63)	C_{OUT1}	6	8	pF
CB (CB0 ~ CB7)	C_{OUT2}	6	8	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version -75	Unit	Note ey15 04
Operating current (One bank active)	I_{CC1}	Burst length =1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	675	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	9	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	9		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	135	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	54		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	27	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	27		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	225	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	135	mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs	1035	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	1,215	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	9	mA	

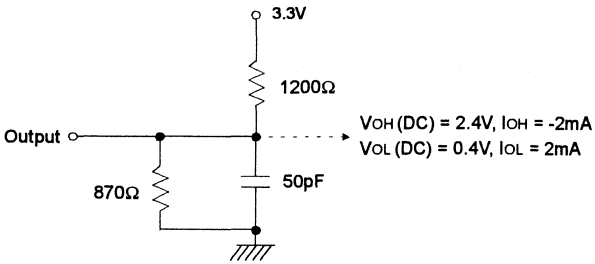
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

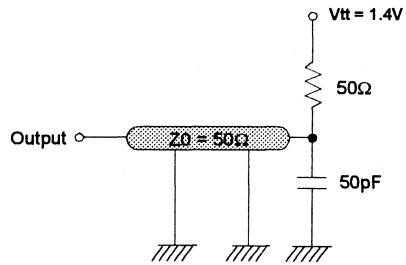
3. Unless otherwise noticed, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}).

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-75		
Row active to row active delay		tRRD(min)	15	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	ns	1
Row precharge time		tRP(min)	20	ns	1
Row active time		tRAS(min)	45	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	65	ns	1
Last data in to row precharge		tRDL(min)	2	CLK	2
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns	-	-
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	-		-		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter	Symbol	-75		Unit	Note
		Min	Max		
CLK cycle time	tCC	7.5	1000	ns	1
CLK to valid	tSAC		5.4	ns	1,2
Output data	tOH	2.7		ns	2
CLK high pulse width	tCH	2.5		ns	3
CLK low pulse width	tCL	2.5		ns	3
Input setup time	tSS	1.5		ns	3
Input hold time	tSH	0.8		ns	3
CLK to output in Low-Z	tSLZ	1		ns	2
CLK to output	tSHZ		5.4	ns	

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

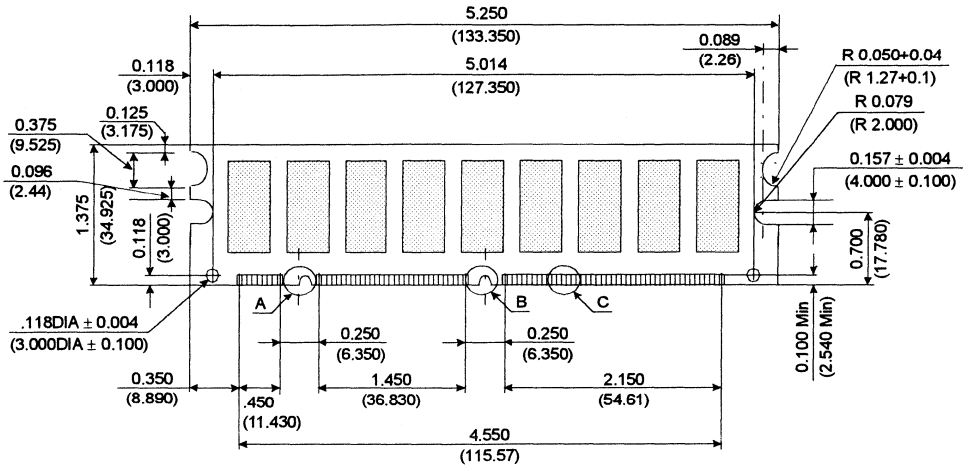
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

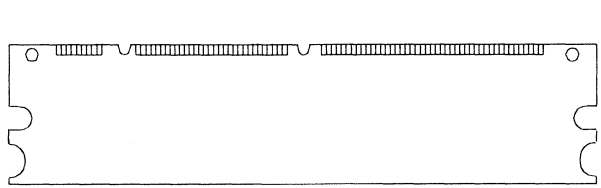
6. Burst stop command is valid at every burst length.

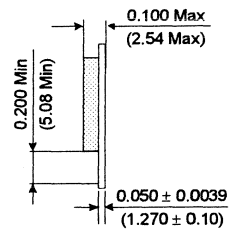
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

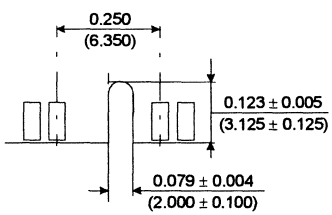
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

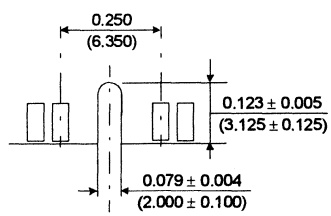




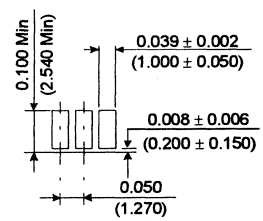




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832D-TC75

M374S0823DTS-C75

- Organization : 8Mx72
- Composition : 8Mx8 *9
- Used component part # : K4S640832D-TC75
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module rows on this assembly	1 row	01h	
6	Data width of this assembly	72 bits	48h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	x8	08h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	
24	SDRAM access time from clock @CAS latency of 2	-	00h	
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module row density	1 row of 64MB	10h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	9Eh	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	7	37h	
77	..... Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	8	38h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	D	44h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	S	53h	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	S	53h	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed 100MHz Information	ADh	6
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.
6. These values apply to PC100 application only, per Intel PC66/100 SPD standards.

M374S1623DT0 SDRAM DIMM

16Mx72 SDRAM DIMM with ECC based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S1623DT0 is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S1623DT0 consists of eighteen CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M374S1623DT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S1623DT0-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ 7	Check bit (Data-in/data-out)
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

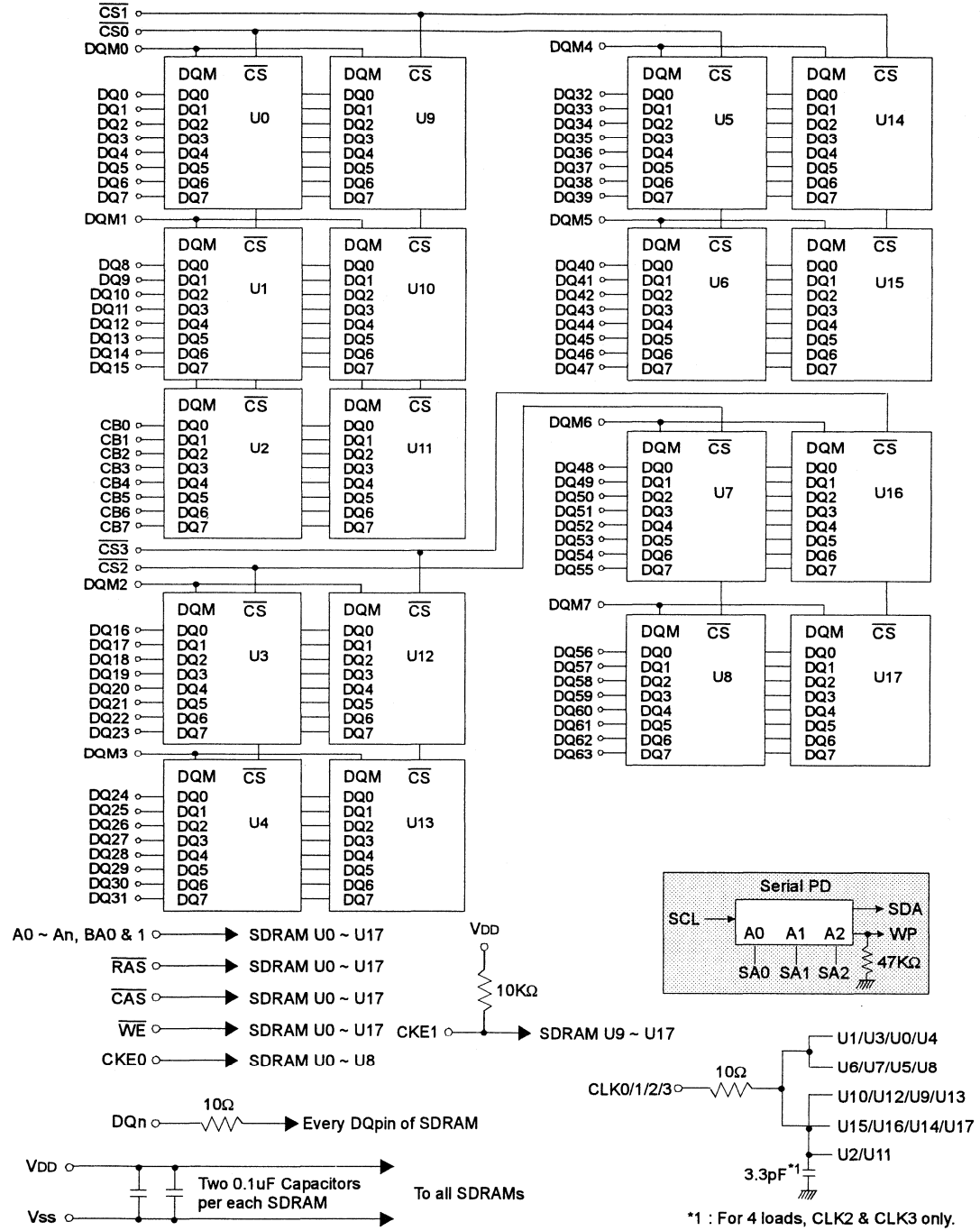
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
WP	*Write protection*	WP pin is connected to Vss through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be wirte-protected.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	18	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Note : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A12, BA0 ~ BA1)	C_{ADD}	75	100	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN}	75	100	pF
CKE (CKE0)	C_{CKE}	50	60	pF
Clock (CLK0, CLK2)	C_{CLK}	35	40	pF
$\overline{CS}$ ($\overline{CS0}$, $\overline{CS2}$)	C_{CS}	30	35	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	20	25	pF
DQ (DQ0 ~ DQ63)	C_{OUT1}	10	15	pF
CB (CB0 ~ CB7)	C_{OUT2}	10	15	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (one Bank Active)	I_{CC1}	Burst length =1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	900	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	18	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	18		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	270	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	108		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	54	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	54		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	450	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	270	mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs	1,260	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	1,440	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	18	mA	

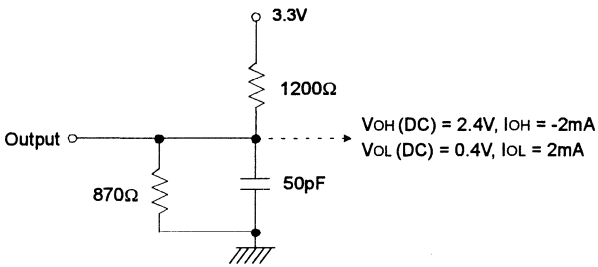
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

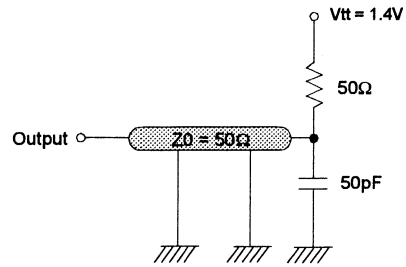
3. Unless otherwise noticed, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}).

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-75		
Row active to row active delay		tRRD(min)	15	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	ns	1
Row precharge time		tRP(min)	20	ns	1
Row active time		tRAS(min)	45	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	65	ns	1
Last data in to row precharge		tRDL(min)	2	CLK	2
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns	-	-
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	-		-		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter	Symbol	-75		Unit	Note
		Min	Max		
CLK cycle time	t_{CC}	7.5	1000	ns	1
CLK to valid output delay	t_{SAC}	-	5.4	ns	1,2
Output data hold time	t_{OH}	2.7	-	ns	2
CLK high pulse width	t_{CH}	2.5		ns	3
CLK low pulse width	t_{CL}	2.5		ns	3
Input setup time	t_{SS}	1.5		ns	3
Input hold time	t_{SH}	0.8		ns	3
CLK to output in Low-Z	t_{SLZ}	1		ns	2
CLK to output	t_{SHZ}		5.4	ns	

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

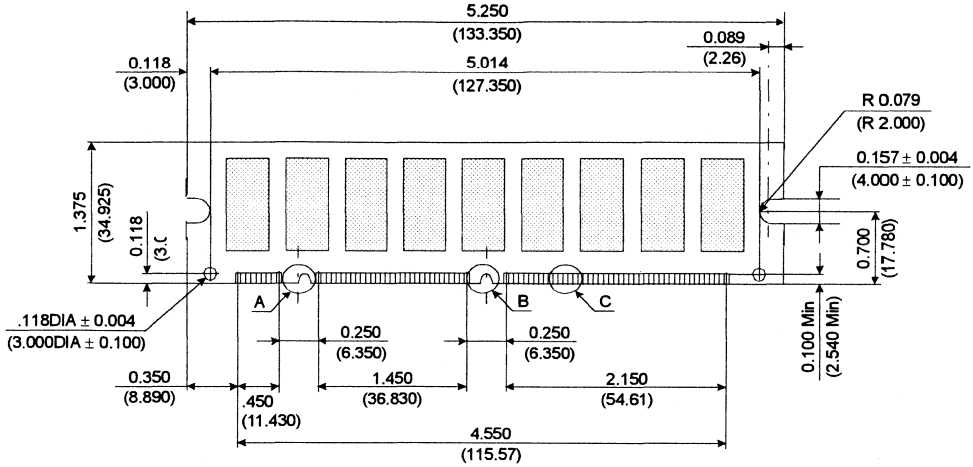
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

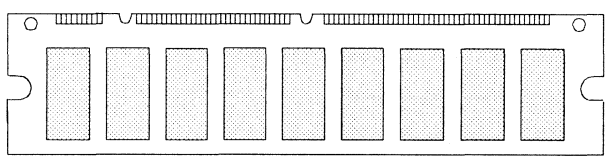
6. Burst stop command is valid at every burst length.

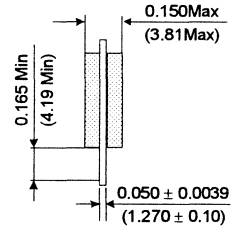
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

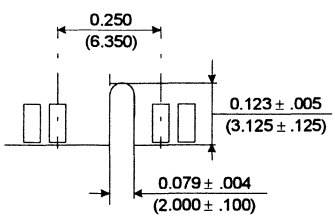
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

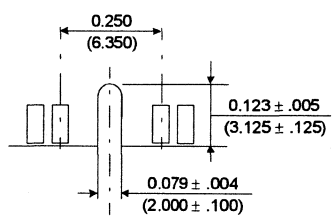




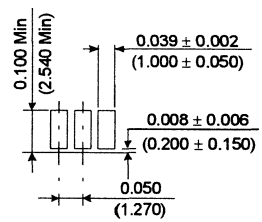




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832D-TC75

M374S1623DT0-C75

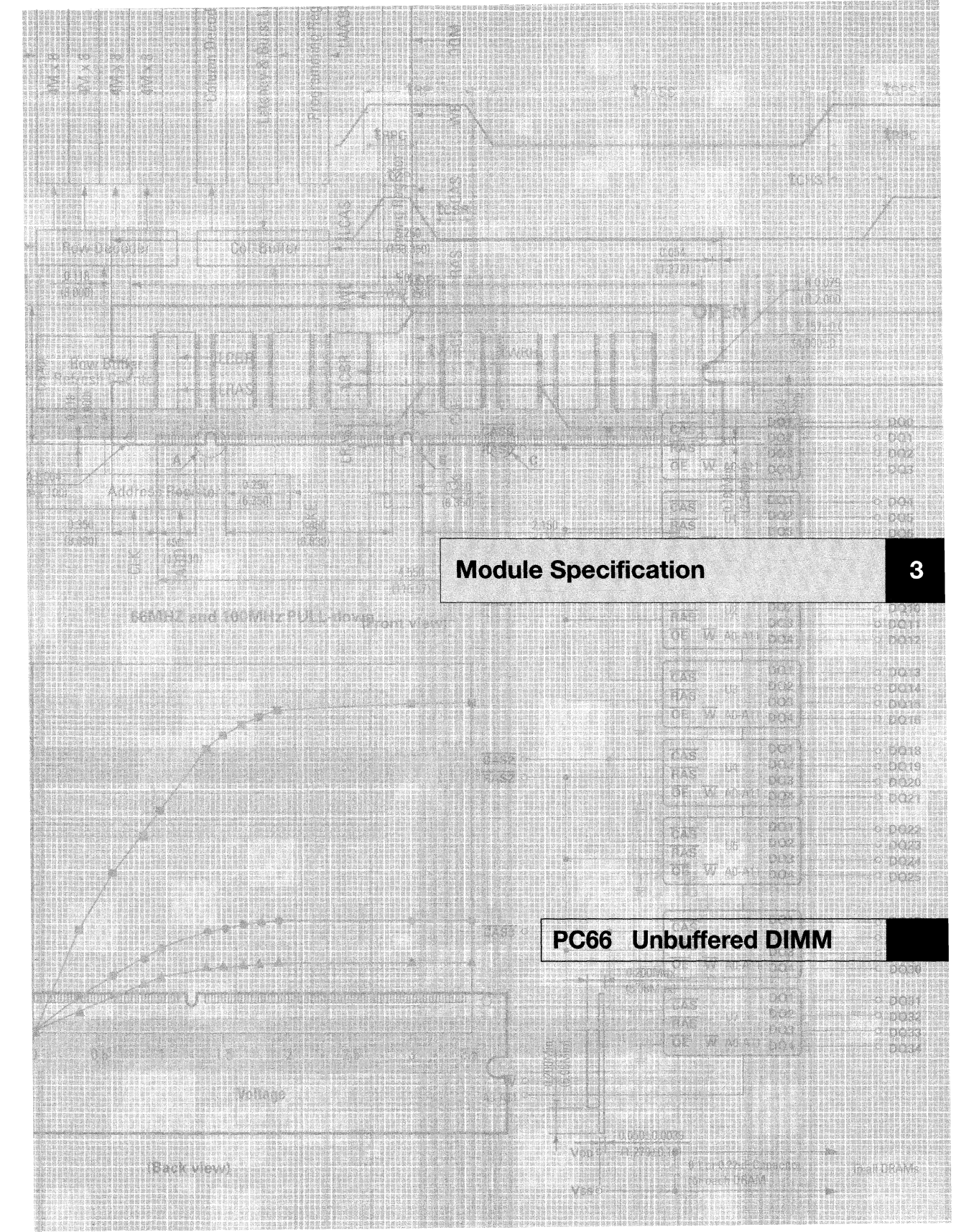
- Organization : 16Mx72
- Composition : 8Mx8 *18
- Used component part # : K4S640832D-TC75
- # of rows in module : 2 rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module rows on this assembly	2 rows	02h	
6	Data width of this assembly	72 bits	48h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	x8	08h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	
24	SDRAM access time from clock @CAS latency of 2	-	00h	
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module row density	2 rows of 64MB	10h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	9Fh	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	7	37h	
77	..... Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	..... Manufacturer part # (Module depth)	6	36h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	D	44h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	0	30h	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	0	30h	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed 100MHz Information	FDh	6
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.
6. These values apply to PC100 application only, per Intel PC66/100 SPD standards.

NOTES



Module Specification 3

PC66 Unbuffered DIMM

M366S0424DTF SDRAM DIMM

4Mx64 SDRAM DIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S0424DTF is a 4M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S0424DTF consists of four CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.33uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M366S0424DTF is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S0424DTF-C10	PC66 (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,000mil)**, single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	*CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection

* These pins are not used in this module.

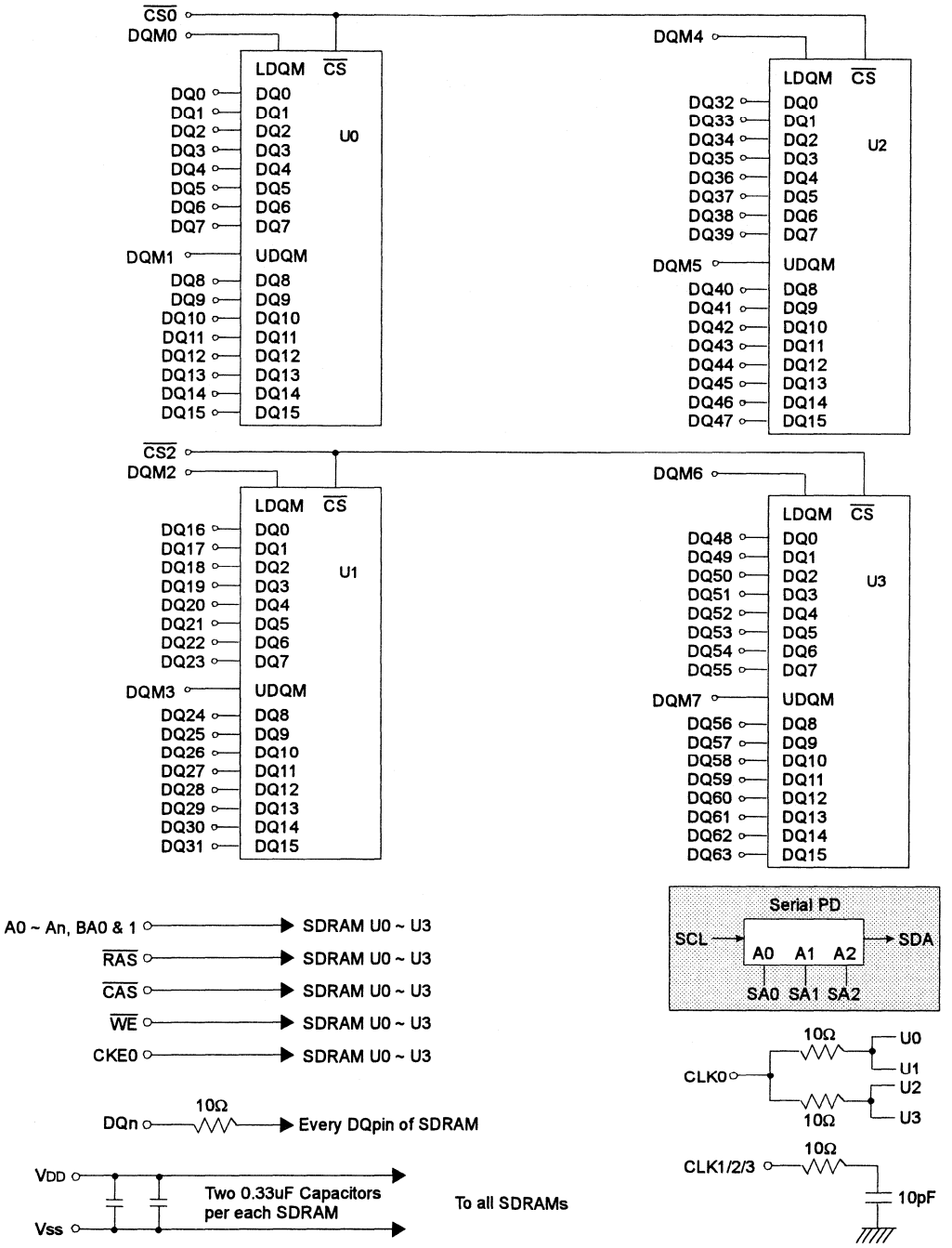
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA7
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*COlumn Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	4	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	15	25	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	15	25	pF
Input capacitance (CKE0)	C_{IN3}	15	25	pF
Input capacitance (CLK0)	C_{IN4}	10	13	pF
Input capacitance ($\overline{CS0}$)	C_{IN5}	10	15	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	8	10	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	9	12	pF

MAXIMUM TRACE LENGTHS

Signal	Max lengths	Unit	Signal	Max lengths	Unit
A0 ~ A11	8.0	Inches	CKE0	5.5	Inches
BA0 ~ BA1	8.0	Inches	$\overline{CS0}$, $\overline{CS2}$	4.0	Inches
$\overline{RAS}$	8.0	Inches	DQM0 ~ DQM7	3.0	Inches
$\overline{CAS}$	8.0	Inches	DQ0 ~ DQ63	2.0	Inches
$\overline{WE}$	8.0	Inches			

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-10		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	400	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	4	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} =∞	4		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	60	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable	24		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	12	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} =∞	12		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	100	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} =∞ Input signals are stable	60	mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs	440	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	500	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	4	mA	

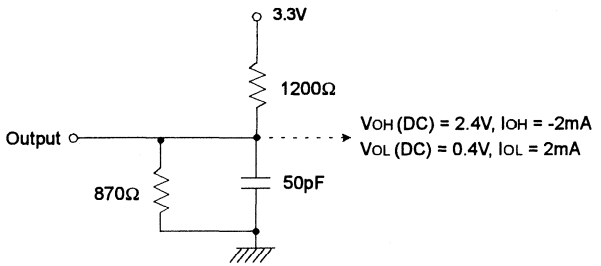
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

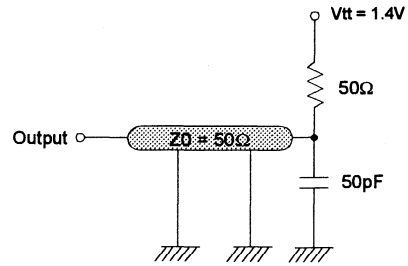
3. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
Row cycle time		tRAS(max)	100	us	
		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	2	CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20ns	-	5
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In ca1se of row precharge interrupt, auto precharge and read burst stop.
5. For -10, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	t_{SAC}		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	t_{OH}	3		ns	1,2
	CAS latency=2		3			
CLK high pulse width		t_{CH}	3.5		ns	3
CLK low pulse width		t_{CL}	3.5		ns	3
Input setup time		t_{SS}	2.5		ns	3
Input hold time		t_{SH}	1.5		ns	3
CLK to output in Low-Z		t_{SLZ}	1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		7	ns	1
	CAS latency=2			7		

Notes :1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, A_9 ~ A_0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A_0 ~ A_7)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A_0 ~ A_7)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
A_0 ~ A_{11} & BA_0 ~ BA_1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA_0 ~ BA_1 : Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

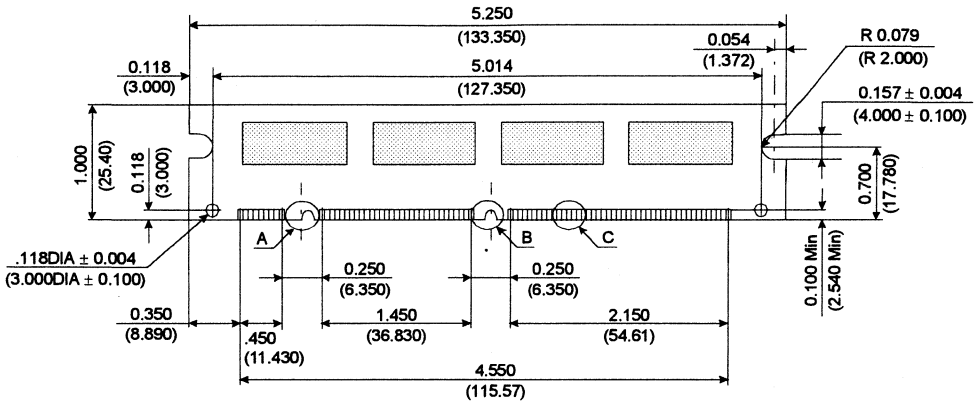
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

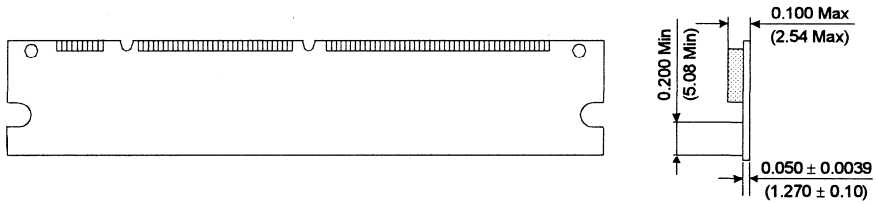
6. Burst stop command is valid at every burst length.

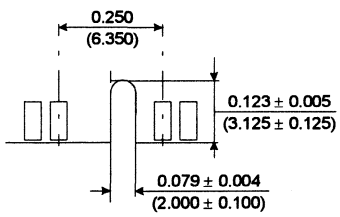
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

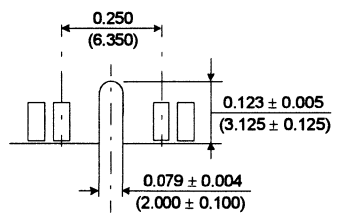
Units : Inches (Millimeters)



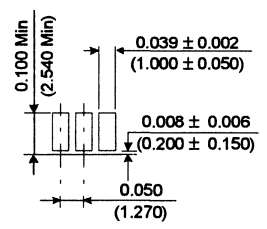




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : K4S641632D

M366S0424DTF-C10

- Organization : 4Mx64
- Composition : 4Mx16 *4
- Used component part # : K4S641632D-TC10
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,000mil height & single sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	8	08h	1
5	# of module banks on this assembly	1 bank	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	1 bank of 32MB	08h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	EBh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	4	34h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	D	44h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	F	46h	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	F	46h	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M366S0823DTF SDRAM DIMM

8Mx64 SDRAM DIMM based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S0823DTF is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S0823DTF consists of eight CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.33uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M366S0823DTF is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S0823DTF-C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,250mil)** , Single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	*CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection

* These pins are not used in this module.

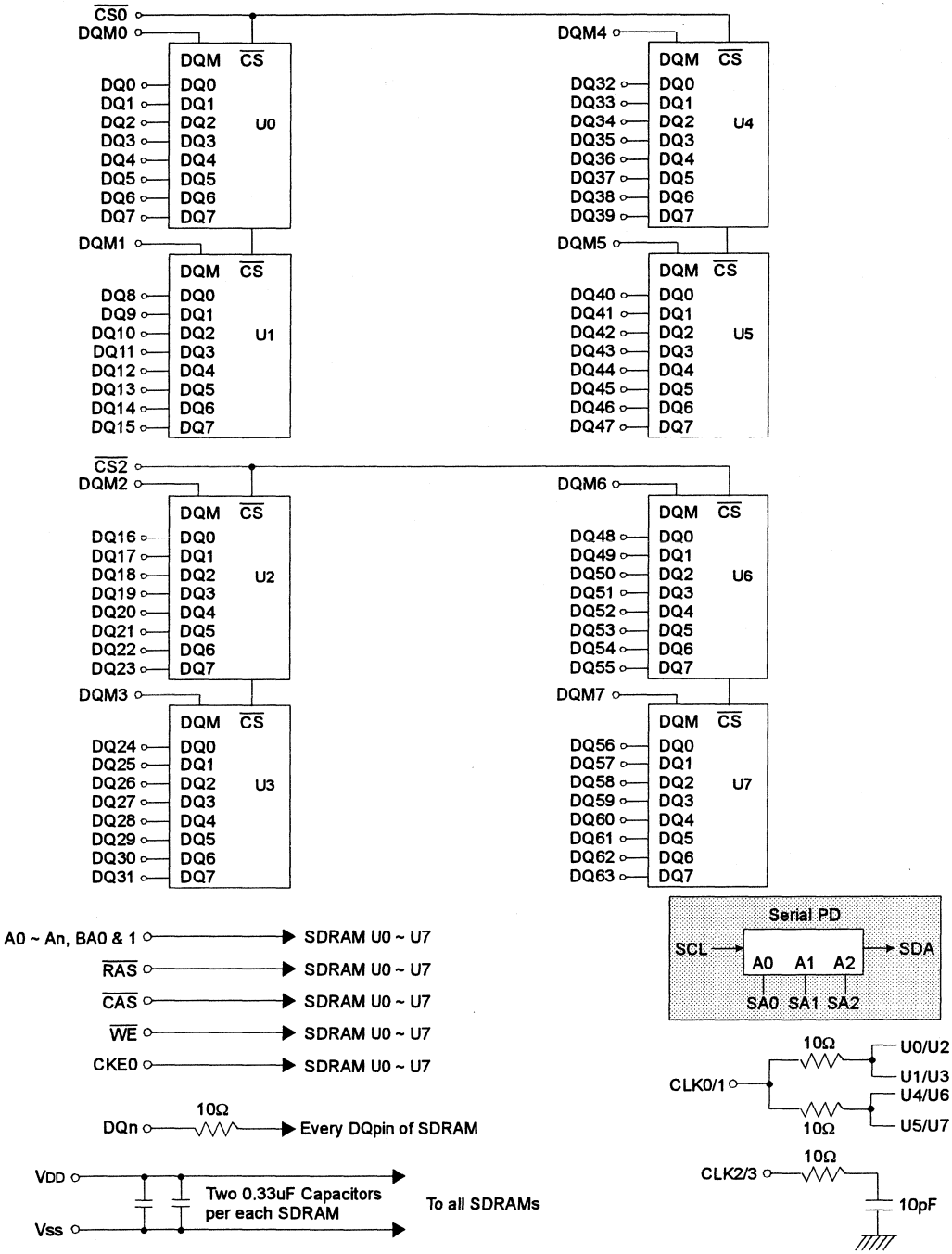
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11, BA0 ~ BA1)	C_{IN1}	25	45	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	25	45	pF
Input capacitance (CKE0)	C_{IN3}	25	45	pF
Input capacitance (CLK0, CLK1)	C_{IN4}	15	21	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	15	25	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	8	12	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	9	12	pF

MAXIMUM TRACE LENGTHS

Signal	Max lengths	Unit	Signal	Max lengths	Unit
A0 ~ A11	8.0	Inches	CKE0	5.5	Inches
BA0 ~ BA1	8.0	Inches	$\overline{CS0}$, $\overline{CS2}$	4.0	Inches
$\overline{RAS}$	8.0	Inches	DQM0 ~ DQM7	3.0	Inches
$\overline{CAS}$	8.0	Inches	DQ0 ~ DQ63	2.0	Inches
$\overline{WE}$	8.0	Inches			

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-10		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	560	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	8	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	8		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	120	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	48		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	24	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	24		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	200	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	120	mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs	760	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	1,000	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	8	mA	

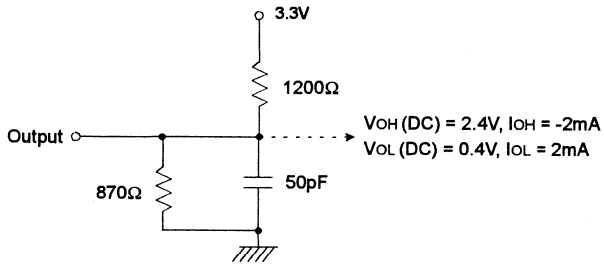
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

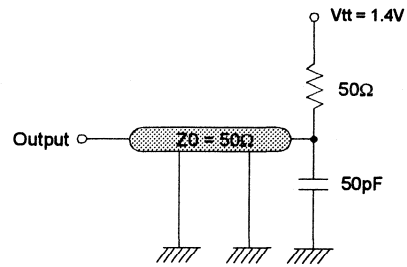
3. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	2	CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns	-	5
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -10, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tSAC		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	tOH	3		ns	1,2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tSS	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	1
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enabie										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

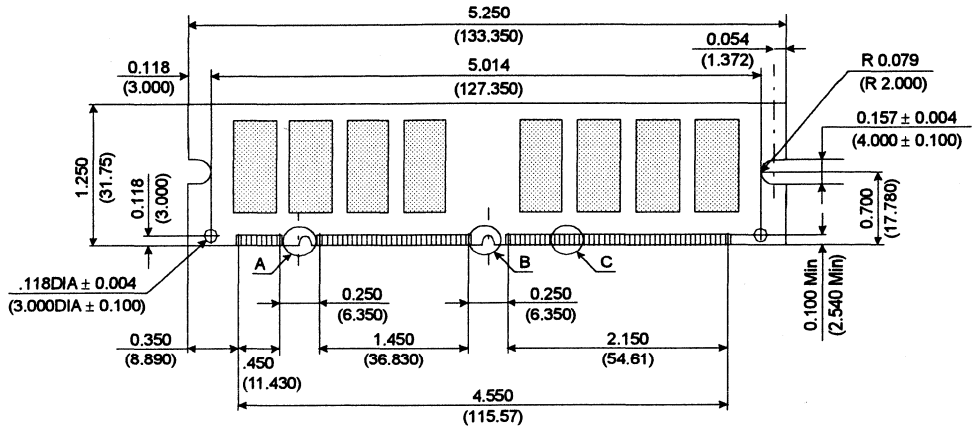
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

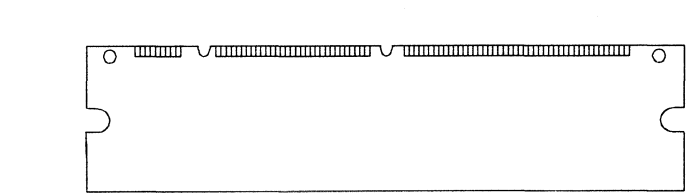
6. Burst stop command is valid at every burst length.

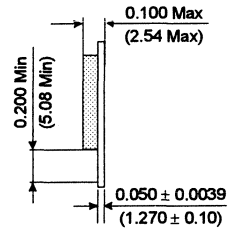
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

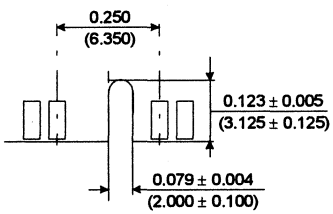
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

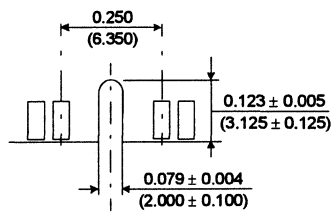




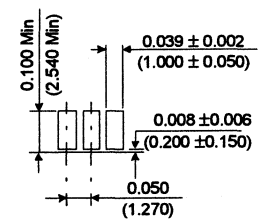




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832D

M366S0823DTF-C10

- Organization : 8Mx64
- Composition : 8Mx8 *8
- Used component part # : K4S640832D-TC10
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module banks on this assembly	1 bank	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	1 bank of 64MB	10h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	ECh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	8	38h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	D	44h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	F	46h	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	F	46h	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M366S0824DTL SDRAM DIMM

8Mx64 SDRAM DIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S0824DTL is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S0824DTL consists of eight CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.33uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M366S0824DTL is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S0824DTL-C10	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,000mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	*CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0 ~ CKE1	Clock enable input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection

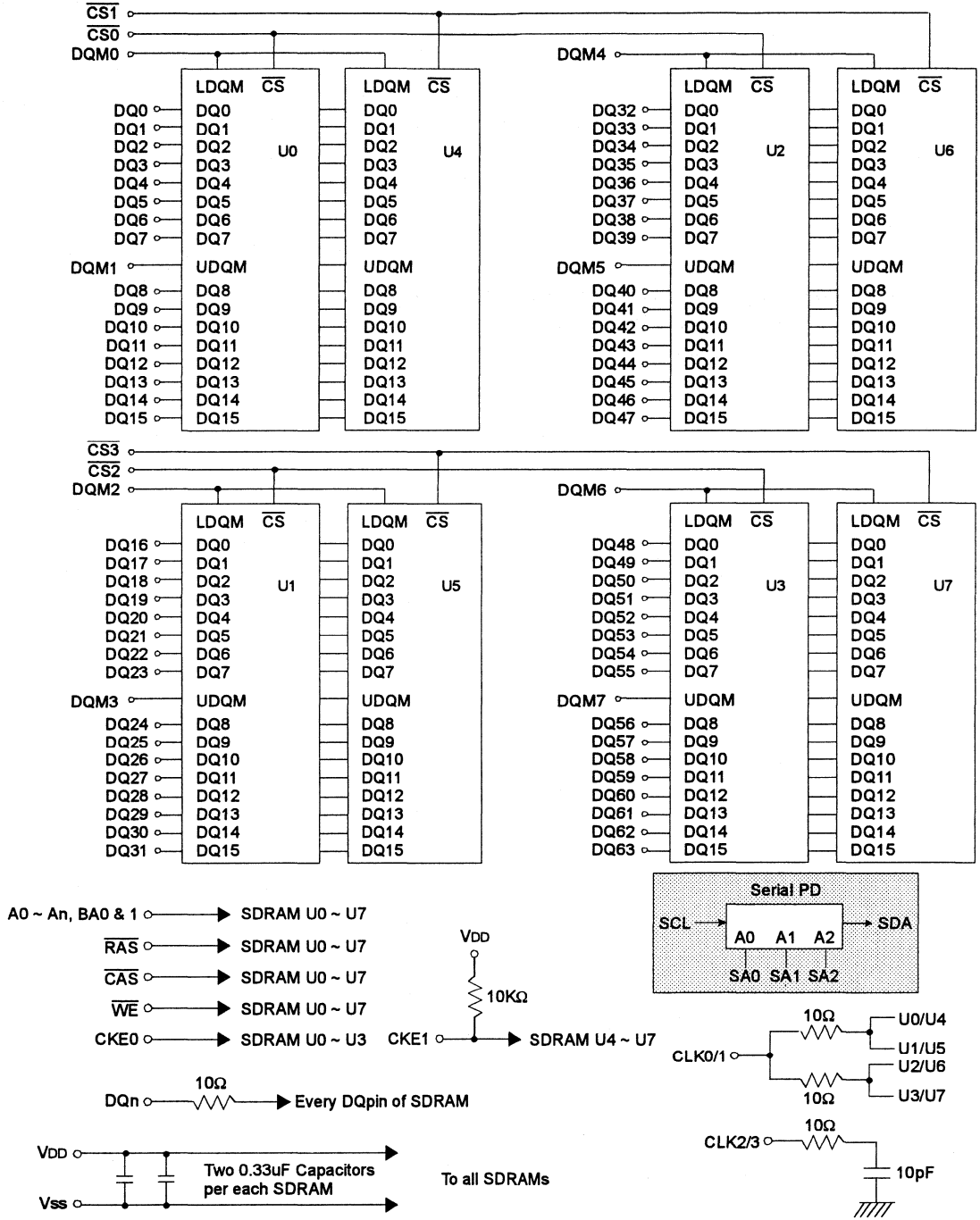
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA7
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*COlumn Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11, BA0 ~ BA1)	C_{IN1}	25	45	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	25	45	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	15	25	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	10	13	pF
Input capacitance ($\overline{CS0}$ ~ $\overline{CS3}$)	C_{IN5}	10.	15	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	8	10	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	9	12	pF

MAXIMUM TRACE LENGTHS

Signal	Max lengths	Unit	Signal	Max lengths	Unit
A0 ~ A11	8.0	Inches	CKE0 ~ CKE1	5.5	Inches
BA0 ~ BA1	8.0	Inches	$\overline{CS0}$ ~ $\overline{CS3}$	4.0	Inches
$\overline{RAS}$	8.0	Inches	DQM0 ~ DQM7	3.0	Inches
$\overline{CAS}$	8.0	Inches	DQ0 ~ DQ63	2.0	Inches
$\overline{WE}$	8.0	Inches			

DC CHARACTERISTICS

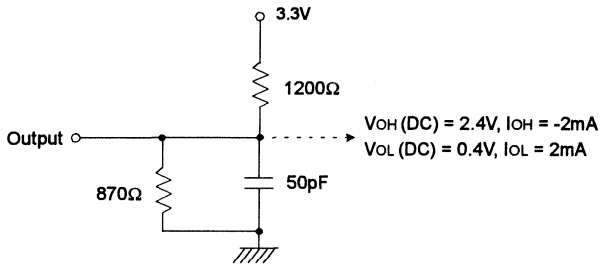
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-10		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	500	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	8	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	8		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	120	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	48		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	24	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	24		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	200	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	120	mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs	540	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	600	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	8	mA	

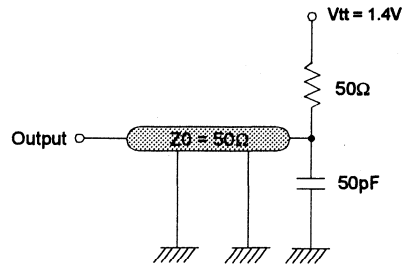
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	2	CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns	-	5
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -10, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	t_{SAC}		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	t_{OH}	3		ns	1,2
	CAS latency=2		3			
CLK high pulse width		t_{CH}	3.5		ns	3
CLK low pulse width		t_{CL}	3.5		ns	3
Input setup time		t_{SS}	2.5		ns	3
Input hold time		t_{SH}	1.5		ns	3
CLK to output in Low-Z		t_{SLZ}	1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		7	ns	1
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

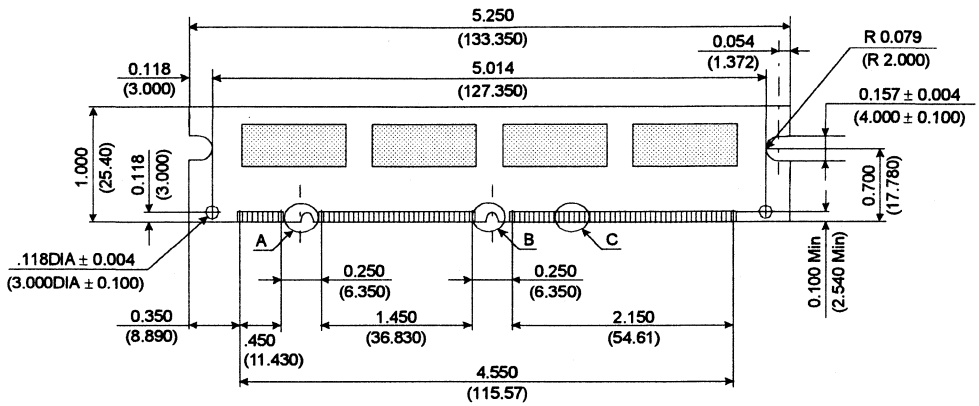
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

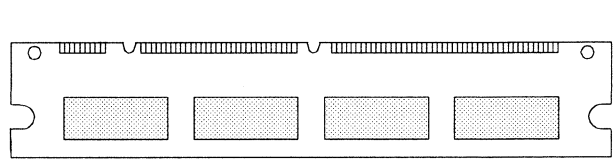
6. Burst stop command is valid at every burst length.

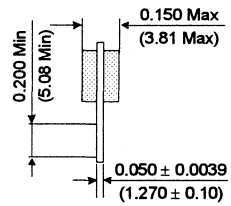
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

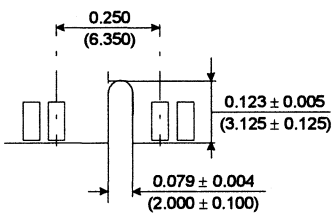
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

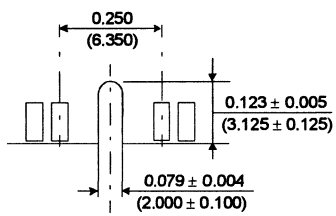




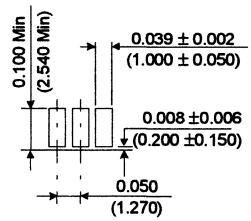




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : K4S641632D

M366S0824DTL-C10

- Organization : 8Mx64
- Composition : 4Mx16 *8
- Used component part # : K4S641632D-TC10
- # of banks in module : 2 banks
- # of banks in component : 4 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	8	08h	1
5	# of module banks on this assembly	2 banks	02h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	2 banks of 32MB	08h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	ECh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	8	38h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	D	44h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	L	4Ch	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	L	4Ch	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M366S1623DTL SDRAM DIMM

16Mx64 SDRAM DIMM based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S1623DTL is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S1623DTL consists of sixteen CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.33uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M366S1623DTL is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

• Performance range

Part No.	Max Freq. (Speed)
M366S1623DTL-C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,250mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection

* These pins are not used in this module.

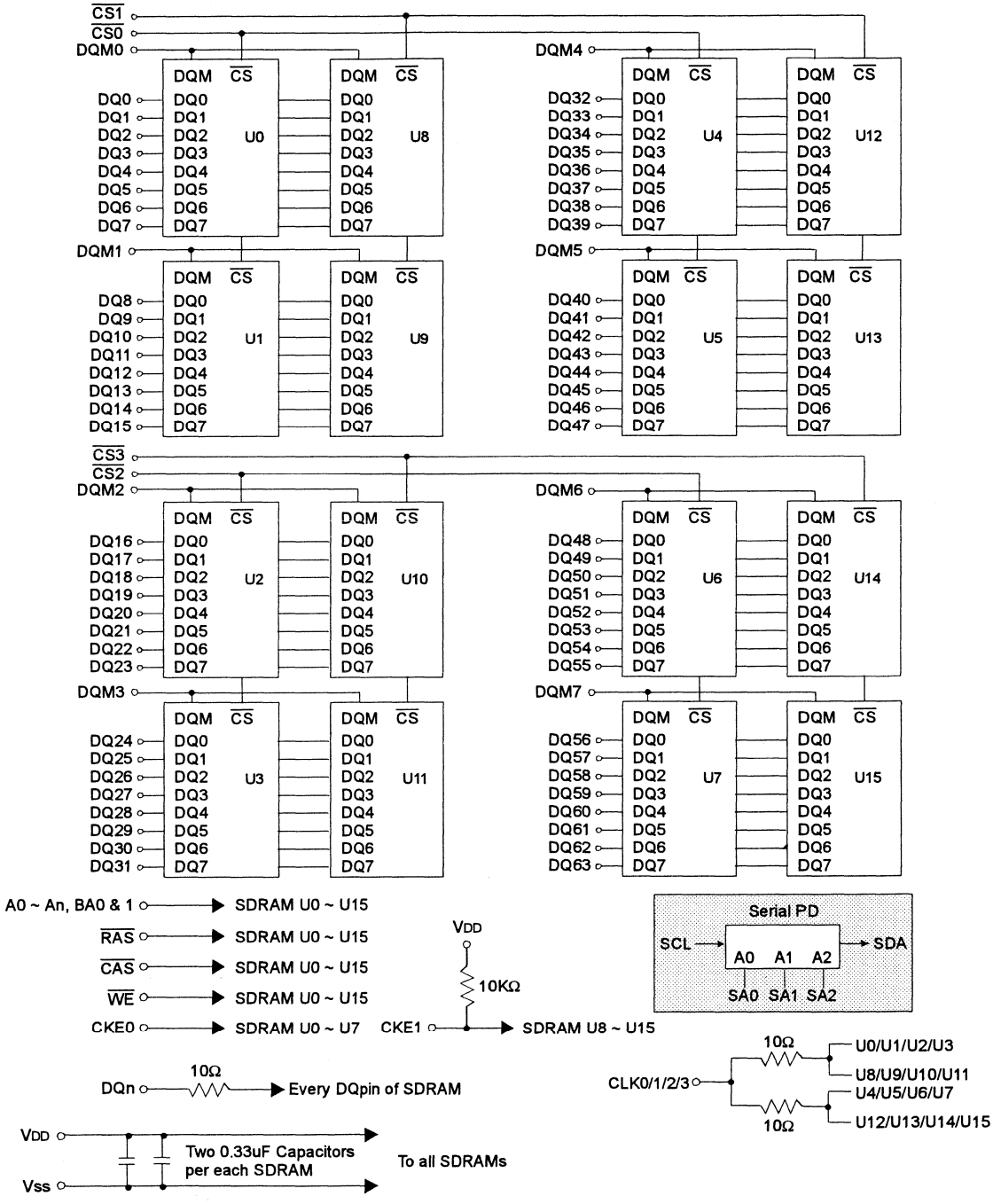
** These pins should be NC in the system which does not support SPD.

SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*COlumn Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	16	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include HI-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11, BA0 ~ BA1)	C_{IN1}	45	85	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	45	85	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	25	45	pF
Input capacitance (CLK0 ~ CLK3)	C_{IN4}	15	21	pF
Input capacitance ($\overline{CS0}$ ~ $\overline{CS3}$)	C_{IN5}	15	25	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	10	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	13	18	pF

MAXIMUM TRACE LENGTHS

Signal	Max lengths	Unit	Signal	Max lengths	Unit
A0 ~ A11	8.0	Inches	CKE0 ~ CKE1	5.5	Inches
BA0 ~ BA1	8.0	Inches	$\overline{CS0}$ ~ $\overline{CS3}$	4.0	Inches
$\overline{RAS}$	8.0	Inches	DQM0 ~ DQM7	3.0	Inches
$\overline{CAS}$	8.0	Inches	DQ0 ~ DQ63	2.0	Inches
$\overline{WE}$	8.0	Inches			

DC CHARACTERISTICS

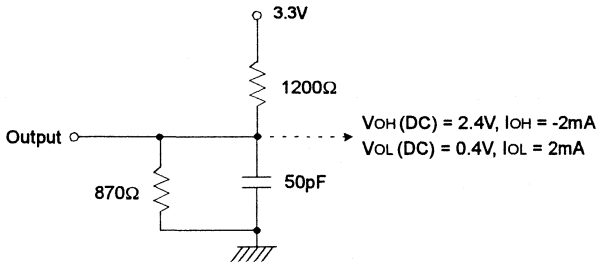
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-10		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	760	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	16	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	16		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	240	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	96		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	48	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	48		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	400	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	240	mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs	960	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	1,200	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	16	mA	

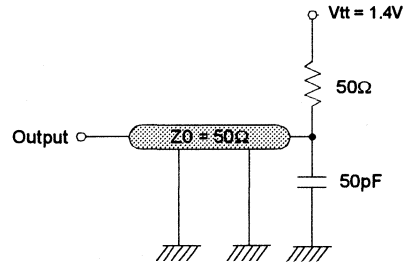
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	2	CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns	-	5
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -10, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tSAC		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	tOH	3		ns	1,2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tSS	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	1
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X	X			
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

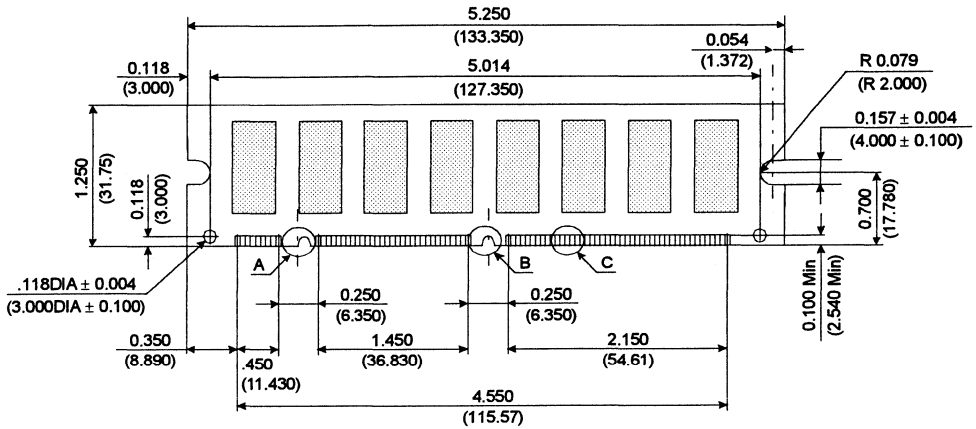
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

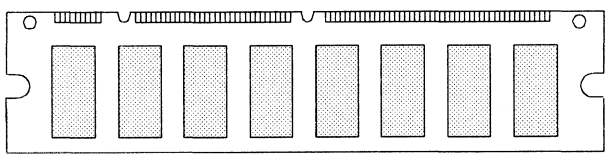
6. Burst stop command is valid at every burst length.

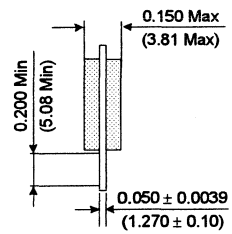
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

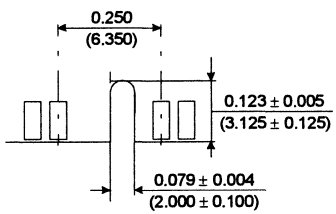
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

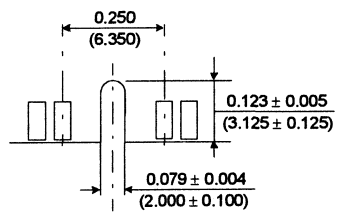




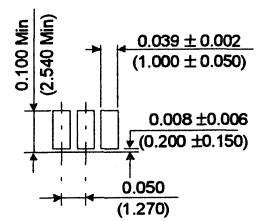




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832D

M366S1623DTL-C10

- Organization : 16Mx64
- Composition : 8Mx8 *16
- Used component part # : K4S640832D-TC10
- # of banks in module : 2 banks
- # of banks in component : 4 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module banks on this assembly	2 banks	02h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	2 banks of 64MB	10h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	EDh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	..... Manufacturer part # (Module depth)	6	36h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	D	44h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	L	4Ch	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	L	4Ch	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M374S0823DTF SDRAM DIMM

8Mx72 SDRAM DIMM with ECC based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S0823DTF is a 8M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S0823DTF consists of nine CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.33uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M374S0823DTF is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S0823DTF-C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,250mil)** , Single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	*CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0 ~ CLK1	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection

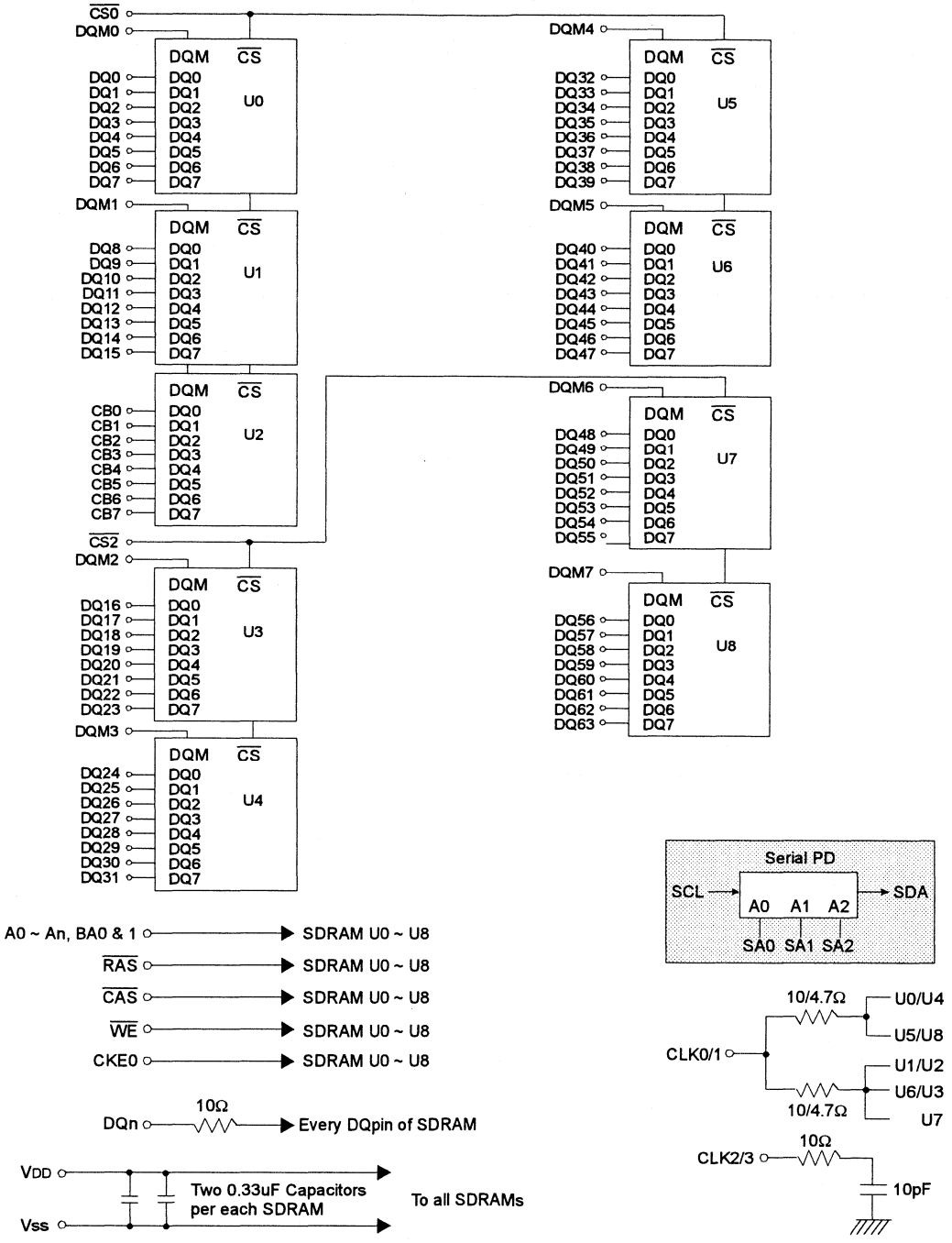
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	9	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11, BA0 ~ BA1)	C_{IN1}	28	50	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	28	50	pF
Input capacitance (CKE0)	C_{IN3}	28	50	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	18	25	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	18	30	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	8	10	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT1}	9	12	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT2}	9	12	pF

MAXIMUM TRACE LENGTHS

Signal	Max lengths	Unit	Signal	Max lengths	Unit
A0 ~ A11	9.0	Inches	CKE0	6.0	Inches
BA0 ~ BA1	9.0	Inches	$\overline{CS0}$, $\overline{CS2}$	4.0	Inches
$\overline{RAS}$	9.0	Inches	DQM0 ~ DQM7	3.0	Inches
$\overline{CAS}$	9.0	Inches	DQ0 ~ DQ63	2.0	Inches
$\overline{WE}$	9.0	Inches	CB0 ~CB7	2.0	Inches

DC CHARACTERISTICS

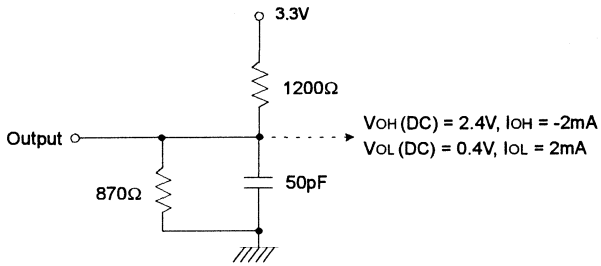
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version -10	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	630	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	9	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	9		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	135	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	54		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	27	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	27		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	225	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	135	mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs	855	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	1,125	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	9	mA	

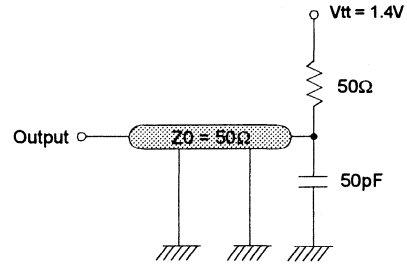
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	2	CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns	-	5
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -10, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	t_{SAC}		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	t_{OH}	3		ns	1,2
	CAS latency=2		3			
CLK high pulse width		t_{CH}	3.5		ns	3
CLK low pulse width		t_{CL}	3.5		ns	3
Input setup time		t_{SS}	2.5		ns	3
Input hold time		t_{SH}	1.5		ns	3
CLK to output in Low-Z		t_{SLZ}	1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		7	ns	1
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row Address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

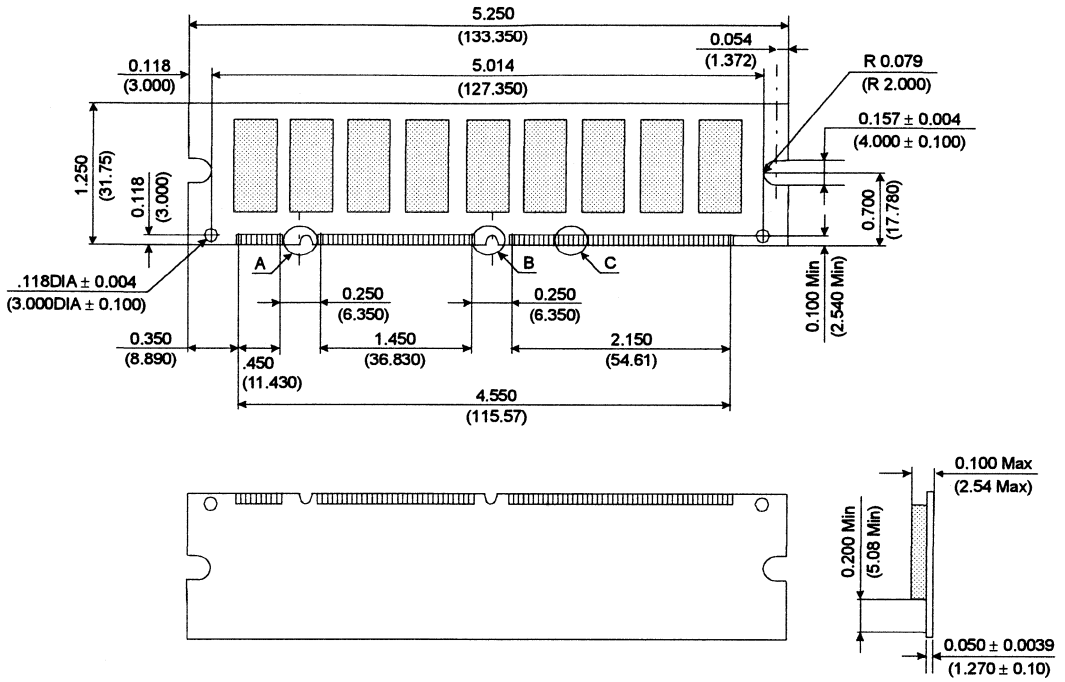
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

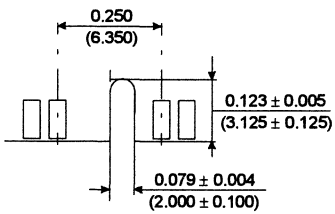
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

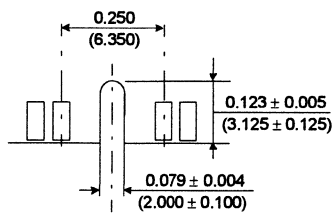
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

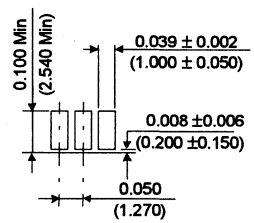




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832D

M374S0823DTF-C10

- Organization : 8Mx72
- Composition : 8Mx8 *9
- Used component part # : K4S640832D-TC10
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module banks on this assembly	1 bank	01h	
6	Data width of this assembly	72 bits	48h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	x8	08h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	1 bank of 64MB	10h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	FEh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	7	37h	
77	..... Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	8	38h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	D	44h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	F	46h	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	F	46h	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M374S1623DTL SDRAM DIMM

16Mx72 SDRAM DIMM with ECC based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S1623DTL is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S1623DTL consists of eighteen CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.33uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M374S1623DTL is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S1623DTL-C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,250mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ 7	Check bit (Data-in/data-out)
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection

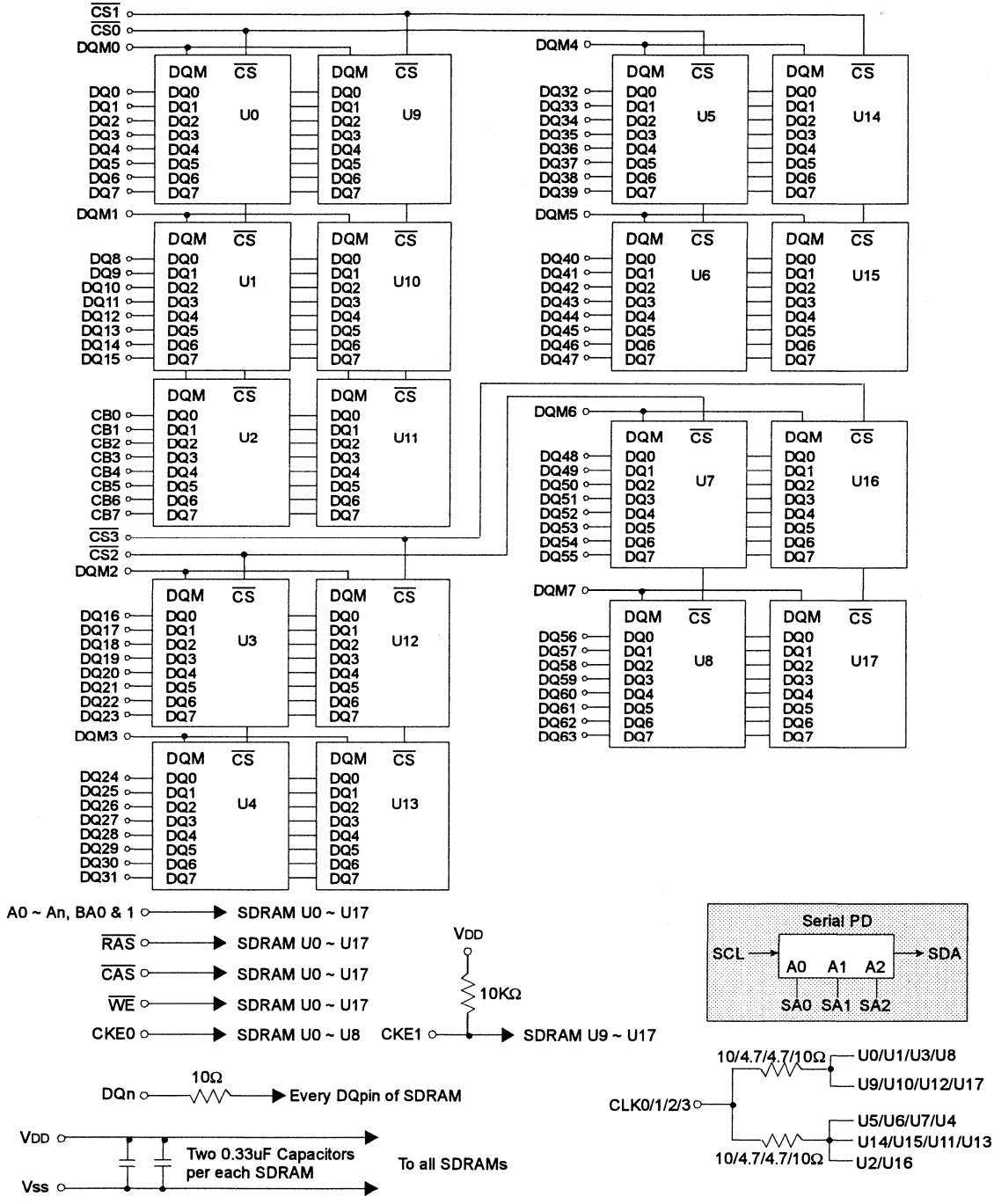
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	18	W
Short circuit current	I_{OS}	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11, BA0 ~ BA1)	C_{IN1}	50	95	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	50	95	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	28	50	pF
Input capacitance (CLK0 ~ CLK3)	C_{IN4}	18	25	pF
Input capacitance ($\overline{CS0}$ ~ $\overline{CS3}$)	C_{IN5}	18	30	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	13	20	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT1}	13	18	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT2}	13	18	pF

MAXIMUM TRACE LENGTHS

Signal	Max lengths	Unit	Signal	Max lengths	Unit
A0 ~ A11	9.0	Inches	CKE0 ~ CKE1	6.0	Inches
BA0 ~ BA1	9.0	Inches	$\overline{CS0}$ ~ $\overline{CS3}$	4.0	Inches
$\overline{RAS}$	9.0	Inches	DQM0 ~ DQM7	3.0	Inches
$\overline{CAS}$	9.0	Inches	DQ0 ~ DQ63	2.0	Inches
$\overline{WE}$	9.0	Inches	CB0 ~ CB7	2.0	Inches

DC CHARACTERISTICS

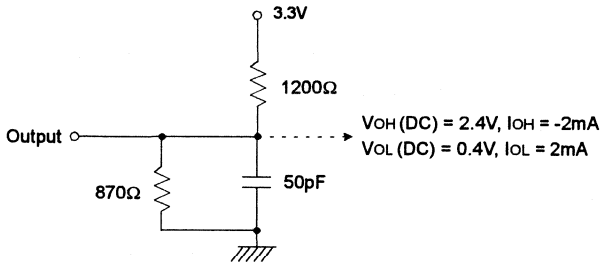
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-10		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	855	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	18	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	18		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	270	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	108		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	54	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	54		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	450	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	270	mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs	1,080	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	1,350	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	18	mA	

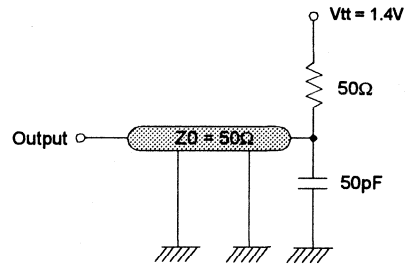
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	2	CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns	-	5
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -10, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tSAC		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	tOH	3		ns	1,2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tSS	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	1
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

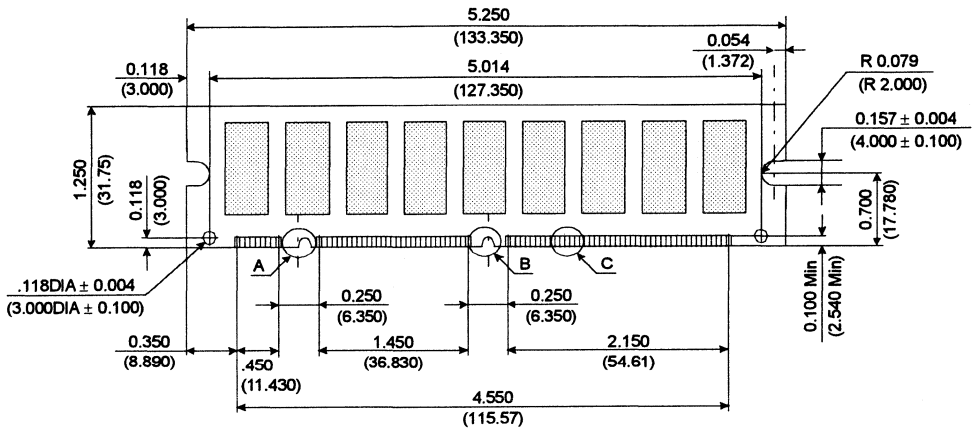
Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

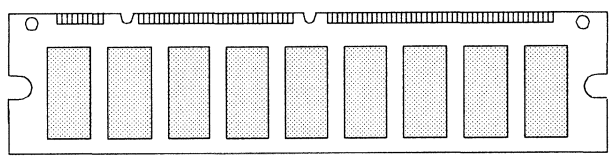
(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

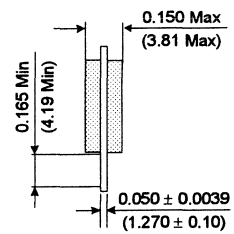
Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

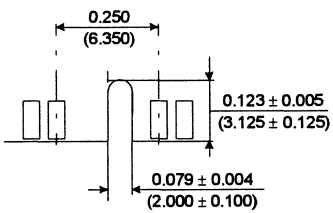
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

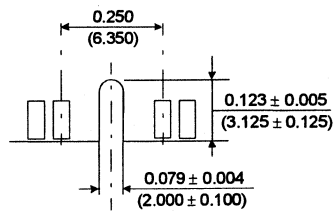




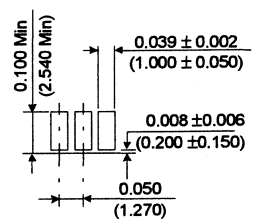




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4M640832D

M374S1623DTL-C10

- Organization : 16Mx72
- Composition : 8Mx8 *18
- Used component part # : K4S640832D-TC10
- # of banks in module : 2 banks
- # of banks in component : 4 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module banks on this assembly	2 banks	02h	
6	Data width of this assembly	72 bits	48h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	x8	08h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	2 banks of 64MB	10h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	FFh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	7	37h	
77	..... Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	..... Manufacturer part # (Module depth)	6	36h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	D	44h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	L	4Ch	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	L	4Ch	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M366S0424CTF SDRAM DIMM

4Mx64 SDRAM DIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S0424CTF is a 4M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S0424CTF consists of four CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.33uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M366S0424CTF is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S0424CTF-C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,000mil)** , single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	*CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection

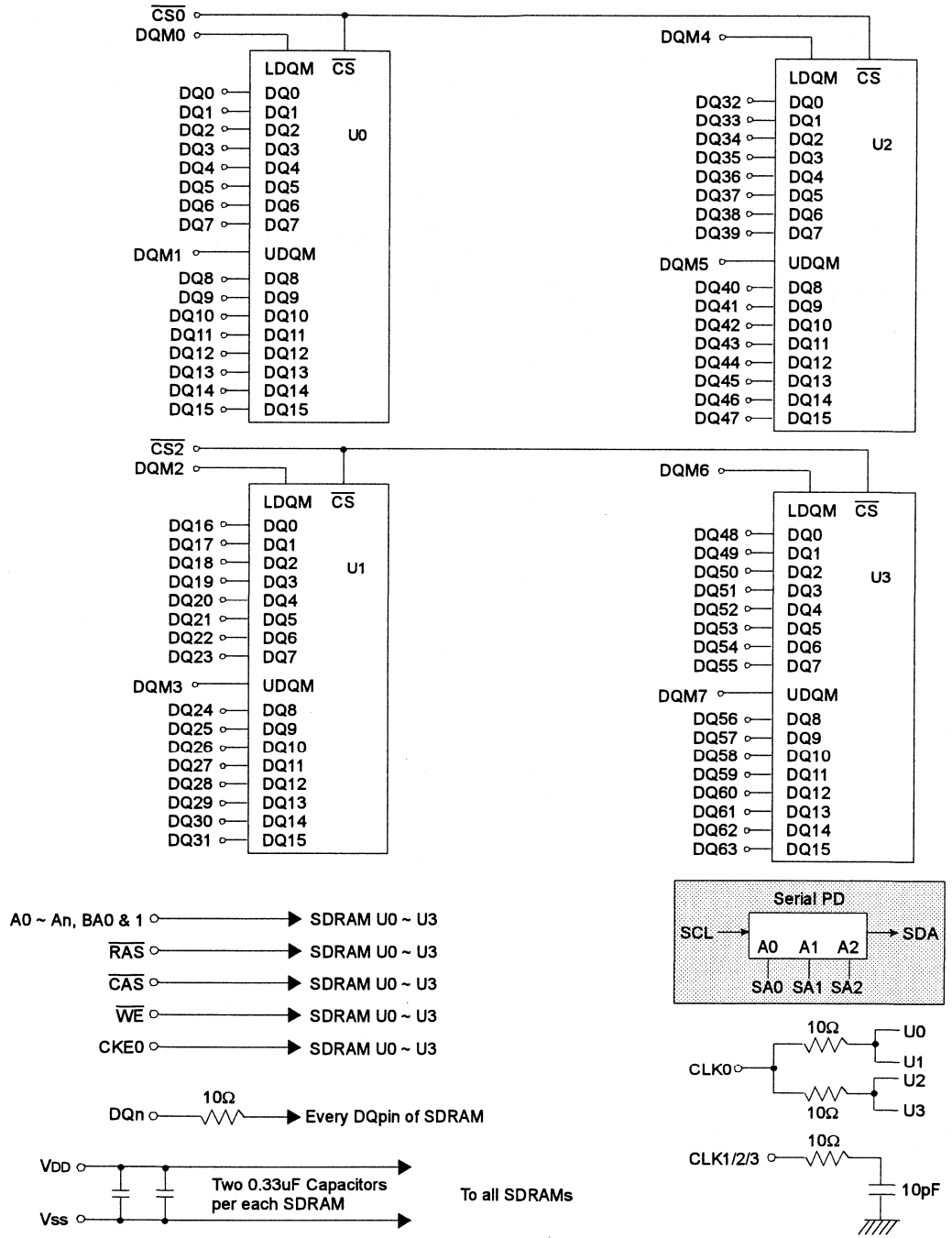
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA7
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*COlumn Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	4	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-4	-	4	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11, BA0 ~ BA1)	C_{IN1}	30	40	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	30	40	pF
Input capacitance (CKE0)	C_{IN3}	25	35	pF
Input capacitance (CLK0)	C_{IN4}	15	25	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	15	25	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	5	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	5	15	pF

MAXIMUM TRACE LENGTHS

Signal	Max lengths	Unit	Signal	Max lengths	Unit
A0 ~ A11	8.0	Inches	CKE0	5.5	Inches
BA0 ~ BA1	8.0	Inches	$\overline{CS0}$, $\overline{CS2}$	4.0	Inches
$\overline{RAS}$	8.0	Inches	DQM0 ~ DQM7	3.0	Inches
$\overline{CAS}$	8.0	Inches	DQ0 ~ DQ63	2.0	Inches
$\overline{WE}$	8.0	Inches			

DC CHARACTERISTICS

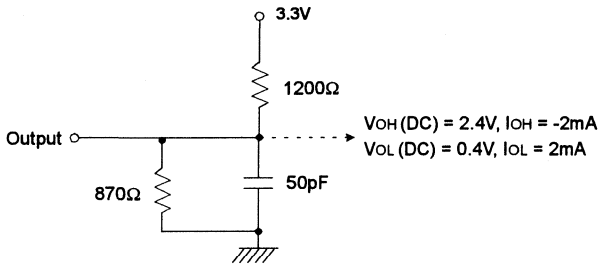
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -10	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		260	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		4	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		4		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), t_{CC} = 15ns Input signals are changed one time during 30ns		48	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		24		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		8	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		8		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), t_{CC} = 15ns Input signals are changed one time during 30ns		80	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		40	mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	300	mA	1
			2	280		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		500	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		4	mA	

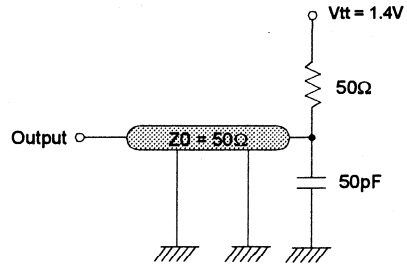
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	12	ns	2
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tSAC		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	tOH	3		ns	1,2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tSS	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	1
	CAS latency=2			7		

Notes :1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

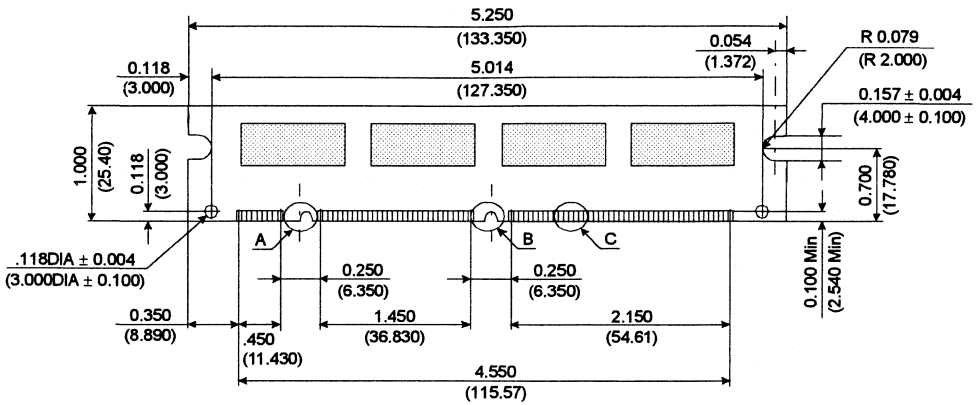
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

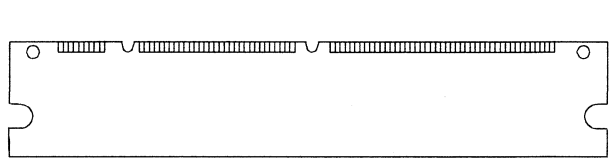
6. Burst stop command is valid at every burst length.

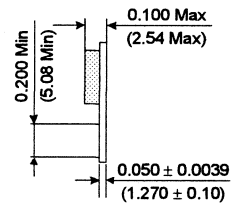
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

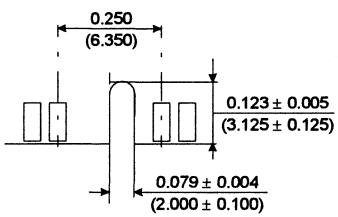
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

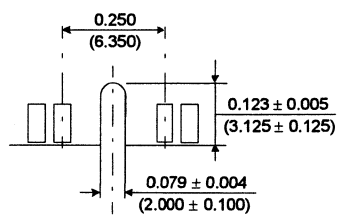




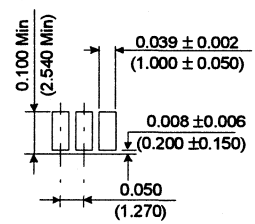




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : K4S641632C

M366S0424CTF-C10

- Organization : 4Mx64
- Composition : 4Mx16 *4
- Used component part # : K4S641632C-TC10
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,000mil height & single sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	8	08h	1
5	# of module banks on this assembly	1 bank	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	1 bank of 32MB	08h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	EBh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	4	34h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	C	43h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	F	46h	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	F	46h	
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)	43h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M366S0424CTL SDRAM DIMM

4Mx64 SDRAM DIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S0424CTL is a 4M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S0424CTL consists of four CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.33uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M366S0424CTL is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S0424CTL-C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,000mil)** , single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	*CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection

* These pins are not used in this module.

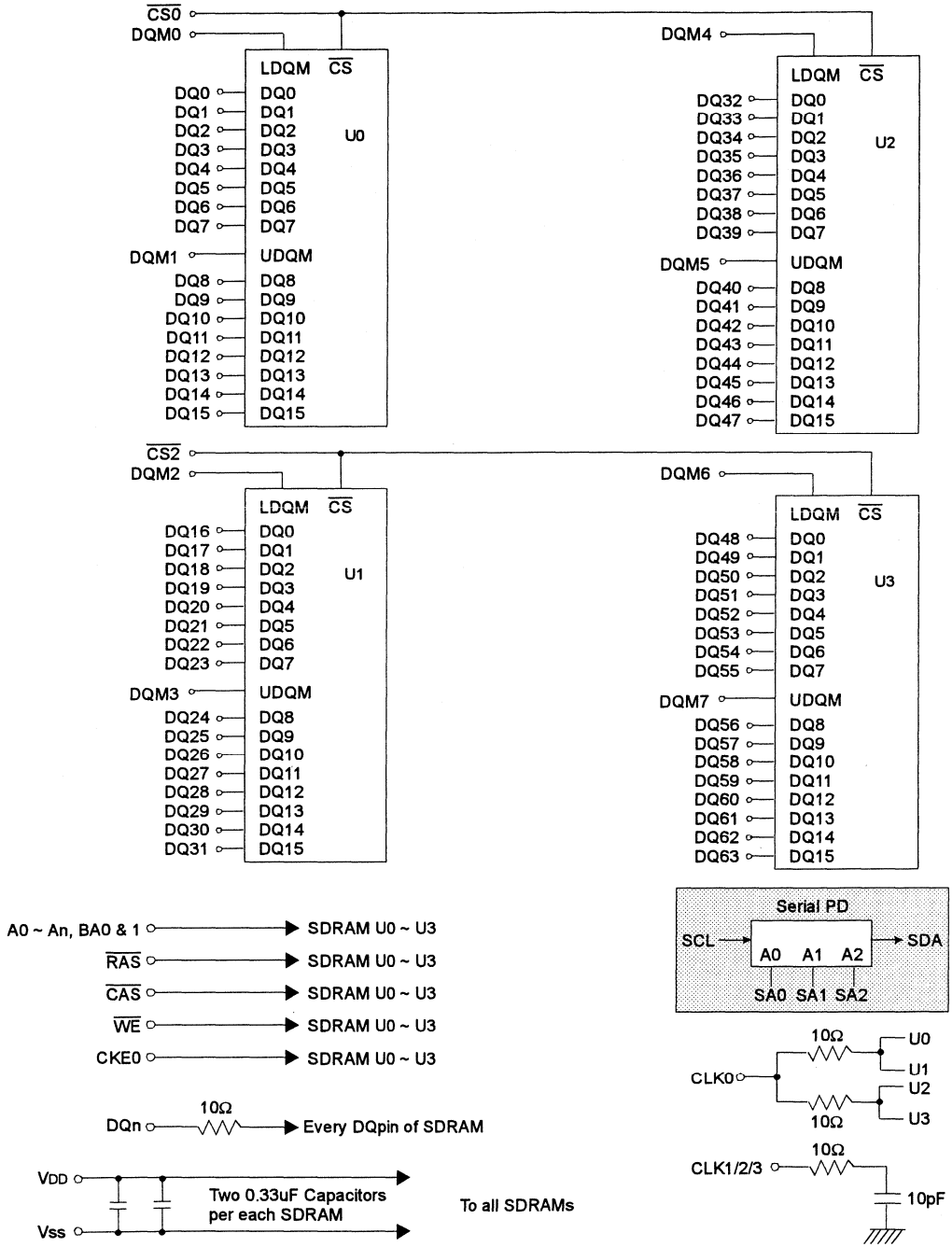
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA7
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*COlumn Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	4	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-4	-	4	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11, BA0 ~ BA1)	C_{IN1}	30	40	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	30	40	pF
Input capacitance (CKE0)	C_{IN3}	25	35	pF
Input capacitance (CLK0)	C_{IN4}	15	25	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	15	25	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	5	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	5	15	pF

MAXIMUM TRACE LENGTHS

Signal	Max lengths	Unit	Signal	Max lengths	Unit
A0 ~ A11	8.0	Inches	CKE0	5.5	Inches
BA0 ~ BA1	8.0	Inches	$\overline{CS0}$, $\overline{CS2}$	4.0	Inches
$\overline{RAS}$	8.0	Inches	DQM0 ~ DQM7	3.0	Inches
$\overline{CAS}$	8.0	Inches	DQ0 ~ DQ63	2.0	Inches
$\overline{WE}$	8.0	Inches			

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

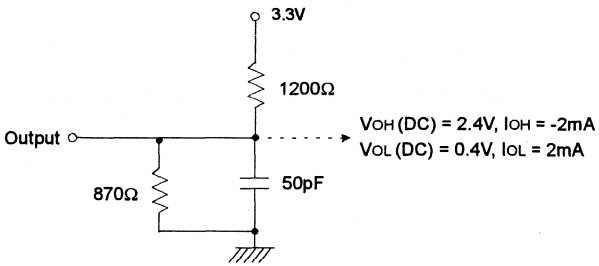
Parameter	Symbol	Test Condition	CAS Latency	Version -10	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		260	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		4	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		4		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		48	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		24		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		8	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		8		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		80	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		40	mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	300	mA	1
			2	280		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		500	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		4	mA	

Notes : 1. Measured with outputs open.

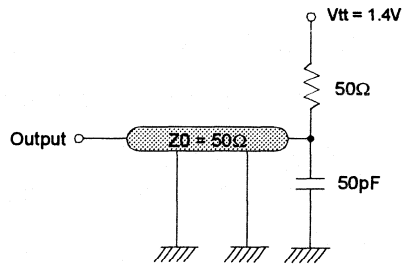
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	12	ns	2
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	t_{SAC}		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	t_{OH}	3		ns	1,2
	CAS latency=2		3			
CLK high pulse width		t_{CH}	3.5		ns	3
CLK low pulse width		t_{CL}	3.5		ns	3
Input setup time		t_{SS}	2.5		ns	3
Input hold time		t_{SH}	1.5		ns	3
CLK to output in Low-Z		t_{SLZ}	1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		7	ns	1
	CAS latency=2			7		

Notes :1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

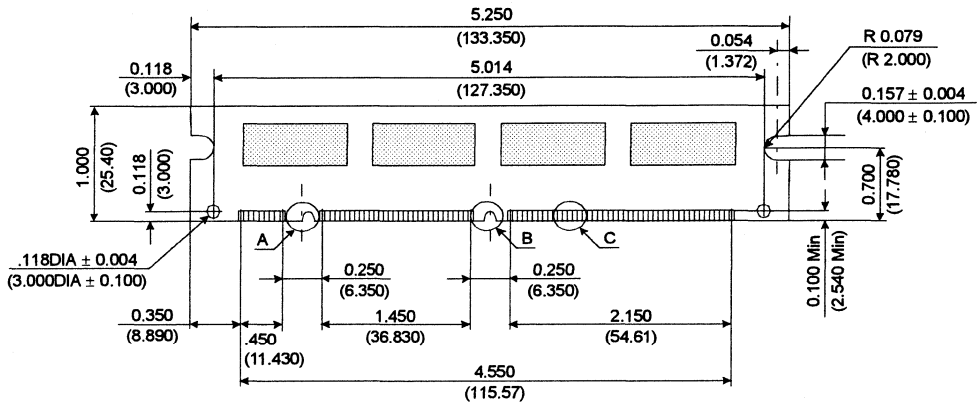
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

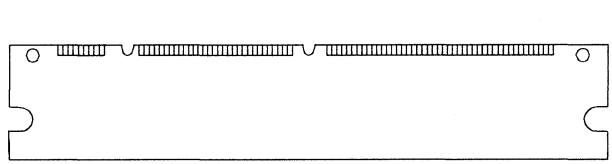
6. Burst stop command is valid at every burst length.

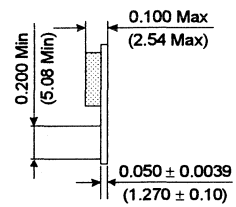
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

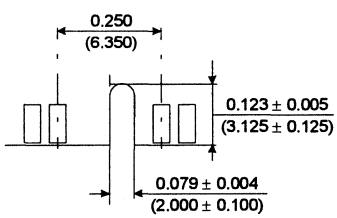
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

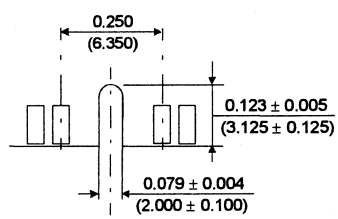




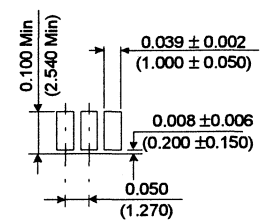




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : K4S641632C

M366S0424CTL-C10

- Organization : 4Mx64
- Composition : 4Mx16 *4
- Used component part # : K4S641632C-TC10
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,000mil height & single sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	8	08h	1
5	# of module banks on this assembly	1 bank	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	1 bank of 32MB	08h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	EBh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	4	34h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	C	43h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	L	4Ch	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	L	4Ch	
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)	43h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M366S0823CTF SDRAM DIMM

8Mx64 SDRAM DIMM based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S0823CTF is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S0823CTF consists of eight CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.33uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M366S0823CTF is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S0823CTF-C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,250mil)** , Single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection

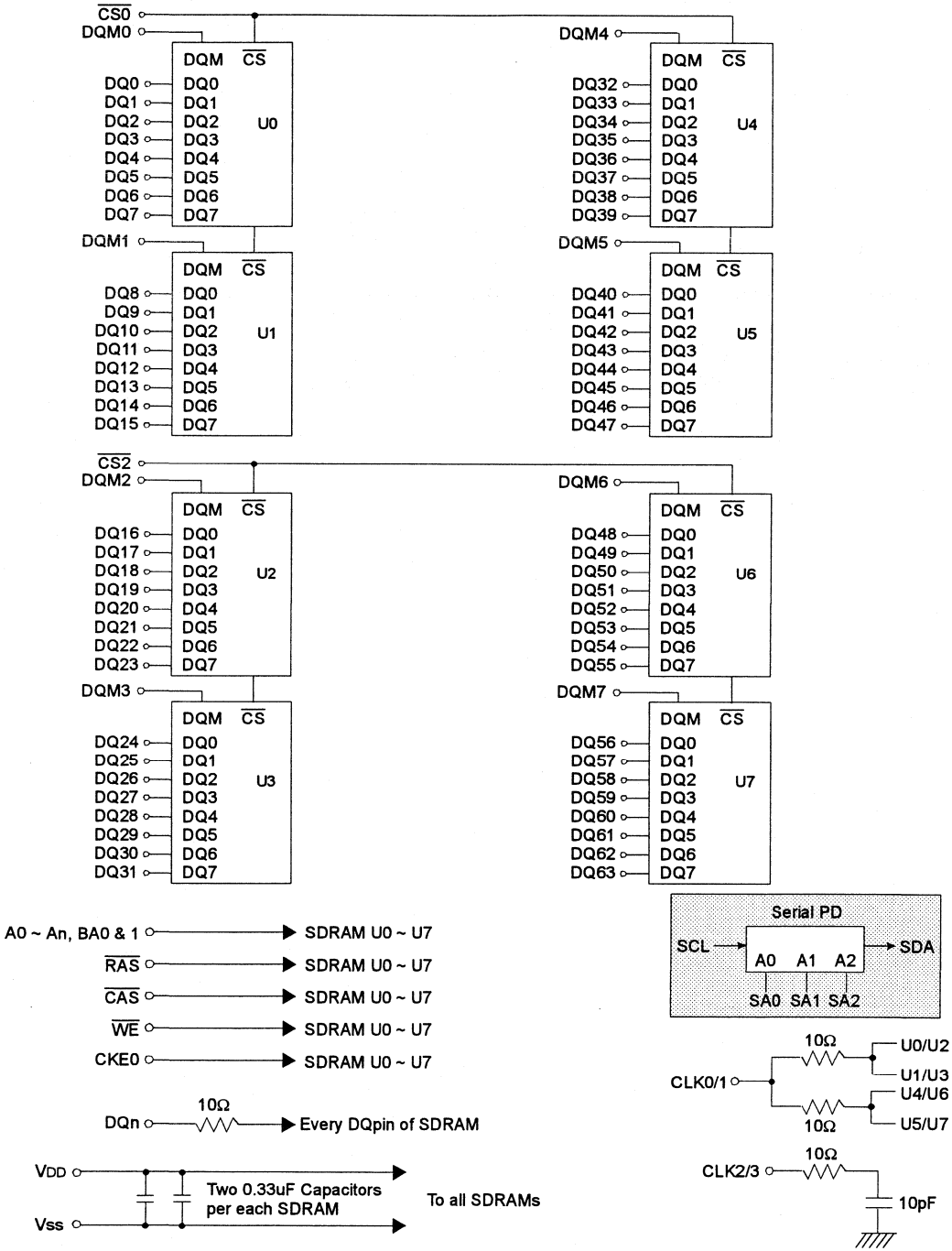
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-8	-	8	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11, BA0 ~ BA1)	C_{IN1}	40	60	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	40	60	pF
Input capacitance (CKE0)	C_{IN3}	35	55	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	25	35	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	25	35	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	5	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	5	15	pF

MAXIMUM TRACE LENGTHS

Signal	Max lengths	Unit	Signal	Max lengths	Unit
A0 ~ A11	8.0	Inches	CKE0	5.5	Inches
BA0 ~ BA1	8.0	Inches	$\overline{CS0}$, $\overline{CS2}$	4.0	Inches
$\overline{RAS}$	8.0	Inches	DQM0 ~ DQM7	3.0	Inches
$\overline{CAS}$	8.0	Inches	DQ0 ~ DQ63	2.0	Inches
$\overline{WE}$	8.0	Inches			

DC CHARACTERISTICS

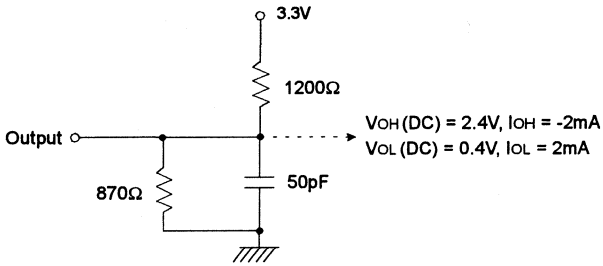
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -10	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		520	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		8	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		8		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		96	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		48		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		16	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		16		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		160	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		80	mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	600	mA	1
			2	560		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,000	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		8	mA	

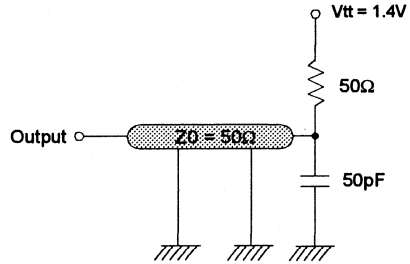
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	12	ns	2
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tSAC		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	tOH	3		ns	1,2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tSS	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	1
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A8)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A8)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

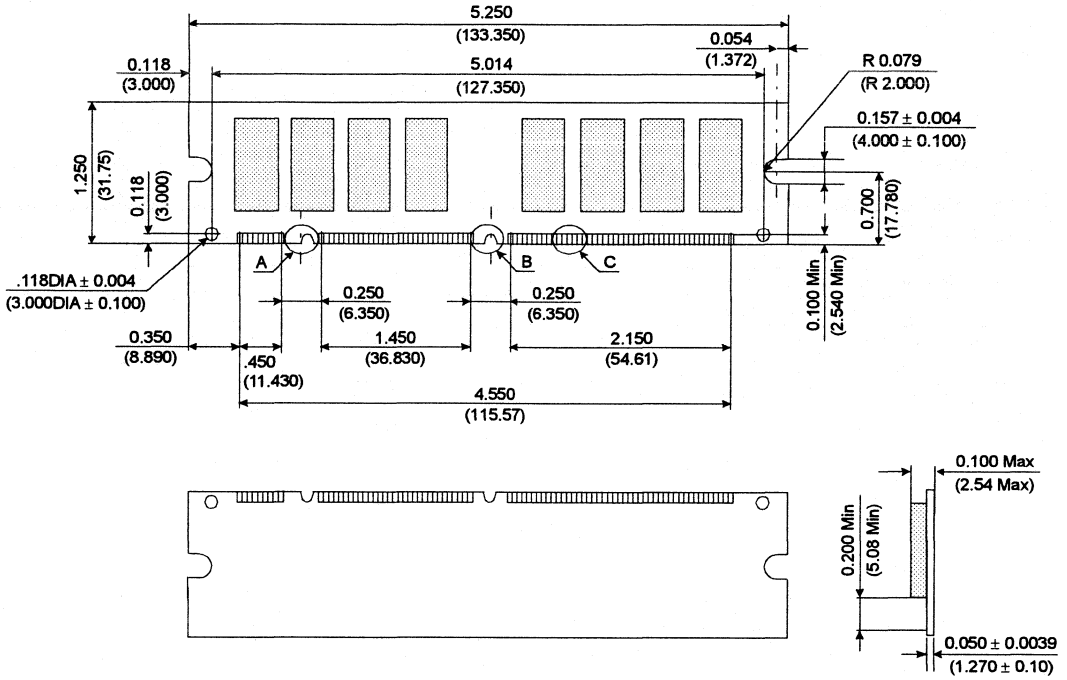
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

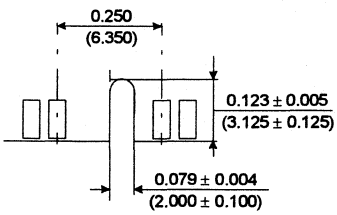
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

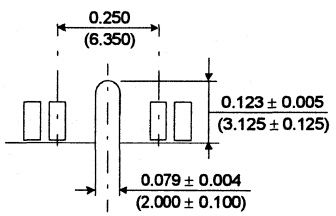
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

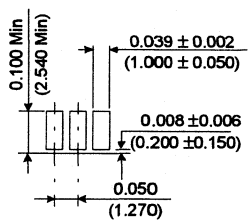




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832C

M366S0823CTF-C10

- Organization : 8Mx64
- Composition : 8Mx8 *8
- Used component part # : K4S640832C-TC10
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module banks on this assembly	1 bank	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	1 bank of 64MB	10h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	ECh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	8	38h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	C	43h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	F	46h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	F	46h	
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)	43h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M366S0823CTL SDRAM DIMM

8Mx64 SDRAM DIMM based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S0823CTL is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S0823CTL consists of eight CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.33uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M366S0823CTL is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S0823CTL-C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,000mil)** , Double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection

* These pins are not used in this module.

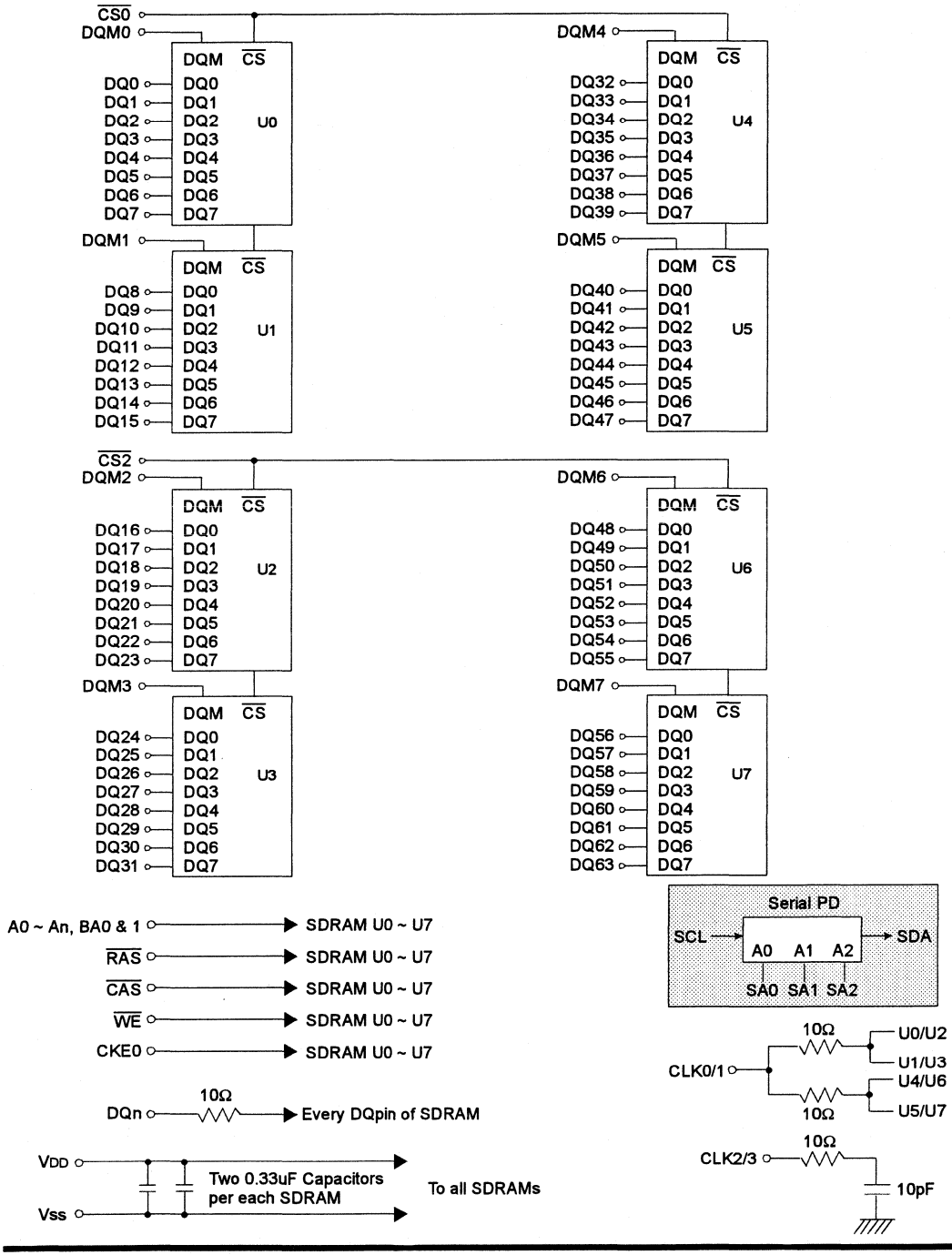
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-8	-	8	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11, BA0 ~ BA1)	C_{IN1}	40	60	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	40	60	pF
Input capacitance (CKE0)	C_{IN3}	35	55	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	25	35	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	25	35	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	5	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	5	15	pF

MAXIMUM TRACE LENGTHS

Signal	Max lengths	Unit	Signal	Max lengths	Unit
A0 ~ A11	8.0	Inches	CKE0	5.5	Inches
BA0 ~ BA1	8.0	Inches	$\overline{CS0}$, $\overline{CS2}$	4.0	Inches
$\overline{RAS}$	8.0	Inches	DQM0 ~ DQM7	3.0	Inches
$\overline{CAS}$	8.0	Inches	DQ0 ~ DQ63	2.0	Inches
$\overline{WE}$	8.0	Inches			

DC CHARACTERISTICS

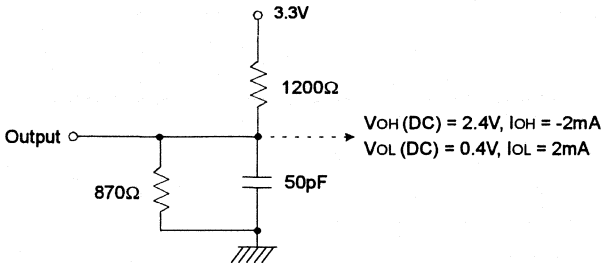
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -10	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		520	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		8	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		8		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		96	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		48		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		16	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		16		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		160	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		80	mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	600	mA	1
			2	560		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,000	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		8	mA	

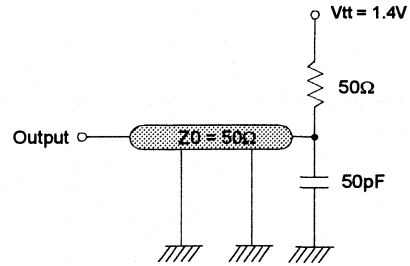
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	12	ns	2
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tSAC		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	tOH	3		ns	1,2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tSS	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	1
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

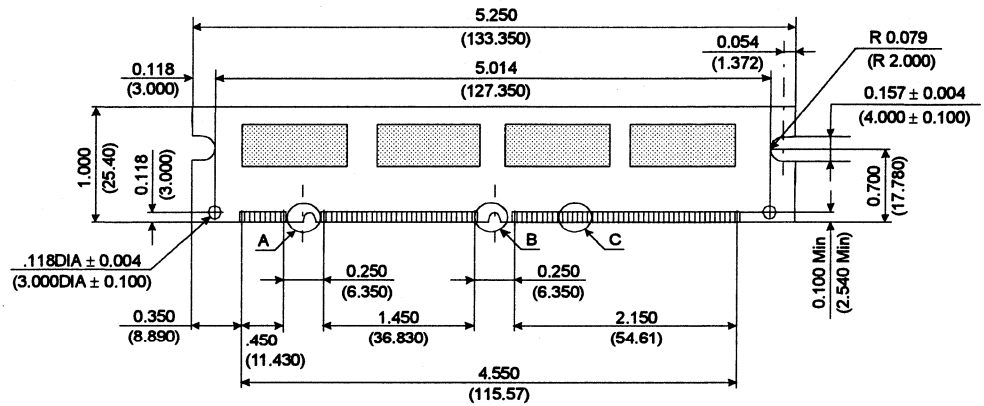
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

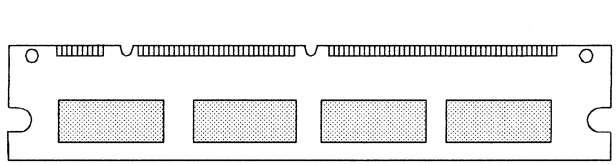
6. Burst stop command is valid at every burst length.

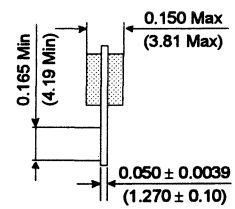
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

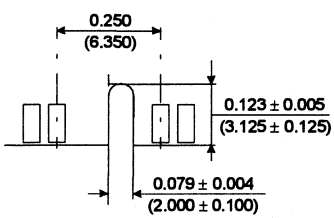
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

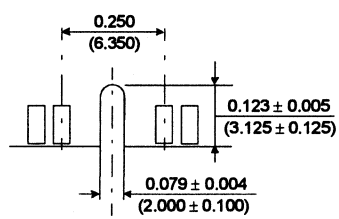




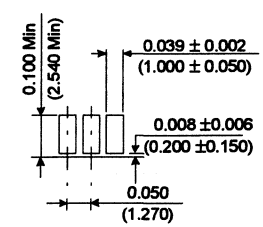




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832C

M366S0823CTL-C10

- Organization : 8Mx64
- Composition : 8Mx8 *8
- Used component part # : K4S640832C-TC10
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module banks on this assembly	1 bank	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	1 bank of 64MB	10h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	ECh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	8	38h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	C	43h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	L	4Ch	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	L	4Ch	
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)	43h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M366S0824CTL SDRAM DIMM

8Mx64 SDRAM DIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S0824CTL is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S0824CTL consists of eight CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.33uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M366S0824CTL is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S0824CTL-C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,000mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	*CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0 ~ CKE1	Clock enable input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection

* These pins are not used in this module.

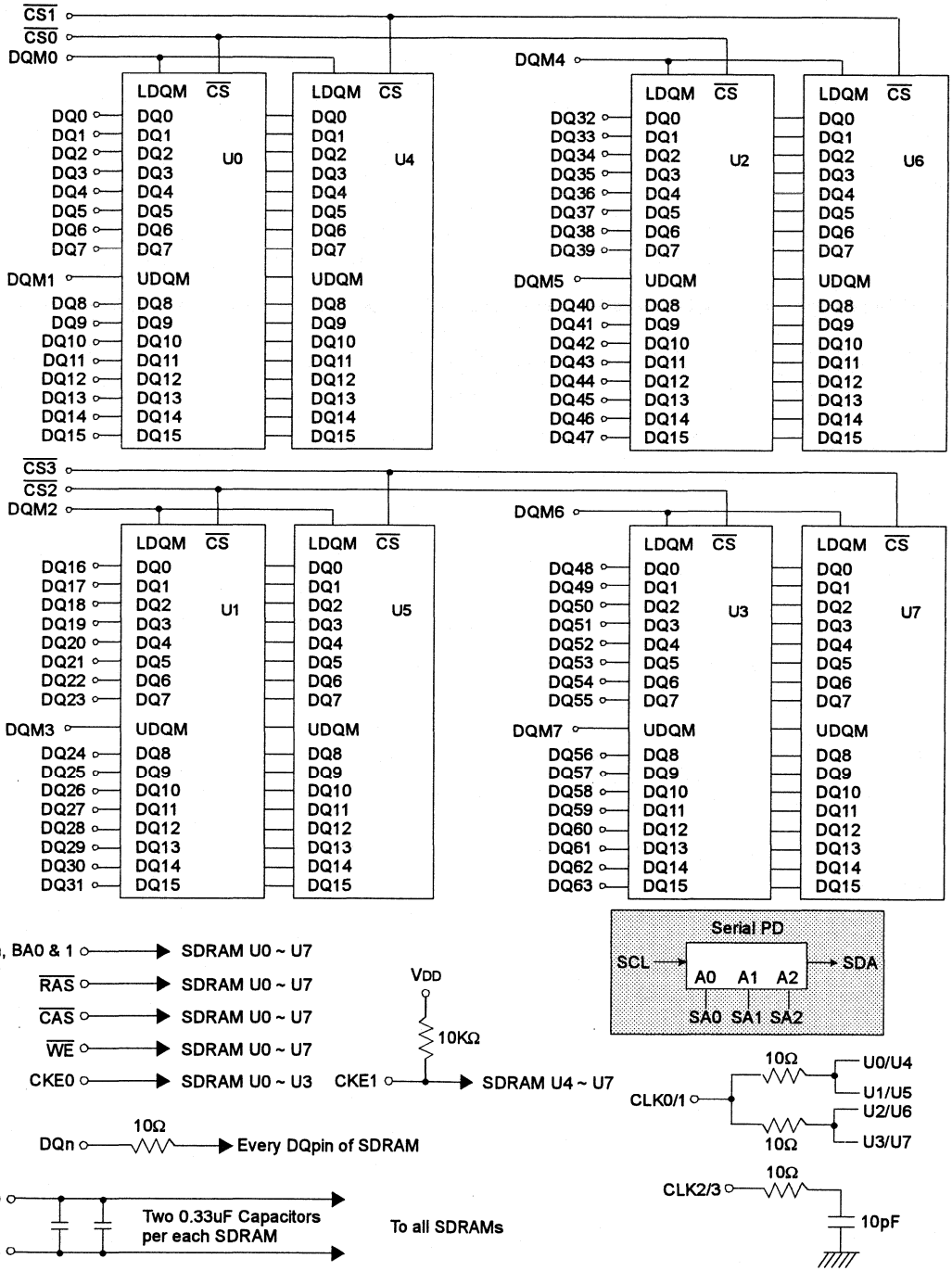
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA7
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*COlumn Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-8	-	8	uA	3
Input leakage current (I/O pins)	I_{IL}	-3	-	3	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11, BA0 ~ BA1)	C_{IN1}	40	60	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	40	60	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	25	35	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	25	35	pF
Input capacitance ($\overline{CS0}$ ~ $\overline{CS3}$)	C_{IN5}	15	25	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	15	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	5	15	pF

MAXIMUM TRACE LENGTHS

Signal	Max lengths	Unit	Signal	Max lengths	Unit
A0 ~ A11	8.0	Inches	CKE0 ~ CKE1	5.5	Inches
BA0 ~ BA1	8.0	Inches	$\overline{CS0}$ ~ $\overline{CS3}$	4.0	Inches
$\overline{RAS}$	8.0	Inches	DQM0 ~ DQM7	3.0	Inches
$\overline{CAS}$	8.0	Inches	DQ0 ~ DQ63	2.0	Inches
$\overline{WE}$	8.0	Inches			

DC CHARACTERISTICS

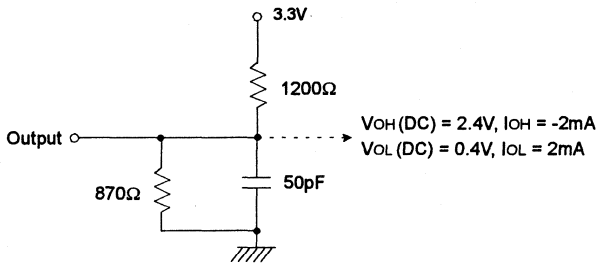
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -10	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		340	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		8	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		8		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		96	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		48		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		16	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		16		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		160	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		80	mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	380	mA	1
			2	360		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,000	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		8	mA	

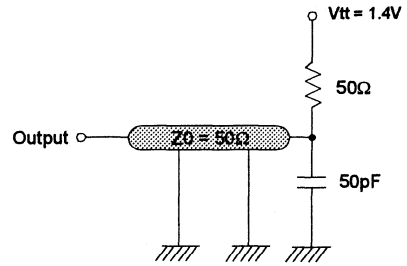
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	12	ns	2
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tSAC		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	tOH	3		ns	1,2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tSS	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	1
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

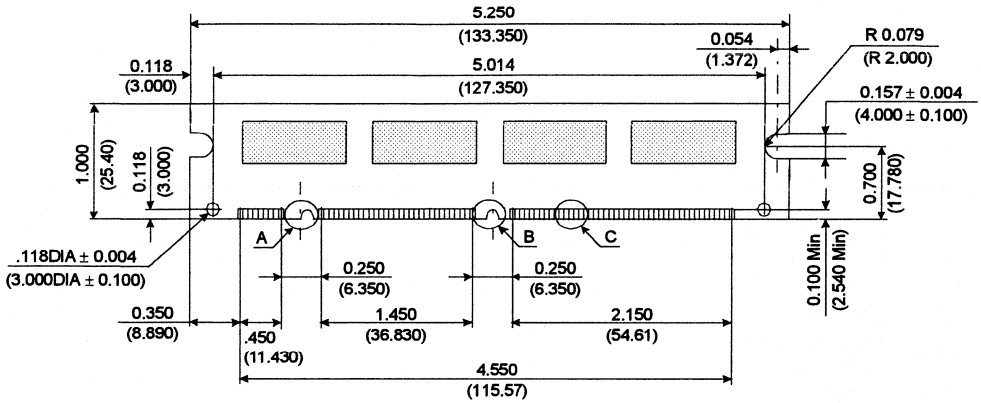
Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

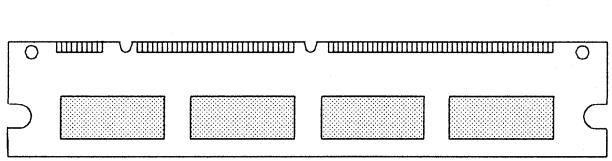
(V=Valid, X=Don't care, H=Logic high, L=Logic low)

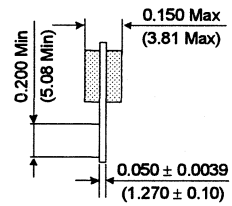
Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

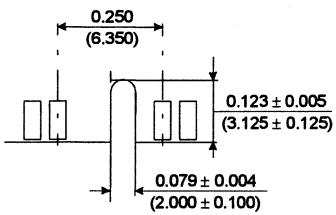
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

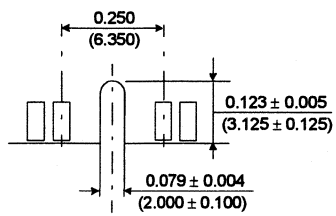




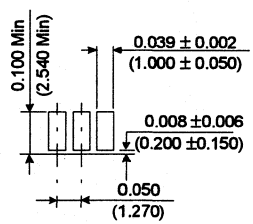




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : K4S641632C

M366S0824CTL-C10

- Organization : 8Mx64
- Composition : 4Mx16 *8
- Used component part # : K4S641632C-TC10
- # of banks in module : 2 banks
- # of banks in component : 4 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	8	08h	1
5	# of module banks on this assembly	2 banks	02h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	2 banks of 32MB	08h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	ECh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	8	38h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	C	43h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	L	4Ch	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	L	4Ch	
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)	43h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M366S1623CTL SDRAM DIMM

16Mx64 SDRAM DIMM based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S1623CTL is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S1623CTL consists of sixteen CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.33uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M366S1623CTL is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

• Performance range

Part No.	Max Freq. (Speed)
M366S1623CTL-C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,250mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection

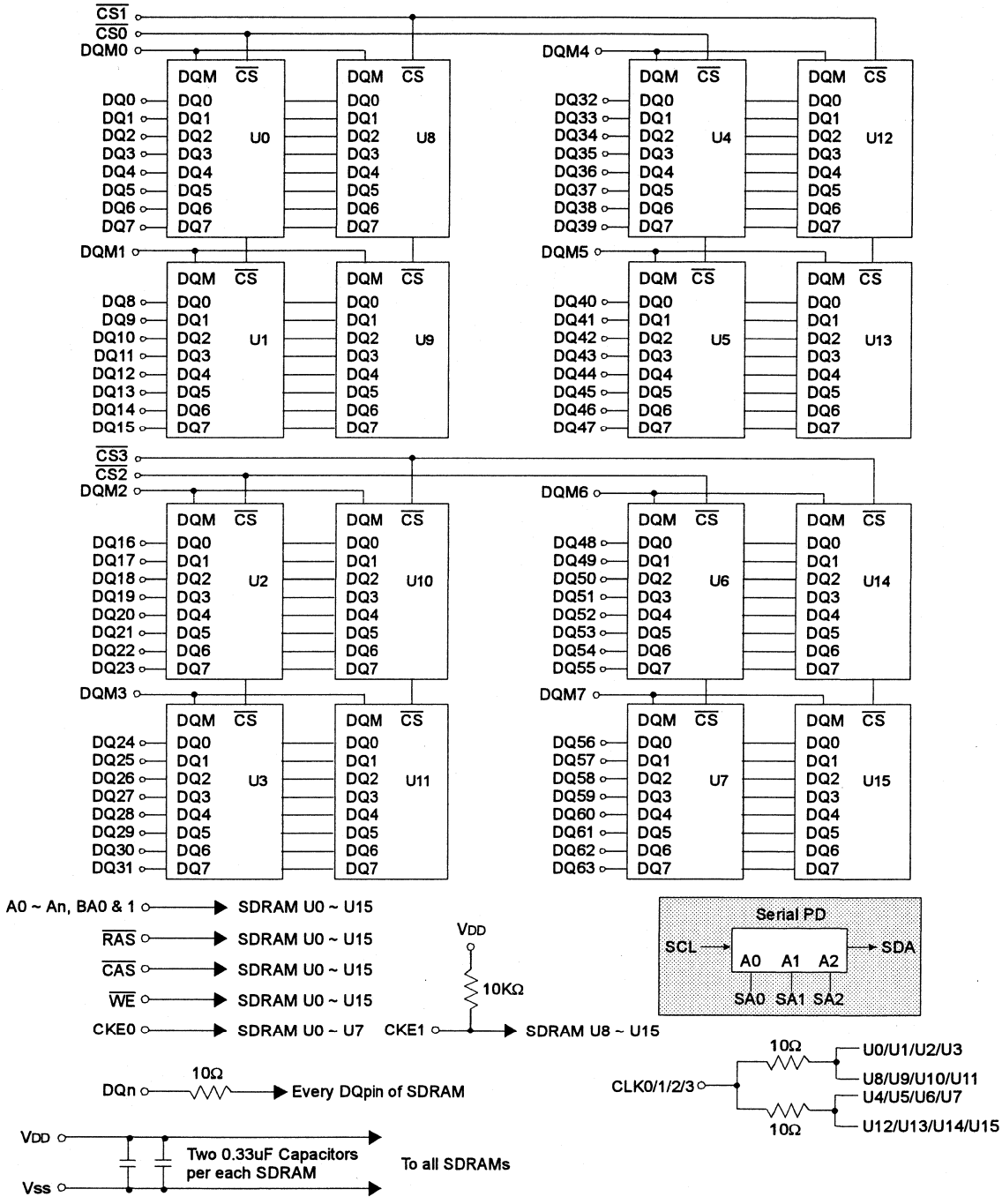
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*COlumn Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	16	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-16	-	16	uA	3
Input leakage current (I/O pins)	I_{IL}	-3	-	3	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include HI-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11, BA0 ~ BA1)	C_{IN1}	60	90	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	60	90	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	35	55	pF
Input capacitance (CLK0 ~ CLK3)	C_{IN4}	25	35	pF
Input capacitance ($\overline{CS0}$ ~ $\overline{CS3}$)	C_{IN5}	25	35	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	15	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	10	20	pF

MAXIMUM TRACE LENGTHS

Signal	Max lengths	Unit	Signal	Max lengths	Unit
A0 ~ A11	8.0	Inches	CKE0 ~ CKE1	5.5	Inches
BA0 ~ BA1	8.0	Inches	$\overline{CS0}$ ~ $\overline{CS3}$	4.0	Inches
$\overline{RAS}$	8.0	Inches	DQM0 ~ DQM7	3.0	Inches
$\overline{CAS}$	8.0	Inches	DQ0 ~ DQ63	2.0	Inches
$\overline{WE}$	8.0	Inches			

DC CHARACTERISTICS

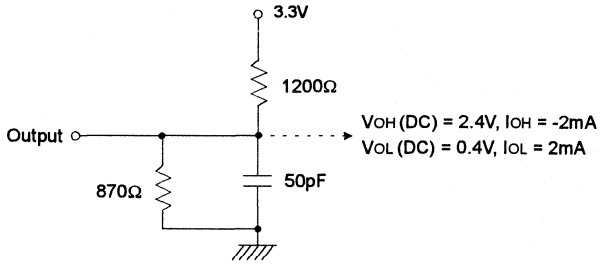
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -10	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		680	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		16	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		16		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		192	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		96		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		32	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		32		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		320	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		160	mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	760	mA	1
			2	720		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		2,000	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		16	mA	

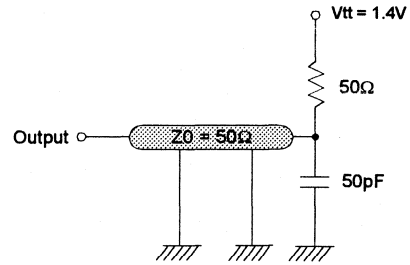
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	12	ns	2
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	t_{SAC}		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	t_{OH}	3		ns	1,2
	CAS latency=2		3			
CLK high pulse width		t_{CH}	3.5		ns	3
CLK low pulse width		t_{CL}	3.5		ns	3
Input setup time		t_{SS}	2.5		ns	3
Input hold time		t_{SH}	1.5		ns	3
CLK to output in Low-Z		t_{SLZ}	1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		7	ns	1
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

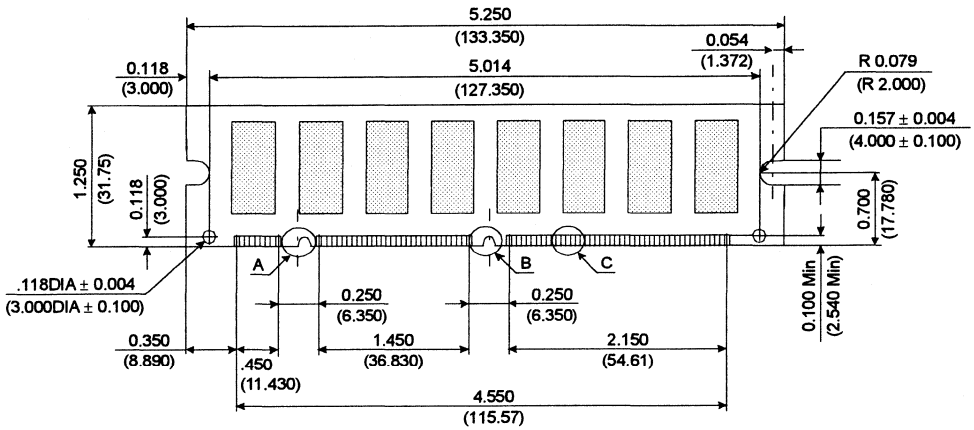
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

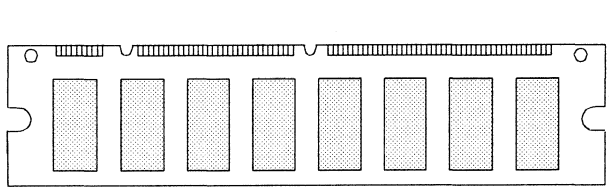
6. Burst stop command is valid at every burst length.

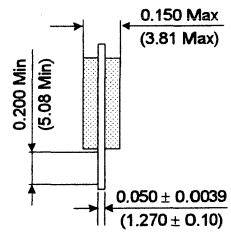
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

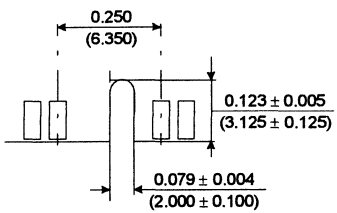
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

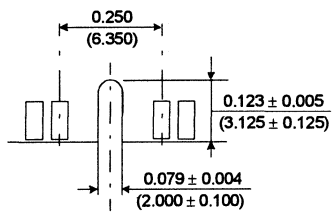




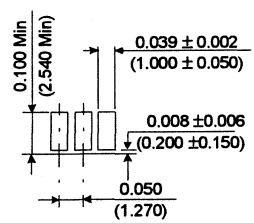




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832C

M366S1623CTL-C10

- Organization : 16Mx64
- Composition : 8Mx8 *16
- Used component part # : K4S640832C-TC10
- # of banks in module : 2 banks
- # of banks in component : 4 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module banks on this assembly	2 banks	02h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	2 banks of 64MB	10h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	EDh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	..... Manufacturer part # (Module depth)	6	36h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	C	43h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	L	4Ch	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	L	4Ch	
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)	43h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M374S0823CTF SDRAM DIMM

8Mx72 SDRAM DIMM with ECC based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S0823CTF is a 8M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S0823CTF consists of nine CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.33uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M374S0823CTF is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S0823CTF-C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,250mil)** , Single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	*CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0 ~ CLK1	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection

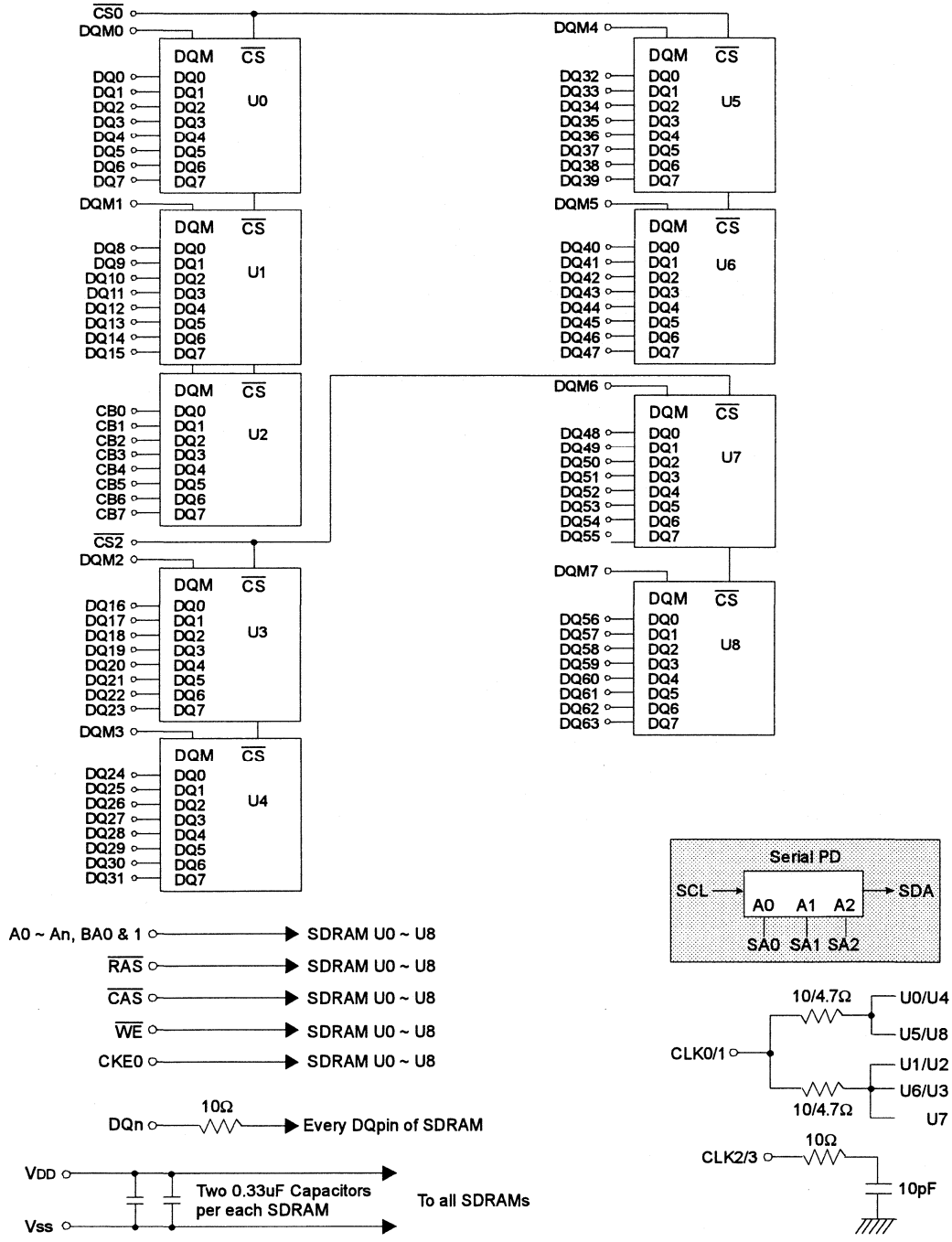
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	9	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-9	-	9	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11, BA0 ~ BA1)	C_{IN1}	45	65	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	45	65	pF
Input capacitance (CKE0)	C_{IN3}	40	60	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	30	40	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	30	40	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	5	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT1}	5	15	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT2}	5	15	pF

MAXIMUM TRACE LENGTHS

Signal	Max lengths	Unit	Signal	Max lengths	Unit
A0 ~ A11	9.0	Inches	CKE0	6.0	Inches
BA0 ~ BA1	9.0	Inches	$\overline{CS0}$, $\overline{CS2}$	4.0	Inches
$\overline{RAS}$	9.0	Inches	DQM0 ~ DQM7	3.0	Inches
$\overline{CAS}$	9.0	Inches	DQ0 ~ DQ63	2.0	Inches
$\overline{WE}$	9.0	Inches	CB0 ~CB7	2.0	Inches

DC CHARACTERISTICS

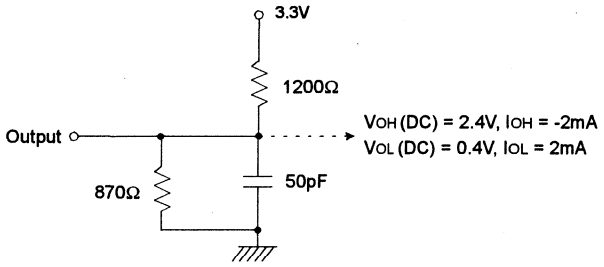
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -10	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		585	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		9	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		9		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		108	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		54		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		18	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		18		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		180	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		90	mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	675	mA	1
			2	630		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,125	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		9	mA	

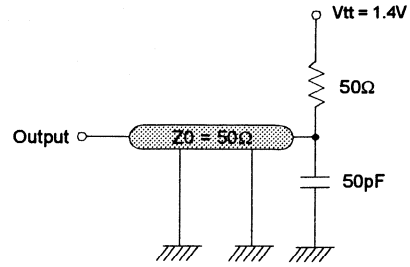
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	12	ns	2
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	t_{SAC}		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	t_{OH}	3		ns	1,2
	CAS latency=2		3			
CLK high pulse width		t_{CH}	3.5		ns	3
CLK low pulse width		t_{CL}	3.5		ns	3
Input setup time		t_{SS}	2.5		ns	3
Input hold time		t_{SH}	1.5		ns	3
CLK to output in Low-Z		t_{SLZ}	1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		7	ns	1
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row Address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

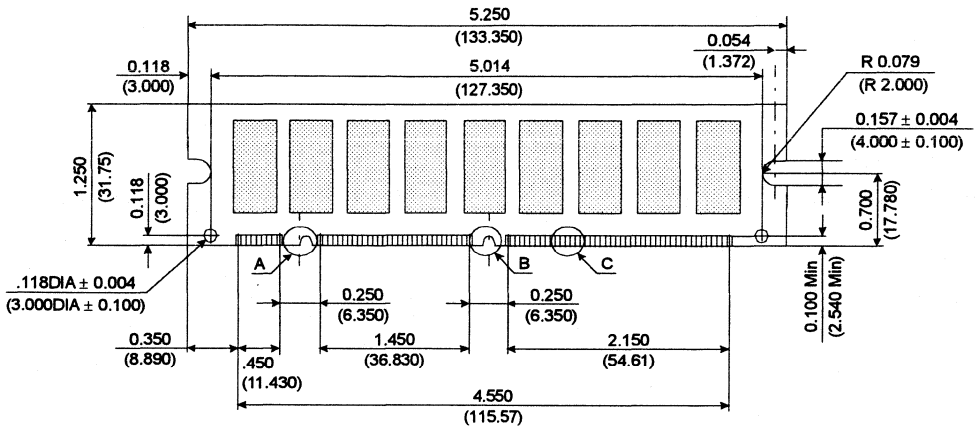
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

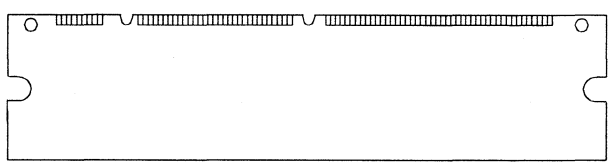
6. Burst stop command is valid at every burst length.

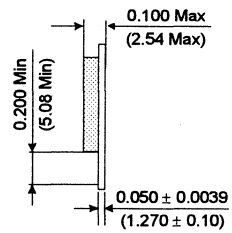
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

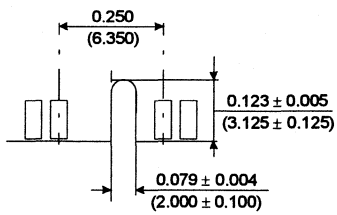
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

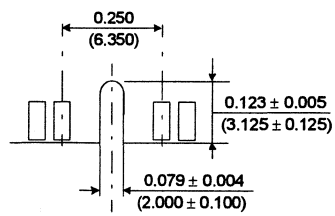




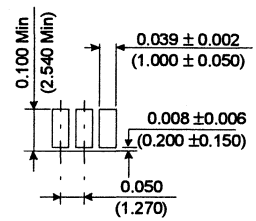




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832C

M374S0823CTF-C10

- Organization : 8Mx72
- Composition : 8Mx8 *9
- Used component part # : K4S640832C-TC10
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module banks on this assembly	1 bank	01h	
6	Data width of this assembly	72 bits	48h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	x8	08h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	1 bank of 64MB	10h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	FEh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	7	37h	
77	..... Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	8	38h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	C	43h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	F	46h	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	F	46h	
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)	43h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M374S0823CTL SDRAM DIMM

8Mx72 SDRAM DIMM with ECC based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S0823CTL is a 8M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S0823CTL consists of nine CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.33uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M374S0823CTL is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S0823CTL-C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,000mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	*CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0 ~ CLK1	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection

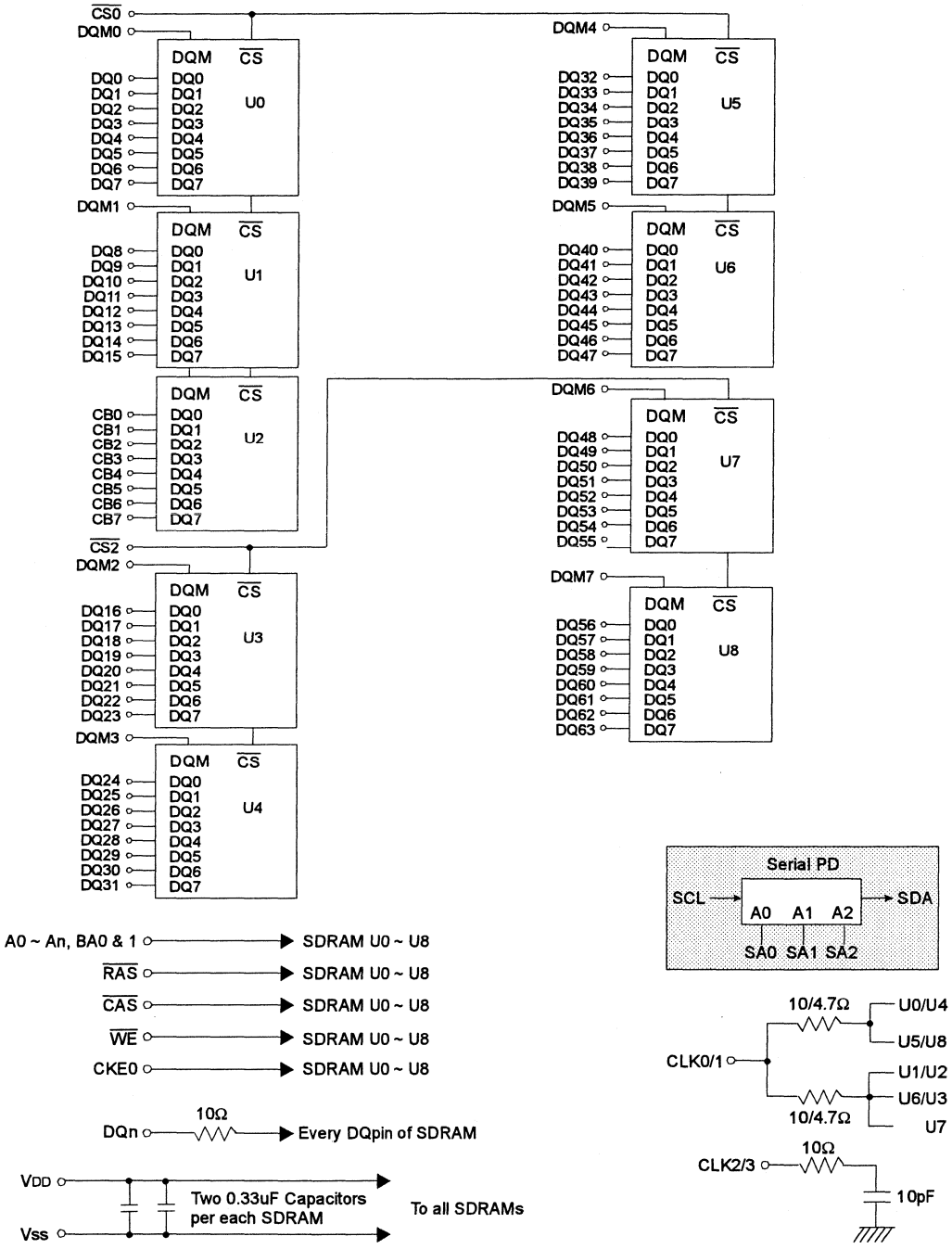
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	9	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-10.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-9	-	9	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11, BA0 ~ BA1)	C_{IN1}	45	65	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	45	65	pF
Input capacitance (CKE0)	C_{IN3}	40	60	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	30	40	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	30	40	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	5	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT1}	5	15	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT2}	5	15	pF

MAXIMUM TRACE LENGTHS

Signal	Max lengths	Unit	Signal	Max lengths	Unit
A0 ~ A11	9.0	Inches	CKE0	6.0	Inches
BA0 ~ BA1	9.0	Inches	$\overline{CS0}$, $\overline{CS2}$	4.0	Inches
$\overline{RAS}$	9.0	Inches	DQM0 ~ DQM7	3.0	Inches
$\overline{CAS}$	9.0	Inches	DQ0 ~ DQ63	2.0	Inches
$\overline{WE}$	9.0	Inches	CB0 ~CB7	2.0	Inches

DC CHARACTERISTICS

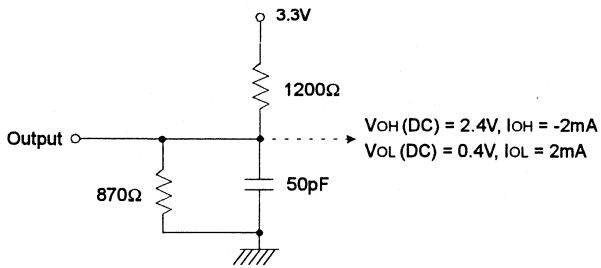
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -10	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		585	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		9	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		9		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		108	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		54		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		18	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		18		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		180	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		90	mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	675	mA	1
			2	630		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,125	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		9	mA	

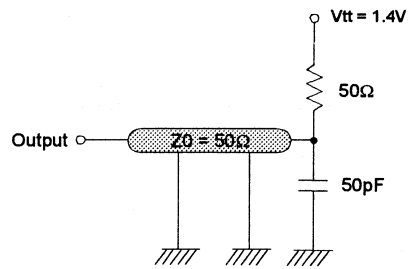
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		t_{RRD}(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		t_{RCD}(min)	24	ns	1
Row precharge time		t_{RP}(min)	24	ns	1
Row active time		t_{RAS}(min)	50	ns	1
		t_{RAS}(max)	100	us	
Row cycle time		t_{RC}(min)	80	ns	1
Last data in to row precharge		t_{RDL}(min)	12	ns	2
Last data in to new col. address delay		t_{CDL}(min)	1	CLK	2
Last data in to burst stop		t_{BDL}(min)	1	CLK	2
Col. address to col. address delay		t_{CCD}(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	t_{SAC}		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	t_{OH}	3		ns	1,2
	CAS latency=2		3			
CLK high pulse width		t_{CH}	3.5		ns	3
CLK low pulse width		t_{CL}	3.5		ns	3
Input setup time		t_{SS}	2.5		ns	3
Input hold time		t_{SH}	1.5		ns	3
CLK to output in Low-Z		t_{SLZ}	1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		7	ns	1
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-10.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row Address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

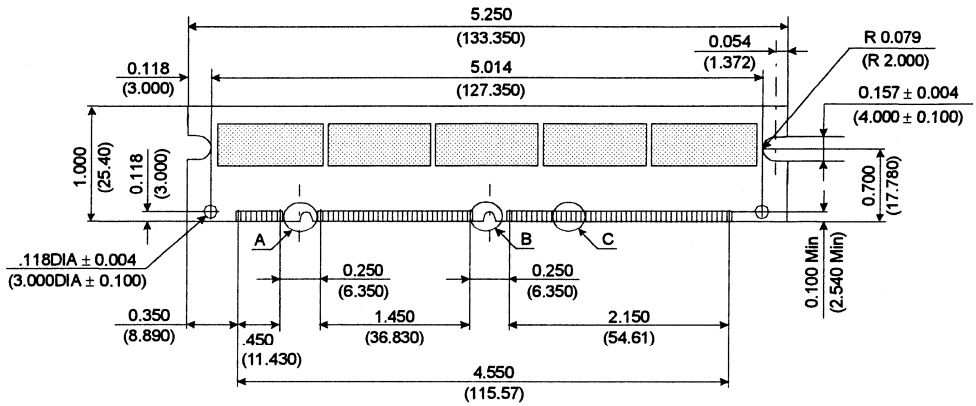
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

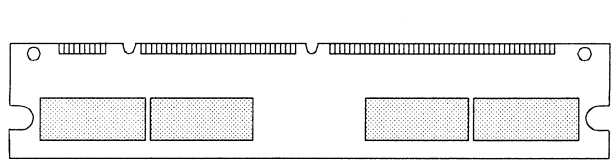
6. Burst stop command is valid at every burst length.

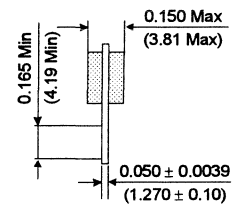
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

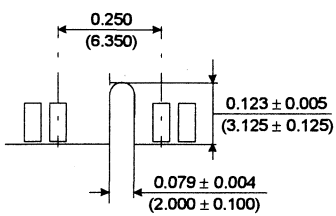
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

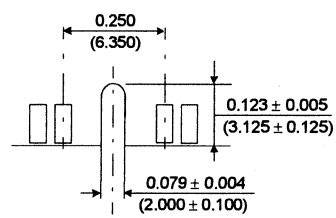




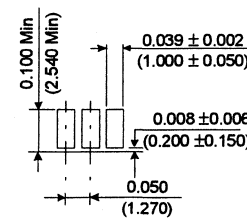




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832C

M374S0823CTL-C10

- Organization : 8Mx72
- Composition : 8Mx8 *9
- Used component part # : K4S640832C-TC10
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms
- **Contents** ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module banks on this assembly	1 bank	01h	
6	Data width of this assembly	72 bits	48h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	x8	08h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	1 bank of 64MB	10h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	FEh	

Byte #	Function Described	Function Supported -10	Hex value -10	Note
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	7	37h	
77	..... Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	8	38h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	C	43h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	L	4Ch	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	L	4Ch	
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)	43h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M374S1623CTL SDRAM DIMM

16Mx72 SDRAM DIMM with ECC based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S1623CTL is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S1623CTL consists of eighteen CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.33uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M374S1623CTL is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S1623CTL-C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,250mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ 7	Check bit (Data-in/data-out)
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection

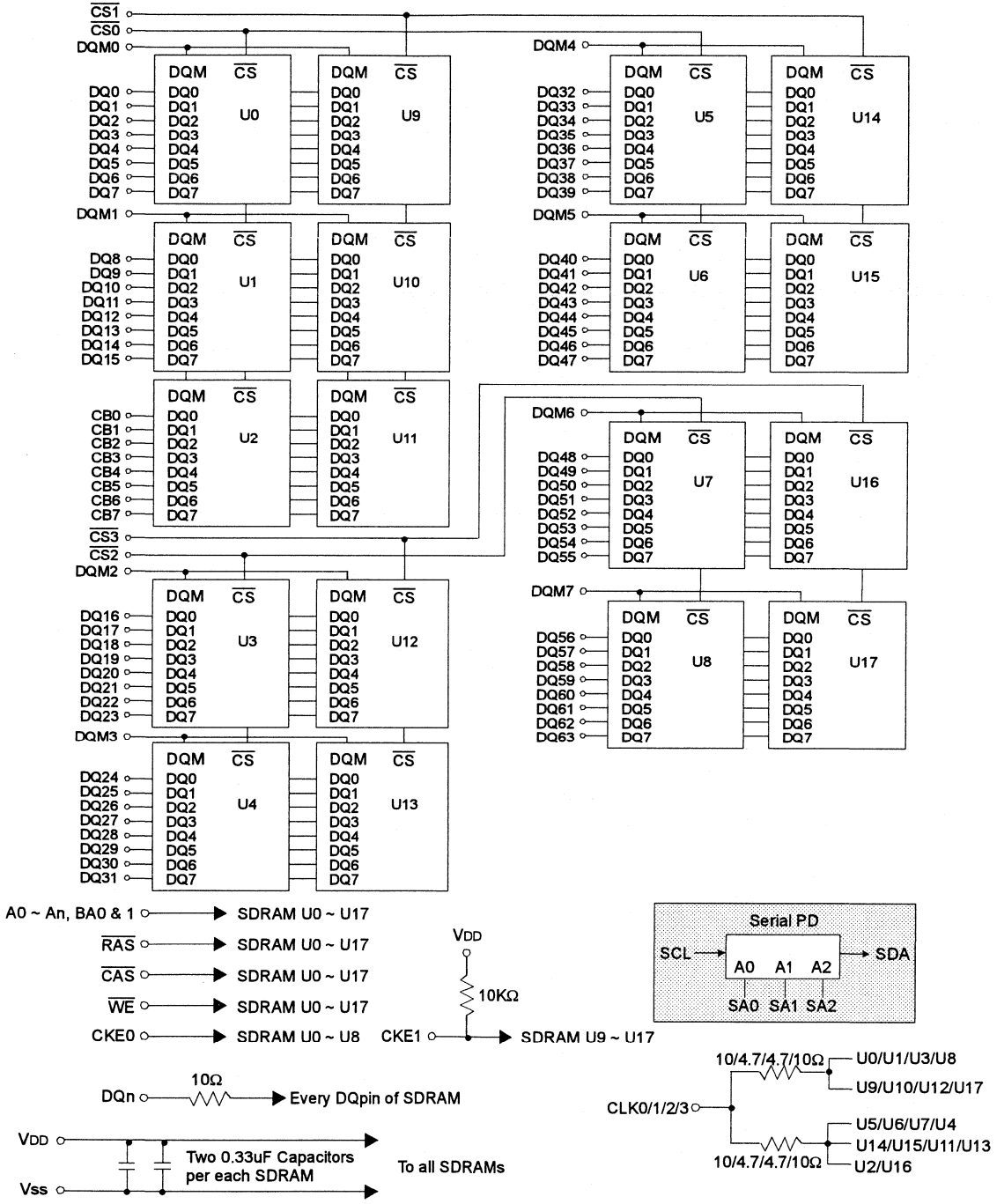
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	18	W
Short circuit current	I_{OS}	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-18	-	18	uA	3
Input leakage current (I/O pins)	I_{IL}	-3	-	3	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11, BA0 ~ BA1)	C_{IN1}	65	95	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	65	95	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	40	60	pF
Input capacitance (CLK0 ~ CLK3)	C_{IN4}	30	40	pF
Input capacitance ($\overline{CS0}$ ~ $\overline{CS3}$)	C_{IN5}	30	40	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	15	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT1}	10	20	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT2}	10	20	pF

MAXIMUM TRACE LENGTHS

Signal	Max lengths	Unit	Signal	Max lengths	Unit
A0 ~ A11	9.0	Inches	CKE0 ~ CKE1	6.0	Inches
BA0 ~ BA1	9.0	Inches	$\overline{CS0}$ ~ $\overline{CS3}$	4.0	Inches
$\overline{RAS}$	9.0	Inches	DQM0 ~ DQM7	3.0	Inches
$\overline{CAS}$	9.0	Inches	DQ0 ~ DQ63	2.0	Inches
$\overline{WE}$	9.0	Inches	CB0 ~ CB7	2.0	Inches

DC CHARACTERISTICS

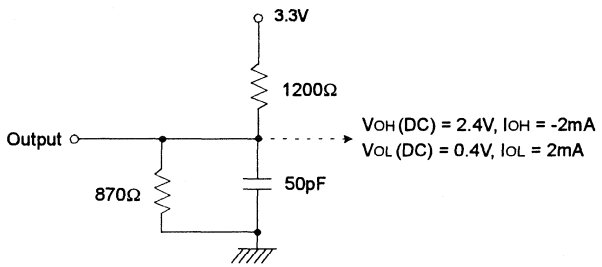
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -10	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		765	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		18	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		18		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		216	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		108		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		36	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		36		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		360	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		180	mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	855	mA	1
			2	810		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		2,250	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		18	mA	

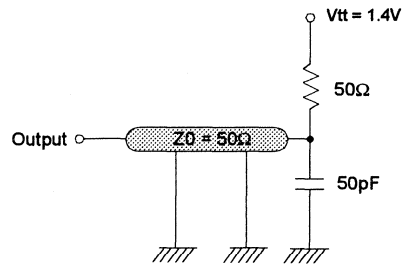
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-10		
Row active to row active delay		tRRD(min)	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	ns	1
Row precharge time		tRP(min)	24	ns	1
Row active time		tRAS(min)	50	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	80	ns	1
Last data in to row precharge		tRDL(min)	12	ns	2
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tSAC		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	tOH	3		ns	1,2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tSS	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	1
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
		Entry		L									3
	Self refresh	Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_8$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

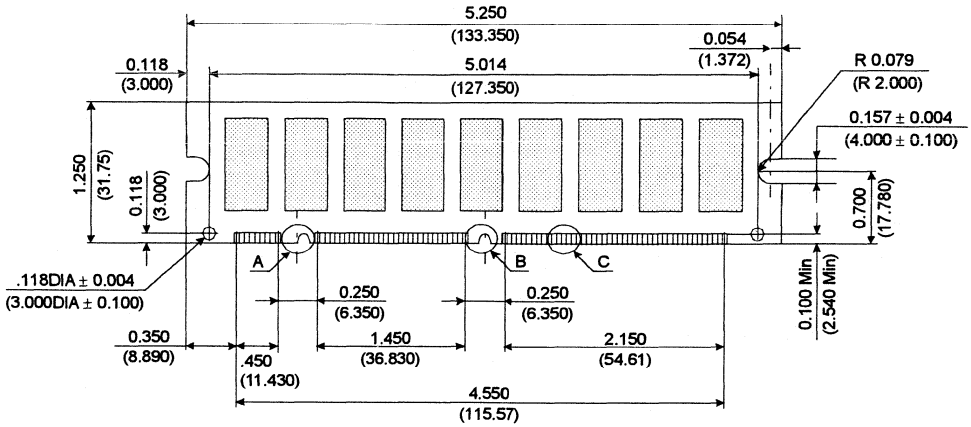
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

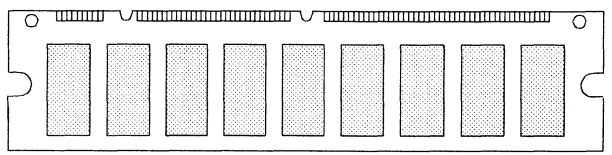
6. Burst stop command is valid at every burst length.

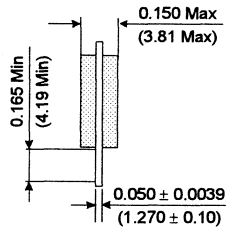
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

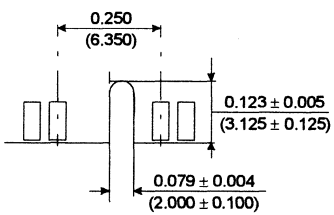
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

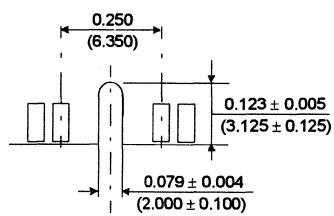




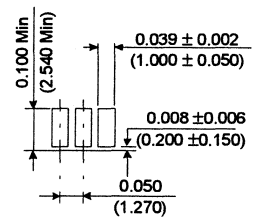




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : K4S640832C

M374S1623CTL-C10

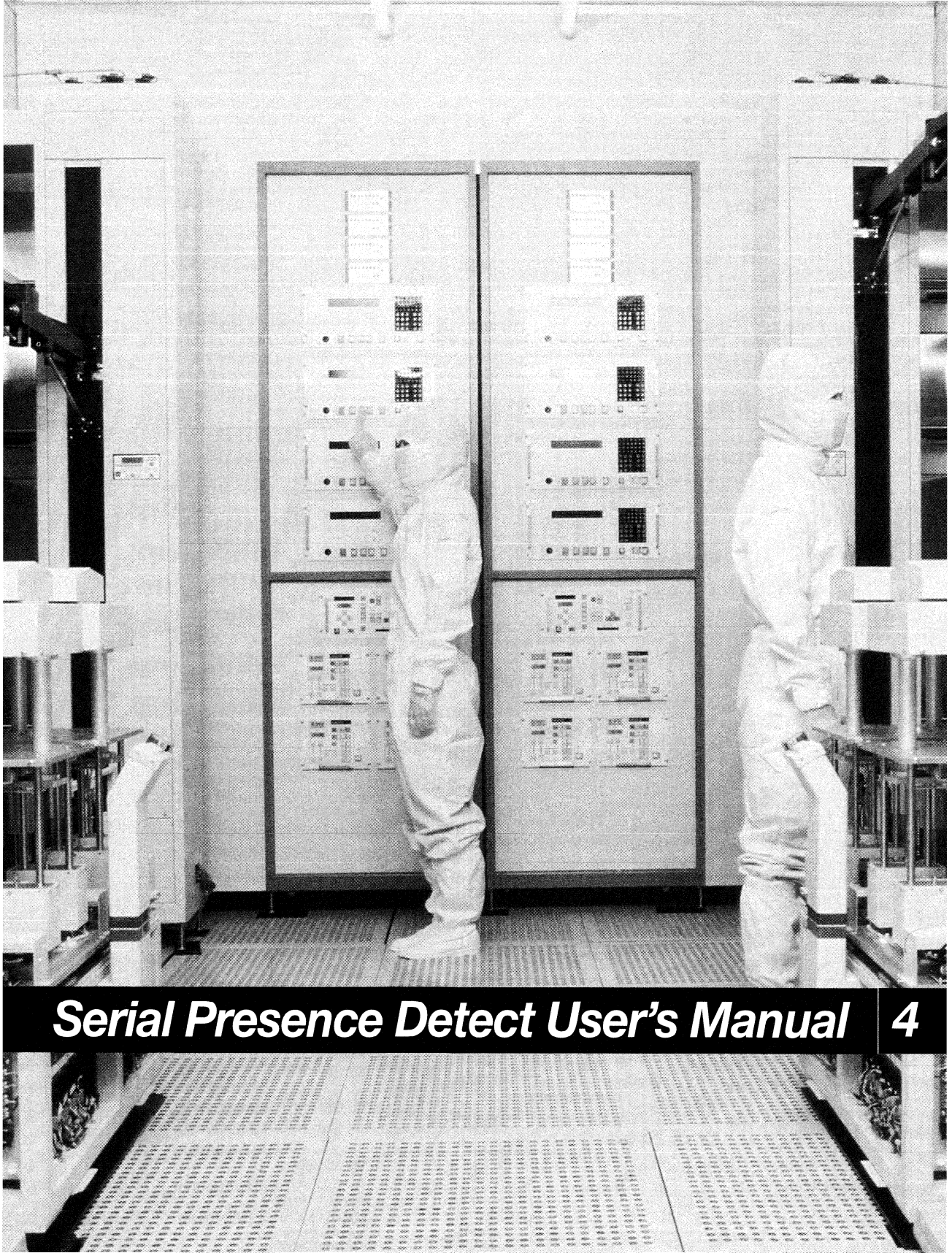
- Organization : 16Mx72
- Composition : 8Mx8 *18
- Used component part # : K4S640832C-TC10
- # of banks in module : 2 banks
- # of banks in component : 4 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module banks on this assembly	2 banks	02h	
6	Data width of this assembly	72 bits	48h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	x8	08h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	2 banks of 64MB	10h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	FFh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	7	37h	
77	..... Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	..... Manufacturer part # (Module depth)	6	36h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	C	43h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	L	4Ch	
86	Manufacturer part # (Hyphen)	"-"	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	L	4Ch	
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)	43h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

NOTES



Serial Presence Detect User's Manual 4

SDRAM Registered DIMM & Unbuffered DIMM (168pin) & SODIMM (144pin) SPD Specification for 100 MHz

Part I : General Information

General Description

This appendix describes the Presence Detects for Synchronous DRAM modules. These PD are those referenced in the SPD standard as "Specific Features". The following PD fields will occur, in the order presented, at the point in the standard where the Specific Features are referenced ; that is, after the identification of the Fundamental memory type and before identification of whether there is any Super-srt Features presented.

Address Map

The following is the SPD address map for Synchronous DRAM. It describes where the individual LUT-Entries will be held in the serial EEPROM ;

Byte #	Function Described	Function Supported	Note
0	# of Bytes written into serial memory at module manufacturer	128 Bytes	1
1	Total # of Bytes of SPD memory device	256 Bytes (2K bit)	2
2	Fundamental memory type	SDRAM	
3	# of Row address on this assembly	*	3
4	# of Column address on this assembly	*	3
5	# of Module Rows on this assembly	*	3
6	Data width of this assembly	*	3
7	... Data width of this assembly (Continued)	*	3
8	Voltage interface standard of this assembly	LVTTL	
9	SRAM cycle time from clock @CAS latency of 3	*	3
10	SRAM access time from clock @CAS latency of 3	*	3
11	DIMM configuration type	*	3
12	Refresh rate & type	15.625us, support self refresh	
13	Primary SDRAM width	*	3
14	Error checking SDRAM width	*	3
15	Minimum clock delay for back-to-back random column address	tCCD = 1 CLK	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	
17	SDRAM device attributes : # of banks on SDRAM device	*	3
18	SDRAM device attributes : CAS latency	*	3
19	SDRAM device attributes : CS latency	0 CLK	
20	SDRAM device attributes : Write latency	0 CLK	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing (RFU)	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all & auto precharge	
23	SDRAM cycle time @CAS latency of 2	*	3
24	SDRAM access time @CAS latency of 2	*	3
25	SDRAM cycle time @CAS latency of 1	*	3
26	SDRAM access time @CAS latency of 1	*	3

Byte #	Function Described	Function Supported	Note
27	Minimum row precharge time (=tRP)	*	3
28	Minimum row active to row active delay (=tRRD)	*	3
29	Minimum RAS to CAS delay (=RCD)	*	3
30	Minimum activate to precharge time (=tRAS)	*	3
31	Module Row density	*	3
32 ~ 61	Superset information (may be used in future)	-	4
62	SPD data revision code	Current release Intel spd 1.2A	
63	Checksum for Bytes 0 ~ 62	*	3
64 ~ 71	Manufacturer JEDEC ID code	Samsung	
72	Manufacturing location	Onyang Korea	
73 ~ 90	Manufacturer part #	*	3
91 ~ 92	Manufacturer revision code	*	3
93	Manufacturing date (Week)	-	5
94	Manufacturing date (Year)	-	5
95 ~ 98	Assembly serial #	-	4
99 ~ 125	Manufacturer specific data	-	6
126	Intel Specification for frequency	100MHz	
127	Intel Specification CAS # Latency Support	Support CL=2 & 3 for 100MHz	
128 +	Unused storage locations	-	6

<Note>

1. This will be 128 Bytes for Synchronous DRAM.
2. This will be typically 256 Bytes.
3. This field is different, module by module. So, if more detail information is needed Individual SPD Datasheets.
4. These Bytes are programmed by Samsung' s own Assembly Serial # system. All modules may have different unique serial #.
5. These Bytes are programmed by code of Date Week & Date Year with BCD format .
6. These bytes are Undefined and can be used for Samsung 's own purpose.

Part II : Detail Byte Assignments

Byte 0 : # of Bytes written into serial memory at module manufacturer

This field describes the total number of Bytes used by the module manufacturer for the SPD data and any(optional) specific supplier information. The byte count includes the fields for all required and optional data ;

Number of Bytes	Byte 0
Undefined	00h
1 Bytes	01h
2 Bytes	02h
:	:
128 Bytes	80h
. . .	. . .
256 Bytes	FFH

Byte 1 : Total # of Bytes of SPD memory device

This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes serial memory densities(in Bytes) along with the corresponding descriptor ;

SPD memory size	Byte 1
RFU	00h
2 Bytes	01h
4 Bytes	02h
8 Bytes	03h
:	:
128 Bytes	07h
256 Bytes	08h
:	:
8192 Bytes	0Dh

Byte 2 : Fundamental memory type

This field describes the fundamental memory type (or technology) implemented on the module ;

fundamental memory type	Byte 2
Reserved	00h
Standard FPM DRAM	01h
EDO DRAM	02h
. . .	. . .
SDRAM	04h
. . .	. . .

Byte 3 : # of row address on this assembly

This field describes the number of row address bits in the SDRAM array. That is, the number of row address bits does not include the bank selects(BA0, BA1). If the module has only one bank or if the module has two banks of the same size and organization, then bits 3:0 describe the number of row address bits and bits 7:4 are 0. If the module has two banks with different size/organization, then bits 3:0 describe the row addressing for bank1 and bits 7:4 describe the row addressing for bank2 ;

# of row address	Bits 3:0	Bits 7:4
Undefined	0h	0h
:	:	:
10	Ah	Ah
11	Bh	Bh
12	Ch	Ch
13	Dh	Dh
14	Eh	Eh
15	Fh	Fh

Byte 4 : # of column address on this assembly

This field describes the number of column address bits in the SDRAM array. That is, the number of column address bits does not include the bank selects(BA0, BA1). If the module has only one bank or if the module has two banks of the same size and organization, then bits 3:0 describe the number of column address bits and bits 7:4 are 0. If the module has two banks with different size/organization, then bits 3:0 describe the column addressing for bank1 and bits 7:4 describe the column addressing for bank2 ;

# of column address	Bits 3:0	Bits 7:4
Undefined	0h	0h
:	:	:
7	7h	7h
8	8h	8h
9	9h	9h
10	Ah	Ah
11	Bh	Bh
:	:	:
15	Fh	Fh

Byte 5 : # of module Rows on this assembly

This field describes the number of module banks on the SDRAM module ;

# of module bank	Byte 5
Undefined	00h
1	01h
2	02h
:	:
254	FEh
255	FFH

Byte 6 & 7 : Data width of this assembly

Byte 6 & 7 are used to designate the data width of the module. The data width is presented as a 16bit word ; bit 0 of byte 6 becomes the LSB of the 16bit width identifier and bit 7 of byte 7 becomes MSB. Consequently, if the module has a data width less than 255 bits wide, byte 7 will be "00h". If the data width is 256 bits or higher, byte 7 is used in conjunction with byte 6 to designate the total module width ;

# of row address	Byte 6	Byte 7
Undefined	00h	00h
:	:	:
32	20h	00h
36	24h	00h
:	:	:
64	40h	00h
72	48h	00h
80	50h	00h
:	:	:
256	00h	01h

Byte 8 : Voltage interface standard of this assembly

This field describes the SDRAM module voltage & interface ;

Voltage & interface	Byte 8
5.0V/TTL	00h
LVTTL	01h
HSTL 1.5V	02h
SSTL 3.3V	03h
SSTL 2.5V	04h
TBD	05h
TBD	06h
:	:
New table	FFh

Byte 9 : SDRAM cycle time from clock @CAS latency of 3

This field describes the total minimum cycle time(clock period) for the SDRAM. For example, if the SDRAM supports CAS latency of 3, 2 and 1(as indicated in byte 18), this byte defines tCC for CAS latency of 3. The byte is broken into two nibbles : the higher order nibble(bit4 ~7) designates the cycle time to a granularity of 1ns ; the value presented by the lower order nibble has a granularity of 1/10ns and is added to the value of the higher nibble. Samsung SDRAM has the different cycle time @CAS latency of 3, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 10 : SDRAM access time from clock @CAS latency of 3

This field describes the total maximum clock to data out for the SDRAM. For example, if the SDRAM supports CAS latency 3, 2 and 1 (as indicated in byte 18), this byte defines tSAC for CAS latency of 3. The byte is broken into two nibbles : the higher order nibble(bit4 ~7) designates the access time to a granularity of 1ns ; the value presented by the lower order nibble has a granularity of 1/10ns and is added to the value of the higher nibble. Samsung SDRAM has the different access time @CAS latency of 3, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 11 : DIMM configuration type

This field describes the module error detection and correction scheme ;

Error detect & correct	Byte 11
None	00h
Parity	01h
ECC	02h
TBD	03h
. . .	. . .
TBD	FFh

Byte 12 : Refresh rate & type

This field describes the module's refresh rate and type. The bit 7 is especially used for self refresh flag ; if SDRAM supports self refresh, bit 7 is "1" and if not, bit 7 is "0" ;

Refresh rate/type	Byte 12
Normal(15.625us)	00h
Reduced (.5x) 7.8us	02h
:	:
Self refresh	
Normal(15.625us)	80h
Reduced (.5x) 7.8us	82h
:	:
Extended(2x) ... 31.3us	83h
:	:
TBD	FFh

Byte 13 : Primary SDRAM width

This field describes the data width of the primary SDRAM components used on the module. The primary SDRAM is that which is used for data ;

SDRAM data width	Byte 13
Undefined	00h
.	.
4	04h
.	.
8	08h
.	.
16	10h
.	.
32	20h
.	.
127	7Fh

Byte 14 : Error checking SDRAM width

If the module incorporates error checking and if the primary data SDRAM does not include these bits ; i.e. there are separate error checking SDRAMs, then the error checking SDRAM width is expressed in this byte ;

ECC SDRAM data width	Byte 14
Undefined	00h
.	.
4	04h
.	.
8	08h
.	.
16	10h
.	.
32	20h
.	.
127	7Fh

Byte 15 : Minimum clock delay for back-to-back random column addresses

Number of clocks	Byte 15
Undefined	00h
1	01h
2	02h
. . .	. . .
256	FFh

Byte 16 : SDRAM device attributes : Burst lengths supported

This field describes various burst lengths supported. If the burst length is supported, then the corresponding bit is "1". Samsung value for this field is "8Fh" because the burst lengths of 1, 2, 4, 8 and full page are supported ;

Burst length supported	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	Full page	TBD	TBD	TBD	8	4	2	1

Byte 17 : SDRAM device attributes : Number of banks on SDRAM device

This field describes the number of banks internal to the SDRAM devices ;

# of banks in component	Byte 17
Undefined	00h
1	01h
2	02h
.	.
4	04h
.	.
256	FFh

Byte 18 : SDRAM device attributes : CAS latency

This field describes which CAS latencies are supported for the module. If the bit is "1", then that CAS latency is supported ;

CAS latency	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	TBD	7	6	5	4	3	2	1

Byte 19 : SDRAM device attributes : CS latency

This field describes which CS latencies are acceptable for the module. If the bit is "1", then that CS latency is supported. Samsung value for this field is "01h" because CS latency of 0 is supported ;

CAS latency	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	TBD	6	5	4	3	2	1	0

Byte 20 : SDRAM device attributes : WE latency

This field describes which WE latencies are accptable for the module. If the bit is "1", then that WE latency is supported. Samsung value for this field is "01h" because WE latency of 0 is supported ;

WE latency	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	TBD	6	5	4	3	2	1	0

Byte 21 : SDRAM module attributes: General

This field describes various aspects of the module. If the aspect is TRUE, then the corresponding bit is "1". Samsung value for this field is "00h" ;

Module attributes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	TBD	Redundant addressing	Differential CLK input	Registered DQMB input	Buffered DQMB input	On-card PLL	Registered Add/Cntr input	Buffered Add/Cntr input

Byte 22 : SDRAM device attributes : General

This field describes various aspects of the SDRAMs on the module. If the aspect is TRUE, then the corresponding bit is "1". Samsung value for this field is "0Eh" ;

Device attributes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	TBD	TBD	Upper Vdd tolerance 0=10% 1=5%	Lower Vdd tolerance 0=10% 1=5%	Support BRSW	Support precharge all	Support auto precharge	Support early RAS precharge

Byte 23 : SDRAM cycle time from clock @CAS latency of 2

This field describes the total minimum cycle time(clock period) for the SDRAM. For example, if the SDRAM supports CAS latency of 3, 2 and 1 (as indicated in byte 18), this byte defines tCC for CAS latency of 2. The byte is broken into two nibbles : the higher order nibble(bit4 ~ 7) designates the cycle time to a granularity of 1ns ; the value presented by the lower order nibble has a granularity of 1/10ns and is added to the value of the higher nibble. Samsung SDRAM has the different cycle time @CAS latency of 2, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 24 : SDRAM access time from clock @CAS latency of 2

This field describes the total maximum clock to data out for the SDRAM. For example, if the SDRAM supports CAS latency of 3, 2 and 1 (as indicated in byte 18), this byte defines tSAC for CAS latency of 2. The byte is broken into two nibbles : the higher order nibble(bit4 ~ 7) designates the access time to a granularity of 1ns ; the value presented by the lower order nibble has a granularity of 1/10ns and is added to the value of the higher nibble. Samsung SDRAM has the different cycle time @CAS latency of 2, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 25 : SDRAM cycle time from clock @CAS latency of 1

This field describes the total minimum cycle time(clock period) for the SDRAM. For example, if the SDRAM supports CAS latency of 3, 2 and 1 (as indicated in byte 18), this byte defines tCC for CAS latency of 1. The byte is broken into two pieces : the higher order piece(bit2 ~ 7) designates the cycle time to a granularity of 1ns ; the value presented by the lower order piece has a granularity of 1/4ns and is added to the value of the higher piece. Samsung SDRAM has the different cycle time @CAS latency of 1, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 26 : SDRAM access time from clock @CAS latency of 1

This field describes the total maximum clock to data out for the SDRAM. For example, if the SDRAM supports CAS latency of 3, 2 and 1 (as indicated in byte 18), this byte defines tSAC for CAS latency of 1. The byte is broken into two pieces : the higher order piece(bit2 ~ 7) designates the access time to a granularity of 1ns ; the value presented by the lower order piece has a granularity of 1/4ns and is added to the value of the higher piece. Samsung SDRAM has the different access time @CAS latency of 1, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 27 : Minimum row precharge time (=tRP)

Bit 0 ~ 5 of this byte describe the precharge to active minimum(=tRP) using 1ns granularity. Bits 7 and 6 are reserved for future use. Samsung SDRAM has the different value, generation by generation and binning by binning. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 28 : Minimum row active to row active delay (=tRRD)

Bit 0 ~ 5 of this byte describe the minimum row activate to row activate delay(=tRRD) using 1ns granularity. Bits 7 and 6 are reserved for future use. Samsung SDRAM has the different value, generation by generation and binning by binning. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 29 : Minimum RAS to CAS delay (=tRCD)

Bit 0 ~ 5 of this byte describe the minimum RAS to CAS delay(=tRCD) using 1ns granularity. Bits 7 and 6 are reserved for future use. Samsung SDRAM has the different value, generation by generation and binning by binning. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 30 : Minimum activate to precharge time (=tRAS)

Bit 0 ~ 5 of this byte describe the minimum activate to precharge time(=tRAS) using 1ns granularity. Bits 7 and 6 are reserved for future use. Samsung SDRAM has the different value, generation by generation and binning by binning. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 31 : Module Row density

This field describes the density of each physical Row on the SDRAM DIMM. This field will have at least one bit to "1" to represent at least one Row density. If there are more than one Row on the module(as indicated in byte 5) and they have the same density, then only one bit is set in this field. If the module has more than one Row of different sizes, then more than one bit will be set for each density represented ;

Module Row density	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If YES, the bit is "1"	512MByte	256MByte	128MByte	64MByte	32MByte	16MByte	8MByte	4MByte

Byte 32~35 : Input setup and hold time for 100MHz system ferquency

Definition of these bytes are in JEDEC Ballot process. The proposed data structure is as defined:

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Posiive/ Negaive	Setup	Time	in ns	Setup	Time	in tenth	of a ns
1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

Bit 7 = 0 defines a positive setup time w.r.t. the clock
Bit 7 = 1 defines a negative setup time w.r.t. the clock
Bit 6-4 = Defines the setup time in ns.
Bit 3-0 = Defines the setup time in tenth of a ns.

Some encoded values in the table

bit 7	bit 6	bit 5	bit4	bit3	bit2	bit 1	bit 0	comment
0	0	0	0	0	0	0	0	0 ns
0	0	0	0	0	0	0	1	0.1ns
0	0	0	0	0	0	1	0	0.2ns
.	.	.	.	.	.	.	.	
0	0	0	0	1	0	0	1	0.9ns
0	0	0	1	0	0	0	0	1.0ns
0	0	0	1	0	0	0	1	1.1ns
.	.	.	.	.	.	.	.	
0	0	0	1	1	0	0	1	1.9ns
0	0	1	0	0	0	0	0	2.0ns
.	.	.	.	.	.	.	.	
0	1	1	1	0	0	0	0	7.0ns
.	.	.	.	.	.	.	.	
0	1	1	1	1	0	0	1	7.9ns
1	0	0	0	0	0	0	1	-0.1ns
1	0	0	0	0	0	1	0	-0.2ns
.	.	.	.	.	.	.	.	
1	0	0	0	1	0	0	1	-0.9ns
1	0	0	1	0	0	0	0	-1.0ns
1	0	0	1	0	0	0	1	-1.1ns
.	.	.	.	.	.	.	.	
1	0	0	1	1	0	0	1	-1.9ns
1	0	1	0	0	0	0	0	-2.0ns
.	.	.	.	.	.	.	.	
1	1	1	1	0	0	0	0	-0.7ns
.	.	.	.	.	.	.	.	
1	1	1	1	1	0	0	1	-7.9ns
x	x	x	x	1	0	1	0	RFU
.	.	.	.	.	.	.	.	RFU
x	x	x	x	1	1	1	1	RUF

Byte 32 : Command and Address signal input setup time.

This byte describes the input setup time w.r.t the rising edge of the clock input. Both positive and negative setup times are supported.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Positive/ Negative	Setup	Time	in ns	Setup	Time	in tenth	of a ns
1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

Bit7= 0 Defines a positive setup time w.r.t the clock.
Bit7= 1 Defines a negative setup time w.r.t the clock.
Bit 6-4= Defines a setup time in ns.
Bit 3-0= Defines a setup time in tenth of a ns.

Byte 33 : Command and Address signal input hold time.

This byte describes the input setup time w.r.t the rising edge of the clock input. Both positive and negative setup times are supported.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Positive/ Negative	Hold	Time	in ns	Hold	Time	in tenth	of a ns
1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

Bit7= 0 Defines a positive Hold time w.r.t the clock.
Bit7= 1 Defines a negative Hold time w.r.t the clock.
Bit 6-4= Defines a Hold time in ns.
Bit 3-0= Defines a Hold time in tenth of a ns.

Byte 34 : Data signal input setup time.

This byte describes the input setup time w.r.t the rising edge of the clock input. Both positive and negative setup times are supported.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Positive/ Negative	Setup	Time	in ns	Setup	Time	in tenth	of a ns
1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

Bit7= 0 Defines a positive setup time w.r.t the clock.
Bit7= 1 Defines a negative setup time w.r.t the clock.
Bit 6-4= Defines a setup time in ns.
Bit 3-0= Defines a setup time in tenth of a ns.

Byte 35 : Data signal input hold time.

This byte describes the input setup time w.r.t the rising edge of the clock input. Both positive and negative setup times are supported.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Positive/ Negative	Hold	Time	in ns	Hold	Time	in tenth	of a ns
1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

Bit7= 0 Defines a positive Hold time w.r.t the clock.
Bit7= 1 Defines a negative Hold time w.r.t the clock.
Bit 6-4= Defines a Hold time in ns.
Bit 3-0= Defines a Hold time in tenth of a ns.

Byte 36 ~ 61 : Superset information (may be used in future)

This field are reserved for superset information. Currently, these fields are programmed by "00h" because the standardization for these fields are not fixed yet.

Byte 62 : SPD data revision code

This field identifies the SDRAM DIMM SPD data revision to which the module conforms. Currently, this field is programmed by "01h"

SPD data revision code	Byte 62
Initial release	00h
2nd edition	01h
.	.
Current Release Nov 97	12h
. .	. .

Byte 63 : Checksum for Bytes 0 ~ 62

This field is the checksum for Bytes 0 through 62. Currently, this byte contains the value of the low 8bits of arithmetic sum of Bytes 0 through byte 62.

Byte 64 ~ 71 : Manufacturer JEDEC ID code

This field describes the manufacturer JEDEC ID code per EIA/JEP106-E. The unique code for Samsung is "CBh" only for byte64 and another Bytes, Bytes 65 ~ 71 are programmed by "00h" ;

JEDEC ID code	Byte 64	Byte 65	Byte 66	Byte 67	Byte 68	Byte 69	Byte 70	Byte 71
Samsung	CEh	00h	00h	00h	00h	00h	00h	00h

Byte 72 : Manufacturing location

This field identifies the manufacturing location and is programmed by binary code not ASCII ;

Manufacturing location	Byte 72
Kiheung Korea	00h
Onyang Korea	01h
. . .	. . .

Byte 73 ~ 90 : Manufacturer part # (ASCII code)

This fields describe the manufacturer part number and are programmed by ASCII code not binary.

Byte 73 : Samsung memory (ASCII code)

Samsung Korea	Byte 73
K	4Bh
. . .	. . .

Byte 74 : Samsung memory (ASCII code)

Samsung Korea	Byte 74
M	4Dh
. . .	. . .

Byte 75 : Samsung module (ASCII code)

Samsung Korea	Byte 75
M	4Dh
. . .	. . .

Byte 76 : Memory type (ASCII code)

Memory type	Byte 76
3 (168 or 200pin DIMM)	33h
4 (144pin SODIMM)	34h
. . .	. . .

Byte 77 ~ 79 : Data bits (ASCII code)

Data bits	Byte 77	Byte 78	Byte 79
50(x72, 168pin, register & SPD , Intel)	20h	35h	30h
64(x64, 168pin, SODIMM. SPD)	20h	36h	34h
:	:	:	:
66(x64, 168pin, unbuffered & SPD)	20h	36h	36h
:	:	:	:
74(x72, 168pin, unbuffered & SPD)	20h	37h	34h
75(x72, 168pin, register, PLL & SPD, JEDEC)	20h	37h	35h
:	:	:	:
77(x72, 168pin, register, PLL & SPD , Intel)	20h	37h	37h
:	:	:	:
90 (x72, 168pin, register, PLL & SPD, PC133)	20h	39h	30h

Byte 80 : Mode & operating voltage (ASCII code)

Mode & operating voltage	Byte 80
F (EDO 3.3V)	46h
S (Sync. DRAM)	53h
.	.
.	.
.	.

Byte 81 ~ 82 : Module density (ASCII code)

Module density	Byte 81	Byte 82
1M	20h	31h
2M	20h	32h
4M	20h	34h
8M	20h	38h
16M	31h	36h
32M	33h	32h
.	.	.
.	.	.

Byte 83 : Refresh, # of banks in Comp. & interface (ASCII code)

Features	Byte 83
0 (4K ref., 2banks, LVTTL)	30h
1 (2K ref., 2banks, LVTTL)	31h
2 (4K ref., 4banks, LVTTL)	32h
.	.
.	.
5 (8K ref., 4banks, LVTTL)	35h
6 (16K ref., 4banks, LVTTL)	36h
.	.
.	.

Byte 84 : Composition component (ASCII code)

Composition component	Byte 84
0 (x4)	30h
3 (x8)	33h
4 (x16)	34h
.	.
.	.
.	.

Byte 85 : Component revision (ASCII code)

Component revision	Byte 85
Blank (Mother die)	20h
A (1st Rev.)	41h
B (2nd Rev.)	42h
C (3rd Rev.)	43h
D (4rd Rev.)	44h
. . .	. . .

Byte 86 : Package type (ASCII code)

Package type	Byte 86
T (400mil TSOP II - forward)	54h

Byte 87 : PCB revision (ASCII code)

This field is used for the expression of PCB height and distinction between new JEDEC DIMM & old JEDEC DIMM. The marked by "N" refers to 16M SDRAM based 168pin unbuffered DIMM only and "L" refers to Intel 1.0 compliant 168pin unbuffered DIMM;

PCB revision	Byte 87
Blank	20h
L	4Ch
N	4Eh
1	31h
2	32h
3	33h
. .	. .

Byte 88 : Hyphen (ASCII code)

Hyphen	Byte 88
" - "	2Dh

Byte 89 : Power (ASCII code)

Power	Byte 89
G (Auto & self Ref., normal power)	47h
F (Auto & self Ref., low power)	46h

Byte 90 : Minimum cycle time (ASCII code)

Minimum cycle time	Byte 90
A (7.5ns =133MHz,CL3)	41h
8 (8ns=125MHz, CL3)	38h
. .	. .
H (10ns=100MHz, CL2)	48h
. .	. .
L (10ns=100MHz, CL3)	4Ch
. .	. .
0 (10ns=100MHz, CL3)	30h

Byte 91 : Manufacturer revision code for PCB (ASCII code)

This field is refered to the module PCB revision and has the same programming code with byte 87.

Byte 92 : Manufacturer revision code for component (ASCII code)

This field is refered to the component revision and has the same programming code with byte 85.

Byte 93 : Manufacturing date ; Week

This field describes manufacturing week and programmed with BCD format.

Byte 94 : Manufacturing date ; Year

This field describes manufacturing year and programmed with BCD format.

Byte 95 ~ 98 : Assembly serial number (Binary code)

These fields describe assembly serial number. But, all of the Samsung modules are controlled by another way, not assembly serial #. Currently, this field is programmed by "00h".

Byte 99 ~ 125 : Manufacturer specific data (may be used in future)

These bytes are Undefined and can be used for Samsung 's own purpose.

Byte 126 : Intel Specification for frequency

System frequency	Byte 126
66MHz	66h
100MHz	64h

Byte 127 : Intel Specification details for 100MHz Support

This byte defines the SDRAM component and Clock interconnection details for the DIMMs as defined:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLK0	CLK1	CLK2	CLK3	Juncion temp	CAS Latency = 3	CAS Latency = 2	Intel AP
1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

Bit7 = 1: CLK0 is connected on the DIMM
Bit7 = 0: CLK0 is not connected on the DIMM
Bit6 = 1: CLK1 is connected on the DIMM
Bit6 = 0: CLK1 is not connected on the DIMM
Bit5 = 1: CLK2 is connected on the DIMM
Bit5 = 0: CLK2 is not connected on the DIMM
Bit4 = 1: CLK3 is connected on the DIMM
Bit4 = 0: CLK3 is not connected on the DIMM
Bit3 = 1: 100 °C junction temp
Bit3 = 0: 90 °C junction temp
Bit2 and Bit1 = 1: CL3 and CL2 support as shown

Performance Grade	Hex Value (Bits 2-1)
CAS Latency 3	04
CAS Latency 2	06

Bit0 = 1: It supports Intel defined Concurrent Auto-precharge
Bit0 = 0: It does not support Intel defined Concurrent Auto-precharge

Byte 128 ~ 255 : Unused storage locations

These bytes are Undefined and can be used for Samsung 's own purpose.

NOTES

SDRAM Unbuffered DIMM(168pin) & SODIMM(144pin) SPD Specifications for 66MHz

Part I : General Information

General Description

This appendix describes the Presence Detects for Synchronous DRAM modules. These PD are those referenced in the SPD standard as "Specific Features". The following PD fields will occur, in the order presented, at the point in the standard where the Specific Features are referenced ; that is, after the identification of the Fundamental memory type and before identification of whether there is any Super-srt Features presented.

Address Map

The following is the SPD address map for Synchronous DRAM. It describes where the individual LUT-Entries will be held in the serial EEPROM ;

Byte #	Function Described	Function Supported	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	1
1	Total # of bytes of SPD memory device	256 bytes (2K bit)	2
2	Fundamental memory type	SDRAM	
3	# of row address on this assembly	*	3
4	# of column address on this assembly	*	3
5	# of module Rows on this assembly	*	3
6	Data width of this assembly	*	3
7	... Data width of this assembly	*	3
8	Voltage interface standard of this assembly	LVTTL	
9	SRAM cycle time from clock @CAS latency of 3	*	3
10	SRAM access time from clock @CAS latency of 3	*	3
11	DIMM configuration type	*	3
12	Refresh rate & type	15.625us, support self refresh	
13	Primary SDRAM width	*	3
14	Error checking SDRAM width	*	3
15	Minimum clock delay for back-to-back random column address	tCCD = 1 CLK	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	
17	SDRAM device attributes : # of banks on SDRAM device	*	3
18	SDRAM device attributes : CAS latency	*	3
19	SDRAM device attributes : CS latency	0 CLK	
20	SDRAM device attributes : Write latency	0 CLK	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing (RFU)	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all & auto precharge	
23	SDRAM cycle time @CAS latency of 2	*	3
24	SDRAM access time @CAS latency of 2	*	3
25	SDRAM cycle time @CAS latency of 1	*	3
26	SDRAM access time @CAS latency of 1	*	3

Byte #	Function Described	Function Supported	Note
27	Minimum row precharge time (=tRP)	*	3
28	Minimum row active to row active delay (=tRRD)	*	3
29	Minimum RAS to CAS delay (=RCD)	*	3
30	Minimum activate to precharge time (=tRAS)	*	3
31	Module Row density	*	3
32 ~ 61	Superset information (may be used in future)	-	4
62	SPD data revision code	2nd edition	
63	Checksum for bytes 0 ~ 62	*	3
64 ~ 71	Manufacturer JEDEC ID code	Samsung	
72	Manufacturing location	Onyang Korea	
73 ~ 90	Manufacturer part #	*	3
91 ~ 92	Manufacturer revision code	*	3
93	Manufacturing date (Week)	-	5
94	Manufacturing date (Year)	-	5
95 ~ 98	Assembly serial #	-	4
99 ~ 125	Manufacturer specific data	-	6
126	System frequency for 66MHz	66MHz	
127	CAS latency for 66MHz	Support CL=2 & 3 for 66MHz	
128 +	Unused storage locations	-	6

<Note>

1. This will be 128 bytes for Synchronous DRAM.
2. This will be typically 256 bytes.
3. This field is different, module by module. So, if more detail information is needed, see the Part III, Individual SPD Datasheets.
4. These bytes are programmed by Samsung' s own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are programmed by code of Date Week & Date Year.
6. These bytes are Undefined and can be used for Samsung 's own purpose.

Part II : Detail Byte Assignments

Byte 0 : # of bytes written into serial memory at module manufacturer

This field describes the total number of bytes used by the module manufacturer for the SPD data and any(optional) specific supplier information. The byte count includes the fields for all required and optional data ;

Number of bytes	Byte 0
Undefined	00h
1 bytes	01h
. . .	. . .
128 bytes	80h
. . .	. . .

Byte 1 : Total # of bytes of SPD memory device

This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes serial memory densities(in bytes) along with the corresponding descriptor ;

SPD memory size	Byte 1
RFU	00h
2 bytes	01h
. . .	. . .
128 bytes	07h
256 bytes	08h
. . .	. . .

Byte 2 : Fundamental memory type

This field describes the fundamental memory type (or technology) implemented on the module ;

fundamental memory type	Byte 2
Reserved	00h
Standard FPM DRAM	01h
EDO DRAM	02h
. . .	. . .
SDRAM	04h
. . .	. . .

Byte 3 : # of row address on this assembly

This field describes the number of row address bits in the SDRAM array. That is, the number of row address bits does not include the bank selects(BA0, BA1). If the module has only one bank or if the module has two banks of the same size and organization, then bits 3:0 describe the number of row address bits and bits 7:4 are 0. If the module has two banks with different size/organization, then bits 3:0 describe the row addressing for bank1 and bits 7:4 describe the row addressing for bank2 ;

# of row address	Bits 3:0	Bits 7:4
Undefined	0h	0h
:	:	:
10	Ah	Ah
11	Bh	Bh
12	Ch	Ch
13	Dh	Dh
14	Eh	Eh
:	:	:

Byte 4 : # of column address on this assembly

This field describes the number of column address bits in the SDRAM array. That is, the number of column address bits does not include the bank selects(BA0, BA1). If the module has only one bank or if the module has two banks of the same size and organization, then bits 3:0 describe the number of column address bits and bits 7:4 are 0. If the module has two banks with different size/organization, then bits 3:0 describe the column addressing for bank1 and bits 7:4 describe the column addressing for bank2 ;

# of column address	Bits 3:0	Bits 7:4
Undefined	0h	0h
:	:	:
7	7h	7h
8	8h	8h
9	9h	9h
10	Ah	Ah
11	Bh	Bh
:	:	:

Byte 5 : # of module Rows on this assembly

This field describes the number of module banks on the SDRAM module ;

# of module bank	Byte 5
Undefined	00h
1	01h
2	02h
:	:

Byte 6 & 7 : Data width of this assembly

Byte 6 & 7 are used to designate the data width of the module. The data width is presented as a 16bit word ; bit 0 of byte 6 becomes the LSB of the 16bit width identifier and bit 7 of byte 7 becomes MSB. Consequently, if the module has a data width less than 255 bits wide, byte 7 will be "00h". If the data width is 256 bits or higher, byte 7 is used in conjunction with byte 6 to designate the total module width ;

# of row address	Byte 6	Byte 7
Undefined	00h	00h
:	:	:
32	20h	00h
36	24h	00h
:	:	:
64	40h	00h
72	48h	00h
80	50h	00h
:	:	:

Byte 8 : Voltage interface standard of this assembly

This field describes the SDRAM module voltage & interface ;

Voltage & interface	Byte 8
5.0V/TTL	00h
LVTTL	01h
HSTL 1.5V	02h
SSTL 3.3V	03h
SSTL 2.5V	04h
TBD	05h
TBD	06h
:	:
New table	FFh

Byte 9 : SDRAM cycle time from clock @CAS latency of 3

This field describes the total minimum cycle time(clock period) for the SDRAM. For example, if the SDRAM supports CAS latency of 3, 2 and 1(as indicated in byte 18), this byte defines tCC for CAS latency of 3. The byte is broken into two nibbles : the higher order nibble(bit4 ~7) designates the cycle time to a granularity of 1ns ; the value presented by the lower order nibble has a granularity of 1/10ns and is added to the value of the higher nibble. Samsung SDRAM has the different cycle time @CAS latency of 3, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 10 : SDRAM access time from clock @CAS latency of 3

This field describes the total maximum clock to data out for the SDRAM. For example, if the SDRAM supports CAS latency 3, 2 and 1 (as indicated in byte 18), this byte defines tSAC for CAS latency of 3. The byte is broken into two nibbles : the higher order nibble(bit4 ~7) designates the access time to a granularity of 1ns ; the value presented by the lower order nibble has a granularity of 1/10ns and is added to the value of the higher nibble. Samsung SDRAM has the different access time @CAS latency of 3, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 11 : DIMM configuration type

This field describes the module error detection and correction scheme ;

Error detect & correct	Byte 11
None	00h
Parity	01h
ECC	02h
. . .	. . .
TBD	FFh

Byte 12 : Refresh rate & type

This field describes the module's refresh rate and type. The bit 7 is especially used for self refresh flag ; if SDRAM supports self refresh, bit 7 is "1" and if not, bit 7 is "0" ;

Refresh rate/type	Byte 12
Normal(15.625us)	00h
Reduced (.5x) 7.8us	02h
. .	. .
Self refresh	
Normal(15.625us)	80h
Reduced (.5x) 7.8us	82h
. .	. .
Extended(2x) ... 31.3us	83h

Byte 13 : Primary SDRAM width

This field describes the data width of the primary SDRAM components used on the module. The primary SDRAM is that which is used for data ;

SDRAM data width	Byte 13
Undefined	00h
.	.
4	04h
.	.
8	08h
.	.
16	10h
.	.
32	20h
.	.
127	7Fh

Byte 14 : Error checking SDRAM width

If the module incorporates error checking and if the primary data SDRAM does not include these bits ; i.e. there are separate error checking SDRAMs, then the error checking SDRAM width is expressed in this byte ;

ECC SDRAM data width	Byte 14
Undefined	00h
.	.
4	04h
.	.
8	08h
.	.
16	10h
.	.
32	20h
.	.
127	7Fh

Byte 15 : Minimum clock delay for back-to-back random column addresses

Number of clocks	Byte 15
Undefined	00h
1	01h
2	02h
. . .	. . .
256	FFh

Byte 16 : SDRAM device attributes : Burst lengths supported

This field describes various burst lengths supported. If the burst length is supported, then the corresponding bit is "1". Samsung value for this field is "8Fh" because the burst lengths of 1, 2, 4, 8 and full page are supported ;

Burst length supported	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	Full page	TBD	TBD	TBD	8	4	2	1

Byte 17 : SDRAM device attributes : Number of banks on SDRAM device

This field describes the number of banks internal to the SDRAM devices ;

# of banks in component	Byte 17
Undefined	00h
1	01h
2	02h
.	.
4	04h
.	.
256	FFh

Byte 18 : SDRAM device attributes : CAS latency

This field describes which CAS latencies are supported for the module. If the bit is "1", then that CAS latency is supported ;

CAS latency	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	TBD	7	6	5	4	3	2	1

Byte 19 : SDRAM device attributes : CS latency

This field describes which CS latencies are acceptable for the module. If the bit is "1", then that CS latency is supported. Samsung value for this field is "01h" because CS latency of 0 is supported ;

CAS latency	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	TBD	6	5	4	3	2	1	0

Byte 20 : SDRAM device attributes : WE latency

This field describes which WE latencies are accptable for the module. If the bit is "1", then that WE latency is supported. Samsung value for this field is "01h" because WE latency of 0 is supported ;

WE latency	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	TBD	6	5	4	3	2	1	0

Byte 21 : SDRAM module attributes: General

This field describes various aspects of the module. If the aspect is TRUE, then the corresponding bit is "1". Samsung value for this field is "00h" ;

Module attributes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	TBD	redundant addressing	differential CLK input	registered DQMB input	buffered DQMB input	On-card PLL	registered Add/Cntr input	buffered Add/Cntr input

Byte 22 : SDRAM device attributes : General

This field describes various aspects of the SDRAMs on the module. If the aspect is TRUE, then the corresponding bit is "1". Samsung value for this field is "0Eh" ;

Device attributes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	TBD	TBD	upper Vdd tolerance 0=10% 1=5%	lower Vdd tolerance 0=10% 1=5%	support BRSW	support precharge all	support auto precharge	support early RAS precharge

Byte 23 : SDRAM cycle time from clock @CAS latency of 2

This field describes the total minimum cycle time(clock period) for the SDRAM. For example, if the SDRAM supports CAS latency of 3, 2 and 1 (as indicated in byte 18), this byte defines tCC for CAS latency of 2. The byte is broken into two nibbles : the higher order nibble(bit4 ~ 7) designates the cycle time to a granularity of 1ns ; the value presented by the lower order nibble has a granularity of 1/10ns and is added to the value of the higher nibble. Samsung SDRAM has the different cycle time @CAS latency of 2, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 24 : SDRAM access time from clock @CAS latency of 2

This field describes the total maximum clock to data out for the SDRAM. For example, if the SDRAM supports CAS latency of 3, 2 and 1 (as indicated in byte 18), this byte defines tSAC for CAS latency of 2. The byte is broken into two nibbles : the higher order nibble(bit4 ~ 7) designates the access time to a granularity of 1ns ; the value presented by the lower order nibble has a granularity of 1/10ns and is added to the value of the higher nibble. Samsung SDRAM has the different cycle time @CAS latency of 2, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 25 : SDRAM cycle time from clock @CAS latency of 1

This field describes the total minimum cycle time(clock period) for the SDRAM. For example, if the SDRAM supports CAS latency of 3, 2 and 1 (as indicated in byte 18), this byte defines tCC for CAS latency of 1. The byte is broken into two pieces : the higher order piece(bit2 ~ 7) designates the cycle time to a granularity of 1ns ; the value presented by the lower order piece has a granularity of 1/4ns and is added to the value of the higher piece. Samsung SDRAM has the different cycle time @CAS latency of 1, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 26 : SDRAM access time from clock @CAS latency of 1

This field describes the total maximum clock to data out for the SDRAM. For example, if the SDRAM supports CAS latency of 3, 2 and 1 (as indicated in byte 18), this byte defines tSAC for CAS latency of 1. The byte is broken into two pieces : the higher order piece(bit2 ~ 7) designates the access time to a granularity of 1ns ; the value presented by the lower order piece has a granularity of 1/4ns and is added to the value of the higher piece. Samsung SDRAM has the different access time @CAS latency of 1, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 27 : Minimum row precharge time (=tRP)

Bit 0 ~ 5 of this byte describe the precharge to active minimum(=tRP) using 1ns granularity. Bits 7 and 6 are reserved for future use. Samsung SDRAM has the different value, generation by generation and binning by binning. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 28 : Minimum row active to row active delay (=tRRD)

Bit 0 ~ 5 of this byte describe the minimum row activate to row activate delay(=tRRD) using 1ns granularity. Bits 7 and 6 are reserved for future use. Samsung SDRAM has the different value, generation by generation and binning by binning. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 29 : Minimum RAS to CAS delay (=tRCD)

Bit 0 ~ 5 of this byte describe the minimum RAS to CAS delay(=tRCD) using 1ns granularity. Bits 7 and 6 are reserved for future use. Samsung SDRAM has the different value, generation by generation and binning by binning. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 30 : Minimum activate to precharge time (=tRAS)

Bit 0 ~ 5 of this byte describe the minimum activate to precharge time(=tRAS) using 1ns granularity. Bits 7 and 6 are reserved for future use. Samsung SDRAM has the different value, generation by generation and binning by binning. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 31 : Module Row density

This field describes the density of each physical Row on the SDRAM DIMM. This field will have at least one bit to "1" to represent at least one Row density. If there are more than one Row on the module(as indicated in byte 5) and they have the same density, then only one bit is set in this field. If the module has more than one Row of different sizes, then more than one bit will be set for each density represented ;

Module Row density	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If YES, the bit is "1"	512MByte	256MByte	128MByte	64MByte	32MByte	16MByte	8MByte	4MByte

Byte 32~61 : Superset information (may be used in future)

these fields are reserved for superset information. Currently, these fields are programmed by "00h" because the standardization for these fields are not fixed yet.

Byte 62 : SPD data revision code

This field identifies the SDRAM DIMM SPD data revision to which the module conforms. Currently, this field is programmed by "01h"

SPD data revision code	Byte 62
Initial release	00h
2nd edition	01h
.	.
Current Release Nov 97	12h
. .	. .

Byte 63 : Checksum for bytes 0 ~ 62

This field is the checksum for bytes 0 through 62. Currently, this byte contains the value of the low 8bits of arithmetic sum of bytes 0 through byte 62.

Byte 64 ~ 71 : Manufacturer JEDEC ID code

This field describes the manufacturer JEDEC ID code per EIA/JEP106-E. The unique code for Samsung is "CBh" only for byte64 and another bytes, bytes 65 ~ 71 are programmed by "00h" ;

JEDEC ID code	Byte 64	Byte 65	Byte 66	Byte 67	Byte 68	Byte 69	Byte 70	Byte 71
Samsung	CEh	00h	00h	00h	00h	00h	00h	00h

Byte 72 : Manufacturing location

This field identifies the manufacturing location and is programmed by binary code not ASCII ;

Manufacturing location	Byte 72
Kiheung Korea	00h
Onyang Korea	01h
. . .	. . .

Byte 73 ~ 90 : Manufacturer part # (ASCII code)

This fields describe the manufacturer part number and are programmed by ASCII code not binary.

Byte 73 : Samsung memory (ASCII code)

Samsung Korea	Byte 73
K	4Bh
. . .	. . .

Byte 74 : Samsung memory (ASCII code)

Samsung Korea	Byte 74
M	4Dh
. . .	. . .

Byte 75 : Samsung module (ASCII code)

Samsung Korea	Byte 75
M	4Dh
. . .	. . .

Byte 76 : Memory type (ASCII code)

Memory type	Byte 76
3 (168 or 200pin DIMM)	33h
4 (144pin SODIMM)	34h
. . .	. . .

Byte 77 ~ 79 : Data bits (ASCII code)

Data bits	Byte 77	Byte 78	Byte 79
64(x64, 168pin, buffered)	20h	36h	34h
. . .	. . .	. . .	. . .
66(x64, 168pin, unbuffered & SPD)	20h	36h	36h
67(x64, 168pin, unbuffered, PLL & SPD)	20h	36h	37h
. . .	. . .	. . .	. . .
72(x72, 168pin, buffered)	20h	37h	32h
. . .	. . .	. . .	. . .
74(x72, 168pin, unbuffered & SPD)	20h	37h	34h
75(x72, 168pin, register, PLL & SPD)	20h	37h	35h
. . .	. . .	. . .	. . .
79(x72, 200pin, register, PLL)	20h	37h	39h

Byte 80 : Mode & operating voltage (ASCII code)

Mode & operating voltage	Byte 80
F (EDO 3.3V)	46h
S (Sync. DRAM)	53h
. . .	. . .

Byte 81 ~ 82 : Module density (ASCII code)

Module density	Byte 81	Byte 82
1M	20h	31h
2M	20h	32h
4M	20h	34h
8M	20h	38h
16M	31h	36h
32M	33h	32h
.	.	.
.	.	.

Byte 83 : Refresh, # of banks in Comp. & interface (ASCII code)

Features	Byte 83
0 (4K ref., 2banks, LVTTL)	30h
1 (2K ref., 2banks, LVTTL)	31h
2 (4K ref., 4banks, LVTTL)	32h
.	.
.	.
.	.

Byte 84 : Composition component (ASCII code)

Composition component	Byte 84
0 (x4)	30h
3 (x8)	33h
4 (x16)	34h
.	.
.	.
.	.

Byte 85 : Component revision (ASCII code)

Component revision	Byte 85
Blank (Mother die)	20h
A (1st Rev.)	41h
B (2nd Rev.)	42h
C (3rd Rev.)	43h
.	.
.	.
.	.

Byte 86 : Package type (ASCII code)

Package type	Byte 86
T (400mil TSOP II - forward)	54h

Byte 87 : PCB revision (ASCII code)

This field is used for the expression of PCB height and distinction between new JEDEC DIMM & old JEDEC DIMM. The marked by "N" refers to 16M SDRAM based 168pin unbuffered DIMM only and "L" refers to Intel 1.0 compliant 168pin unbuffered DIMM;

PCB revision	Byte 87
Blank	20h
L	4Ch
N	4Eh
1	31h
2	32h
3	33h
. .	. .

Byte 88 : Hyphen (ASCII code)

Hyphen	Byte 88
" - "	2Dh

Byte 89 : Power (ASCII code)

Power	Byte 89
G (Auto & self Ref., normal power)	47h
F (Auto & self Ref., low power)	46h

Byte 90 : Minimum cycle time (ASCII code)

Minimum cycle time	Byte 90
7 (7ns=143MHz)	37h
8 (8ns=125MHz)	38h
. . .	. . .
0 (10ns=100MHz)	30h
. . .	. . .
2 (12ns=83MHz)	32h
. . .	. . .

Byte 91 : Manufacturer revision code for PCB (ASCII code)

This field is refered to the module PCB revision and has the same programming code with byte 87.

Byte 92 : Manufacturer revision code for component (ASCII code)

This field is refered to the component revision and has the same programming code with byte 85.

Byte 93 : Manufacturing date : Week (Binary code)

This field describes manufacturing week and is increased sequently from "01h" whenever manufacturing week is varied.

Byte 94 : Manufacturing date : Year (Binary code)

This field describes manufacturing year and currently is programmed by "61h", which signifies '97.

Byte 95 ~ 98 : Assembly serial number (Binary code)

These fields describe assembly serial number. But, all of the Samsung modules are controlled by another way, not assembly serial #. Currently, this field is programmed by "00h".

Byte 99 ~ 125 : Manufacturer specific data (may be used in future)

These bytes are Undefined and can be used for Samsung 's own purpose.

Byte 126 : System frequency for 66MHz

System frequency	Byte 126
66MHz	66h

Byte 127 : CAS latency for 66MHz

CAS latency for 66MHz	Byte 127
Support 2 & 3 for 66MHz	06h

Byte 128 ~ 255 : Unused storage locations

These bytes are Undefined and can be used for Samsung 's own purpose.



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